

TPS61193-Q1 具有三条 100mA 通道的低 EMI 汽车 LED 驱动器

1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果：
 - 器件温度 1 级：-40°C 至 +125°C 的环境运行温度范围
- 输入电压工作范围：4.5V 至 40V
- 三路高精度电流阱
 - 电流匹配度为 1%（典型值）
 - 发光二极管 (LED) 灯串电流高达 100mA/通道
 - 输出可在外部合并，从而提高电流能力
- 100Hz 下的调光比率高达 10000:1
- 用于 LED 灯串电源的集成升压/SEPIC 转换器
 - 输出电压高达 45V
 - 开关频率：300kHz 至 2.2MHz
 - 开关同步输入
 - 扩展频谱，用于降低电磁干扰 (EMI)
- 丰富的故障检测功能 特性
 - 故障输出
 - 输入电压过压保护 (OVP)、欠压锁定 (UVLO) 和过流保护 (OCP)
 - 开路和短路 LED 故障检测
 - 热关断
- 最大限度减少外部组件数

2 应用

- 为以下应用提供背光：
 - 汽车信息娱乐系统
 - 汽车仪表盘
 - 智能车镜
 - 抬头显示屏 (HUD)
 - 中央信息显示屏 (CID)
 - 音视频导航 (AVN)

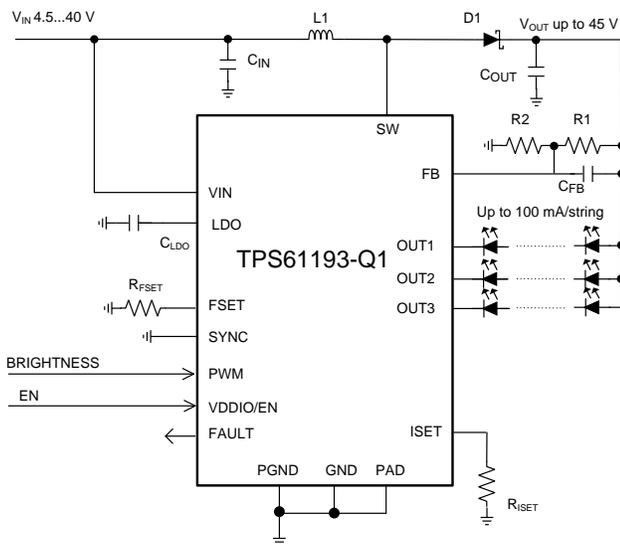
3 说明

TPS61193-Q1 是一款集成有 DC-DC 转换器的低 EMI 且易于使用的汽车类高效 LED 驱动器。DC-DC 转换器支持升压和 SEPIC 工作模式。该器件具有三路高精度电流阱，可组合在一起使用，以提高电流能力。

DC-DC 转换器可基于 LED 电流阱余量电压提供自适应输出电压控制。该特性可在所有条件下将电压调节到能够满足需要的最低水平，从而更大幅度降低功耗。为了降低 EMI，DC-DC 转换器支持针对开关频率进行扩频以及使用专用引脚实现外部同步。凭借宽范围可调频率，TPS61193-Q1 能够避免 AM 无线电频带的干扰。

TPS61193-Q1 的输入电压范围为 4.5V 至 40V，支持汽车启动/停止以及负载突降的情况。TPS61193-Q1 集成了丰富的故障检测 功能的反馈。

简化原理图



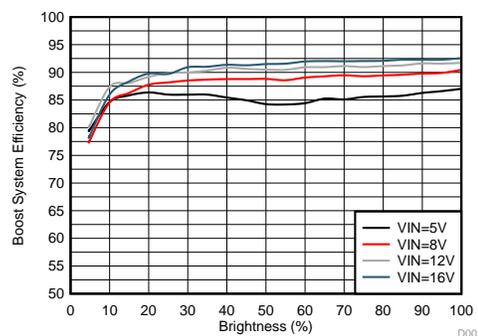
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器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPS61193-Q1	HTSSOP (20)	6.50mm x 4.40mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

系统效率



D001



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (April 2017) to Revision C	Page
• Enhanced pin descriptions for pins 3, 10 and 16 in <i>Pin Functions</i> table	3
• Deleted "Dimming ratio is calculated as ratio between the input PWM period and minimum on/off time (0.5 μ s). " from <i>Brightness Control</i>	14

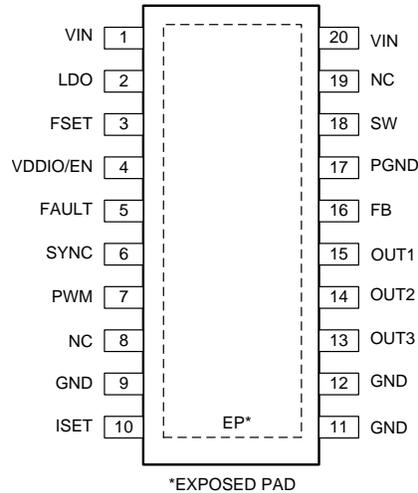
Changes from Revision A (October 2016) to Revision B	Page
• Deleted " $I_{OUT} = 100$ mA" from $t_{ON/OFF}$ row of <i>PWM Brightness Control Electrical Characteristics</i>	6
• Changed "0.5" from MAX to TYP column in $t_{ON/OFF}$ row of <i>PWM Brightness Control Electrical Characteristics</i> ; add note 1 to <i>PWM Brightness Control Electrical Characteristics</i>	6
• Added table note 1 for <i>Boost and SEPIC Converter Characteristics</i>	7
• Deleted "Initial DC-DC voltage is about 88% of $V_{MAX BOOST}$." from <i>Integrated DC-DC Converter</i> ; change wording in last sentence before <i>Equation 1</i>	12
• Changed <i>Equation 1</i> and added "K" eq definitions; added new paragraph after <i>Figure 9</i>	12
• Added new paragraph before <i>Internal LDO</i>	14

5 器件比较表

	LP8860-Q1	LP8862-Q1	LP8861-Q1	TPS61193-Q1	TPS61194-Q1	TPS61196-Q1
VIN 范围	3V 至 48V	4.5V 至 40V	4.5V 至 45V	4.5V 至 40V	4.5V 至 40V	8V 至 30V
LED 通道的数量	4	2	4	3	4	6
LED 电流/通道	150mA	160mA	100mA	100mA	100mA	200mA
I2C/SPI 支持	有	无	无	无	无	无
SEPIC 支持	无	有	是	是	是	无

6 Pin Configuration and Functions

PWP Package
20-Pin TSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	VIN	A	Input power pin
2	LDO	A	Output of internal LDO; connect a 1- μ F decoupling capacitor between this pin and noise-free GND.
3	FSET	A	DC-DC (boost or SEPIC) switching frequency setting resistor; for normal operation, resistor value from 24 k Ω to 219 k Ω must be connected between this pin and ground.
4	VDDIO/EN	I	Enable input for the device as well as supply input (VDDIO) for digital pins
5	FAULT	OD	Fault signal output. If unused, the pin may be left floating.
6	SYNC	I	Input for synchronizing boost. If synchronization is not used, connect this pin to GND to disable spread spectrum or to VDDIO/EN to enable spread spectrum.
7	PWM	I	PWM dimming input.
8	NC	—	No connect
9	GND	G	Ground.
10	ISET	A	LED current setting resistor; for normal operation, resistor value from 24 k Ω to 129 k Ω must be connected between this pin and ground.
11	GND	G	Ground
12	GND	G	Ground
13	OUT3	A	Current sink output; this pin must be connected to GND if not used.
14	OUT2	A	Current sink output This pin must be connected to GND if not used.
15	OUT1	A	Current sink output This pin must be connected to GND if not used.
16	FB	A	DC-DC (boost or SEPIC) feedback input; ; for normal operation this pin must be connected to the middle of a resistor divider between VOUT and ground using feedback resistor values between 5 k Ω and 150 k Ω .
17	PGND	G	DC-DC (boost or SEPIC) power ground
18	SW	A	DC-DC (boost or SEPIC) switch pin
19	NC	A	No connect
20	VIN	A	Input power pin

(1) A: Analog pin, G: Ground pin, P: Power pin, I: Input pin, I/O: Input/Output pin, O: Output pin, OD: Open Drain pin

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Voltage on pins	VIN, SW, FB	-0.3	50	V
	OUT1, OUT2, OUT3	-0.3	45	
	LDO, SYNC, FSET, ISET, PWM, VDDIO/EN, FAULT	-0.3	5.5	
Continuous power dissipation ⁽³⁾		Internally Limited		
Ambient temperature range T_A ⁽⁴⁾		-40	125	°C
Junction temperature range T_J ⁽⁴⁾		-40	150	°C
Maximum lead temperature (soldering)			See ⁽⁵⁾	
Storage temperature, T_{stg}		-65	150	°C

- Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are with respect to the potential at the GND pins.
- Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J = 165^\circ\text{C}$ (typical) and disengages at $T_J = 145^\circ\text{C}$ (typical).
- In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 150^\circ\text{C}$), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$.
- For detailed soldering specifications and information, refer to [PowerPAD™ Thermally Enhanced Package](#).

7.2 ESD Ratings

		VALUE	UNIT	
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V	
	Charged-device model (CDM), per AEC Q100-011	All other pins		±500
		Corner pins (1,10,11,20)		±750

- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage on pins	VIN	4.5	45	V
	SW	0	45	
	OUT1, OUT2, OUT3	0	40	
	FB, FSET, LDO, ISET, VDDIO/EN, FAULT	0	5.25	
	SYNC, PWM	0	VDDIO/EN	

- All voltages are with respect to the potential at the GND pins.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS61193-Q1	UNIT
		PWP (TSSOP)	
		20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	44.2	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	26.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	22.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	22.2	°C/W
R _{θJcbot}	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

7.5 Electrical Characteristics⁽¹⁾⁽²⁾

T_J = -40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _Q	Standby supply current	Device disabled, V _{VDDIO/EN} = 0 V, V _{IN} = 12 V		4.5	20	μA
	Active supply current	V _{IN} = 12 V, V _{OUT} = 26 V, output current 80 mA/channel, converter f _{SW} = 300 kHz		5	12	mA
V _{POR_R}	Power-on reset rising threshold	LDO pin voltage			2.7	V
V _{POR_F}	Power-on reset falling threshold	LDO pin voltage	1.5			V
T _{TSD}	Thermal shutdown threshold		150	165	175	°C
T _{TSD_HYST}	Thermal shutdown hysteresis			20		°C

(1) All voltages are with respect to the potential at the GND pins.

(2) Minimum and maximum limits are specified by design, test, or statistical analysis.

7.6 Internal LDO Electrical Characteristics

T_J = -40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{LDO}	Output voltage	V _{IN} = 12 V	4.15	4.3	4.55	V
V _{DR}	Dropout voltage		120	300	430	mV
I _{SHORT}	Short circuit current			50		mA

7.7 Protection Electrical Characteristics

 $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	VIN OVP threshold voltage		41	42	44	V
V_{UVLO}	VIN UVLO			4		V
V_{UVLO_HYST}	VIN UVLO hysteresis			100		mV
	LED short detection threshold		5.6	6	7	V

7.8 Current Sinks Electrical Characteristics

 $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKAGE}$	Leakage current	Outputs OUT1 to OUT3, $V_{OUTx} = 45\text{ V}$		0.1	5	μA
I_{MAX}	Maximum current	OUT1, OUT2, OUT3		100		mA
I_{OUT}	Output current accuracy	$I_{OUT} = 100\text{ mA}$	-5%		5%	
I_{MATCH}	Output current matching ⁽¹⁾	$I_{OUT} = 100\text{ mA}$, PWM duty = 100%		1%	5%	
V_{SAT}	Saturation voltage ⁽²⁾	$I_{OUT} = 100\text{ mA}$		0.4	0.7	V

- (1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUTx), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Matching number is calculated: $(MAX-MIN)/AVG$. The typical specification provided is the most likely norm of the matching figure for all parts. LED current sinks were characterized with 1-V headroom voltage. Note that some manufacturers have different definitions in use.
- (2) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1 V.

7.9 PWM Brightness Control Electrical Characteristics

 $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM}	PWM input frequency		100		20 000	Hz
$t_{ON/OFF}$	Minimum on/off time ⁽¹⁾			0.5		μs

- (1) This specification is not ensured by ATE.

7.10 Boost and SEPIC Converter Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (unless otherwise noted).

Unless otherwise specified: $V_{IN} = 12\text{ V}$, $V_{EN/VDDIO} = 3.3\text{ V}$, $L = 22\text{ }\mu\text{H}$, $C_{IN} = 2 \times 10\text{-}\mu\text{F}$ ceramic and $33\text{-}\mu\text{F}$ electrolytic, $C_{OUT} = 2 \times 10\text{-}\mu\text{F}$ ceramic and $33\text{-}\mu\text{F}$ electrolytic, $D = \text{NRVB460MFS}$, $f_{SW} = 300\text{ kHz}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5		40	V
V_{OUT}	Output voltage		6		45	
f_{SW_MIN}	Minimum switching frequency (central frequency if spread spectrum is enabled)	Defined by R_{FSET} resistor		300		kHz
f_{SW_MAX}	Maximum switching frequency (central frequency if spread spectrum is enabled)			2 200		kHz
V_{OUT}/V_{IN}	Conversion ratio				10	
T_{OFF}	Minimum switch OFF time ⁽¹⁾	$f_{SW} \geq 1.15\text{ MHz}$			55	ns
I_{SW_MAX}	SW current limit		1.8	2	2.2	A
R_{DSON}	FET R_{DSON}	Pin-to-pin		240	400	m Ω
f_{SYNC}	External SYNC frequency		300		2 200	kHz
$t_{SYNC_ON_MIN}$	External SYNC minimum on time ⁽¹⁾			150		ns
$t_{SYNC_OFF_MIN}$	External SYNC minimum off time ⁽¹⁾			150		ns

(1) This specification is not ensured by ATE.

7.11 Logic Interface Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT VDDIO/EN						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.65			
I_I	Input current		-1	5	30	μA
LOGIC INPUT SYNC/FSET, PWM						
V_{IL}	Input low level			$0.2 \times V_{DDIO/EN}$		V
V_{IH}	Input high level		$0.8 \times V_{DDIO/EN}$			
I_I	Input current		-1		1	μA
LOGIC OUTPUT FAULT						
V_{OL}	Output low level	Pullup current 3 mA		0.3	0.5	V
$I_{LEAKAGE}$	Output leakage current	$V = 5.5\text{ V}$			1	μA

7.12 Typical Characteristics

Unless otherwise specified: D = NRVB460MFS, T = 25°C

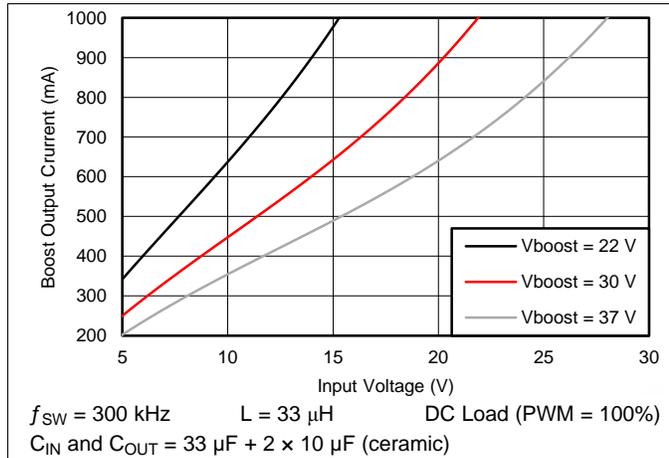


Figure 1. Maximum Boost Current

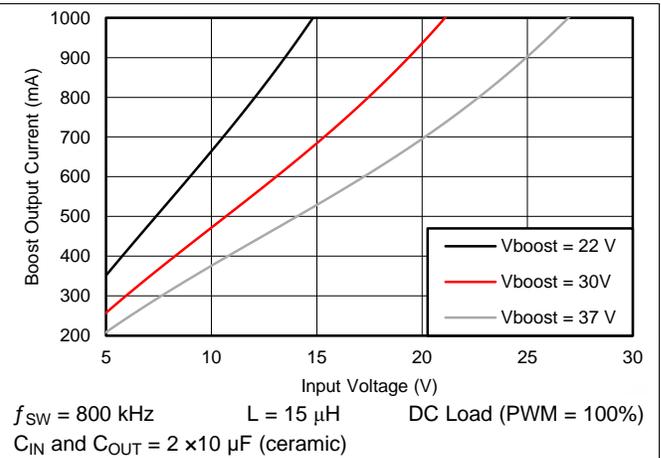


Figure 2. Maximum Boost Current

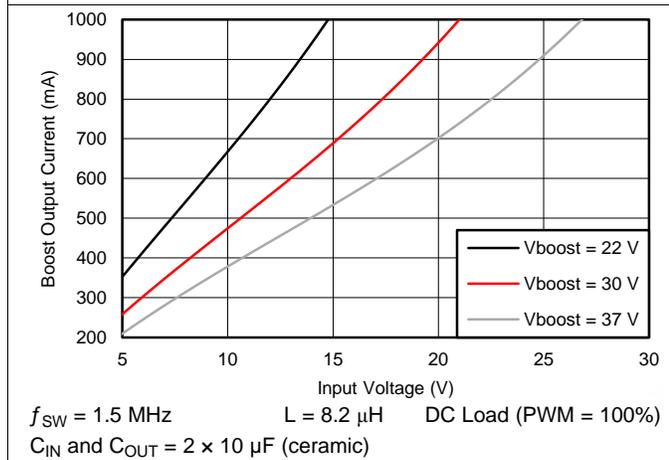


Figure 3. Maximum Boost Current

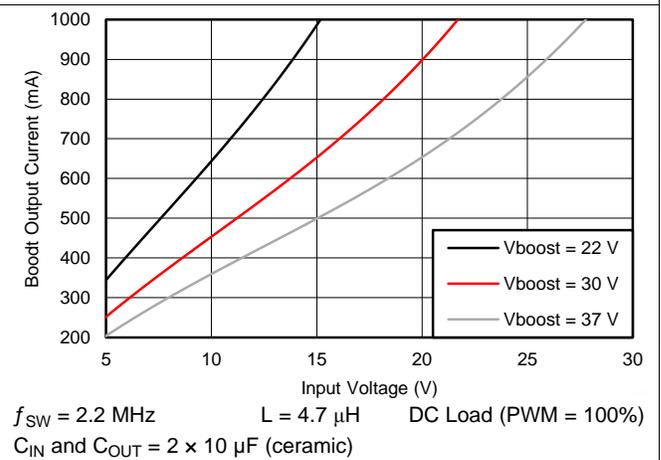


Figure 4. Maximum Boost Current

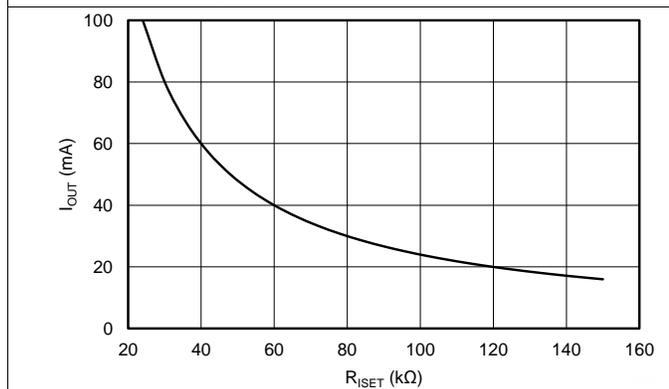


Figure 5. LED Current vs R_{ISET}

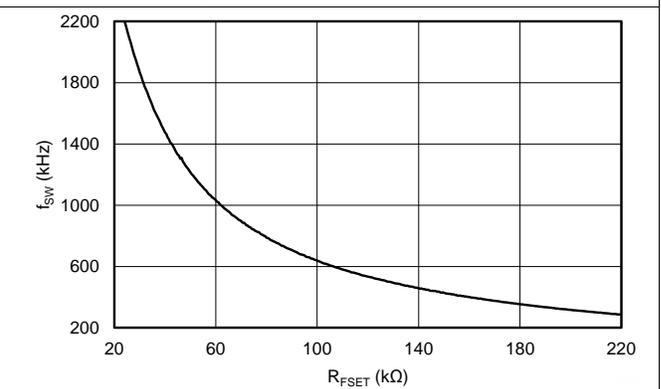
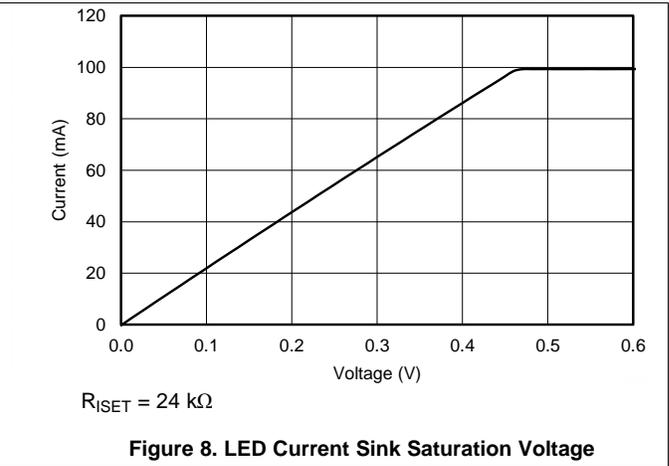
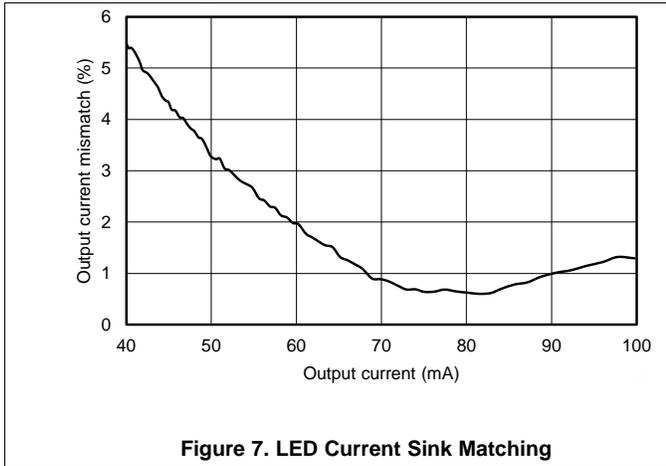


Figure 6. Boost Switching Frequency f_{SW} vs R_{FSET}

Typical Characteristics (continued)

Unless otherwise specified: D = NRVB460MFS, T = 25°C



8 Detailed Description

8.1 Overview

The TPS61193-Q1 is a highly integrated LED driver for automotive infotainment, lighting systems, and medium-sized LCD backlight applications. It includes a DC-DC with an integrated FET, supporting both boost and SEPIC modes, an internal LDO enabling direct connection to battery without need for a pre-regulated supply and three LED current sinks. The VDDIO/EN pin provides the supply voltage for digital IOs (PWM and SYNC inputs) and at the same time enables the device.

The switching frequency on the DC-DC converter is set by a resistor connected to the FSET pin. The maximum voltage of the DC-DC is set by a resistive divider connected to the FB pin. For the best efficiency the output voltage is adapted automatically to the minimum necessary level needed to drive the LED strings. This is done by monitoring LED output voltage drop in real time. For EMI reduction and control two optional features are available:

- Spread spectrum, which reduces EMI noise around the switching frequency and its harmonic frequencies
- DC-DC can be synchronized to an external frequency connected to SYNC pin

The three constant current sinks OUT1, OUT2, and OUT3 provide LED current up to 100 mA. Value for the current per OUT pin is set with a resistor connected to ISET pin. Current sinks that are not used must be connected to ground. Grounded current sink is disabled and excluded from adaptive voltage detection loop.

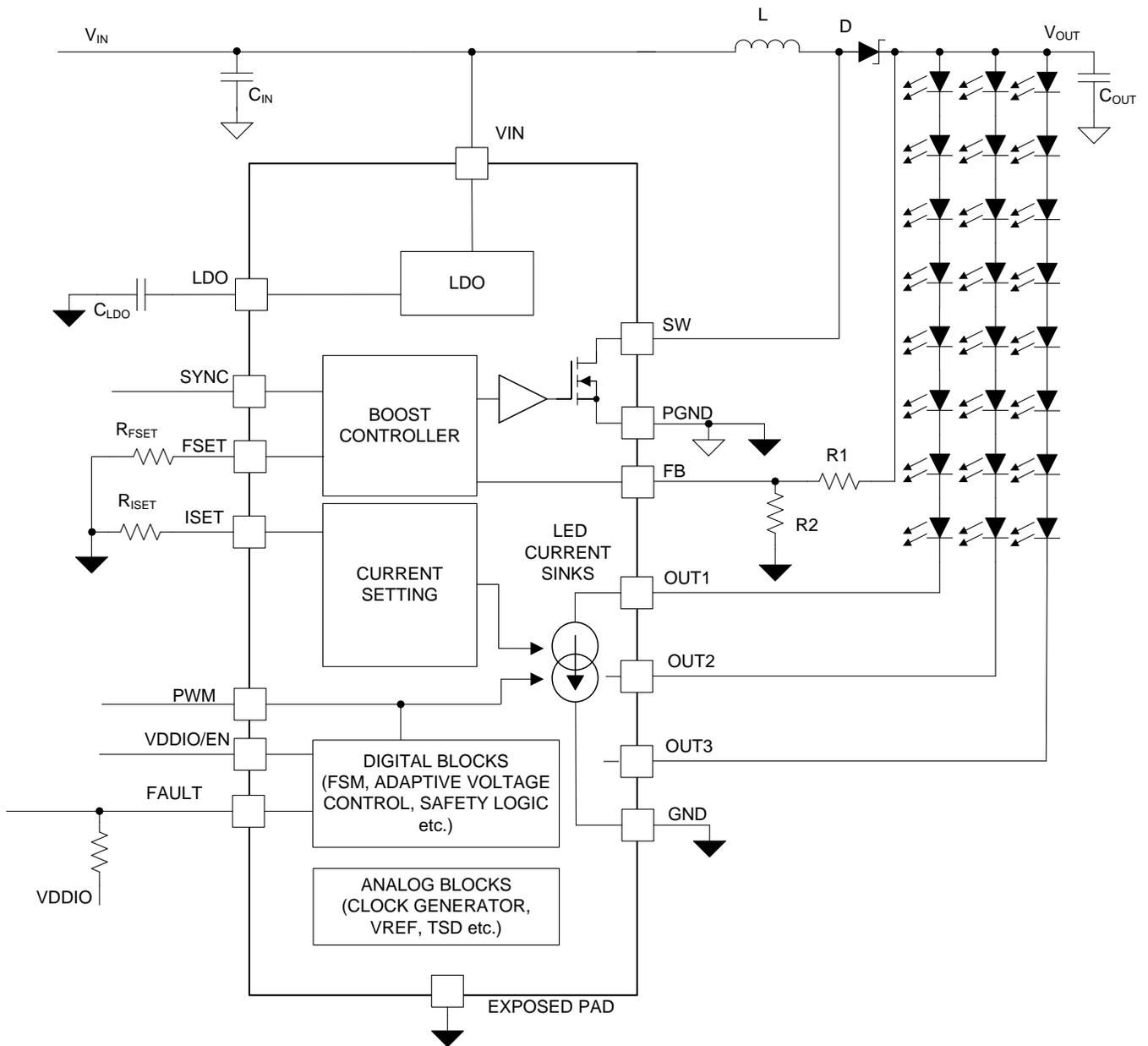
Brightness is controlled with the PWM input. Frequency range for the input PWM is from 100 Hz to 20 kHz. LED output PWM follows the input PWM so the output frequency is equal to the input frequency.

TPS61193-Q1 has extensive fault detection features :

- Open-string and shorted LED detections
 - LED fault detection prevents system overheating in case of open or short in some of the LED strings
- V_{IN} input overvoltage protection
 - Threshold sensing from VIN pin
- V_{IN} input undervoltage protection
 - Threshold sensing from VIN pin
- Thermal shutdown in case of die overtemperature

Fault condition is indicated through the FAULT output pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Integrated DC-DC Converter

The TPS61193-Q1 DC-DC converter generates supply voltage for the LEDs and can operate in boost mode or in SEPIC mode. The maximum output voltage V_{OUT_MAX} is defined by an external resistive divider (R_1 , R_2).

V_{OUT_MAX} voltage should be chosen based on the maximum voltage required for LED strings. Recommended maximum voltage is about 30% higher than maximum LED string voltage. DC-DC output voltage is adjusted automatically based on LED current sink headroom voltage. Maximum, minimum, and initial boost voltages can be calculated with Equation 1:

$$V_{BOOST} = \left(\frac{V_{BG}}{R_2} + K \times 0.0387 \right) \times R_1 + V_{BG}$$

where

- $V_{BG} = 1.2$ V
- R_2 recommended value is 130 k Ω
- Resistor values are in k Ω
- $K = 1$ for maximum adaptive boost voltage (typical)
- $K = 0$ for minimum adaptive boost voltage (typical)
- $K = 0.88$ for initial boost voltage (typical)

(1)

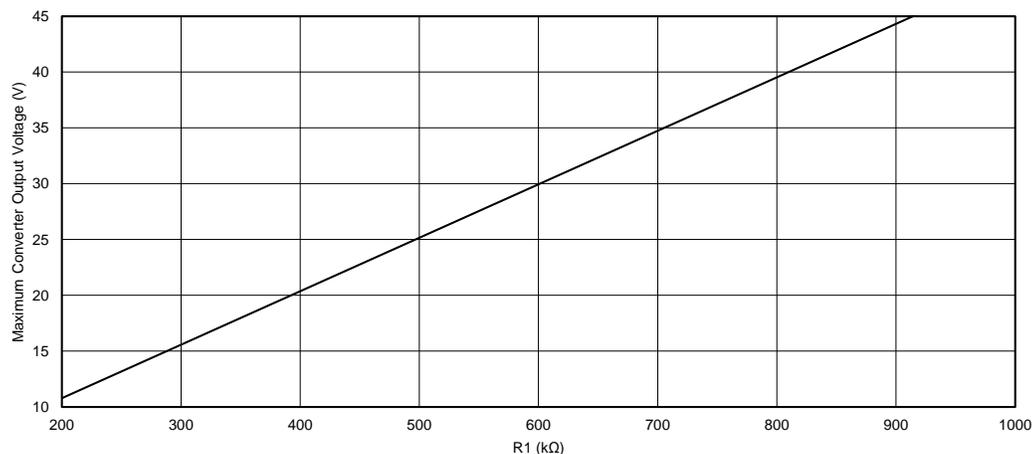


Figure 9. Maximum Converter Output Voltage vs R1 Resistance

Alternatively, a T-divider can be used if resistance less than 100 k Ω is required for the external resistive divider. Refer to [Using the TPS61193EVM and TPS61193-Q1EVM Evaluation Module](#) for details.

The converter is a current mode DC-DC converter, where the inductor current is measured and controlled with the feedback. Switching frequency is adjustable between 250 kHz and 2.2 MHz with R_{FSET} resistor as Equation 2:

$$f_{SW} = 67600 / (R_{FSET} + 6.4)$$

where

- f_{SW} is switching frequency, kHz
- R_{FSET} is frequency setting resistor, k Ω

(2)

In most cases lower frequency has higher system efficiency. DC-DC internal parameters are chosen automatically according to the selected switching frequency (see Table 2) to ensure stability. In boost mode a 15-pF capacitor C_{FB} must be placed across resistor R_1 when operating in 300-kHz to 500-kHz range (see [Typical Application for 3 LED Strings](#)). When operating in the 1.8-MHz to 2.2-MHz range $C_{FB} = 4.7$ pF.

Feature Description (continued)

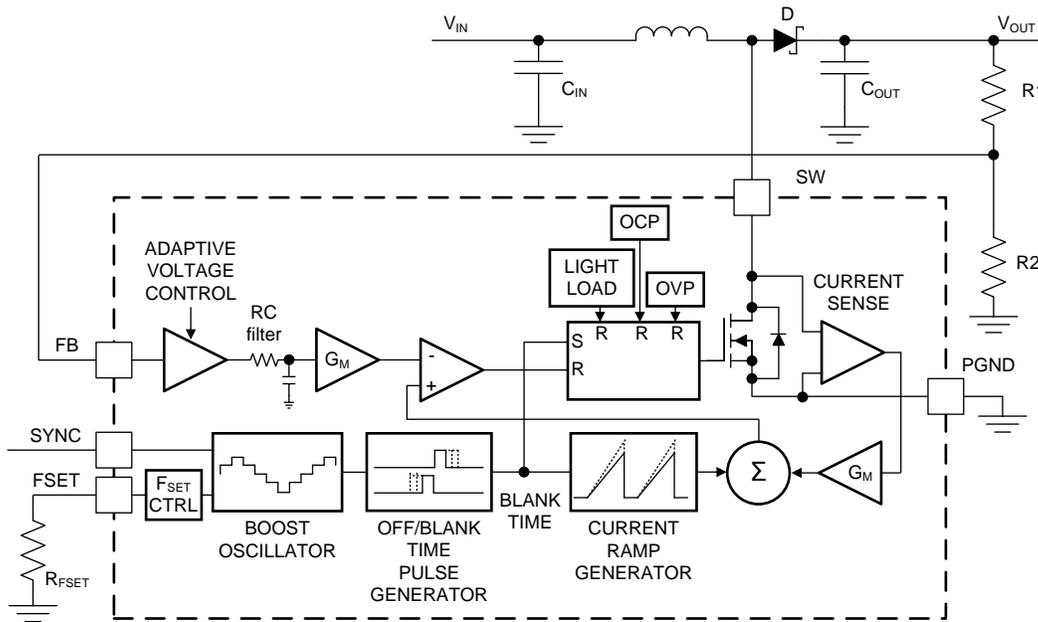


Figure 10. Boost Block Diagram

DC-DC can be driven by an external SYNC signal between 300 kHz and 2.2 MHz. If the external synchronization input disappears, DC-DC continues operation at the frequency defined by R_{FSET} resistor. When external frequency disappears and SYNC pin level is low, converter continues operation without spread spectrum immediately. If SYNC remains high, converter continues switching with spread spectrum enabled after 256 μ s.

External SYNC frequency must be 1.2 to 1.5 times higher than the frequency defined by R_{FSET} resistor. Minimum frequency setting with R_{FSET} is 250 kHz to support 300-kHz switching with external clock.

The optional spread spectrum feature ($\pm 3\%$ from central frequency, 1-kHz modulation frequency) reduces EMI noise at the switching frequency and its harmonic frequencies. When external synchronization is used, spread spectrum is not available.

Table 1. DC-DC Synchronization Mode

SYNC PIN INPUT	MODE
Low	Spread spectrum disabled
High	Spread spectrum enabled
300 to 2200 kHz frequency	Spread spectrum disabled, external synchronization mode

Table 2. DC-DC Parameters⁽¹⁾

RANGE	FREQUENCY (kHz)	TYPICAL INDUCTANCE (μ H)	TYPICAL BOOST INPUT AND OUTPUT CAPACITORS (μ F)	MINIMUM SWITCH OFF TIME (ns) ⁽²⁾	BLANK TIME (ns)	CURRENT RAMP (A/s)	CURRENT RAMP DELAY (ns)
1	300 to 480	33	2 x 10 (cer.) + 33 (electr.)	150	95	24	550
2	480 to 1150	15	10 (cer.) + 33 (electr.)	60	95	43	300
3	1150 to 1650	10	3 x 10 (cer.)	40	95	79	0
4	1650 to 2200	4.7	3 x 10 (cer.)	40	70	145	0

(1) Parameters are for reference only

(2) Due to current sensing comparator delay the actual minimum off time is 6 ns (typical) longer than in the table.

The converter SW pin DC current is limited to 2 A (typical). To support warm-start transient conditions the current limit is automatically increased to 2.5 A for a short period of 1.5 seconds when a 2-A limit is reached.

NOTE

Application condition where the 2-A limit is exceeded continuously is not allowed. In this case the current limit would be 2 A for 1.5 seconds followed by 2.5-A limit for 1.5 seconds, and this 3-second period repeats.

To keep switching voltage within safe levels there is a 48-V limit comparator in the event that FB loop is broken.

8.3.2 Internal LDO

The internal LDO regulator converts the input voltage at VIN to a 4.3-V output voltage for internal use. Connect a minimum of 1- μ F ceramic capacitor from LDO pin to ground, as close to the LDO pin as possible.

8.3.3 LED Current Sinks

8.3.3.1 Output Configuration

TPS61193-Q1 detects LED output configuration during start-up. Any current sink output connected to ground is disabled and excluded from the adaptive voltage control of the DC-DC and fault detections.

8.3.3.2 Current Setting

Maximum current for the LED outputs is controlled with external R_{ISET} resistor. R_{ISET} value for target maximum current can be calculated using [Equation 3](#):

$$R_{ISET} = 2342 / (I_{OUT} - 2.5)$$

where

- R_{ISET} is current setting resistor, k Ω
 - I_{LED} is output current per output, mA
- (3)

8.3.3.3 Brightness Control

TPS61193-Q1 controls the brightness of the display with conventional PWM. Output PWM directly follows the input PWM. Input PWM frequency can be in the range of 100 Hz to 20 kHz.

8.3.4 Protection and Fault Detections

The TPS61193-Q1 has fault detection for LED open and short, VIN input overvoltage protection (VIN_OVP), VIN undervoltage lockout (VIN_UVLO), and thermal shutdown (TSD).

8.3.4.1 Adaptive DC-DC Voltage Control and Functionality of LED Fault Comparators

Adaptive voltage control function adjusts the DC-DC output voltage to the minimum sufficient voltage for proper LED current sink operation. The current sink with highest V_F LED string is detected and DC-DC output voltage adjusted accordingly. DC-DC adaptive control voltage step size is defined by maximum voltage setting, $V_{STEP} = (V_{OUT_MAX} - V_{OUT_MIN}) / 256$. Periodic down pressure is applied to the target voltage to achieve better system efficiency.

Every LED current sink has 3 comparators for the adaptive DC-DC control and LED fault detections. Comparator outputs are filtered, filtering time is 1 μ s.

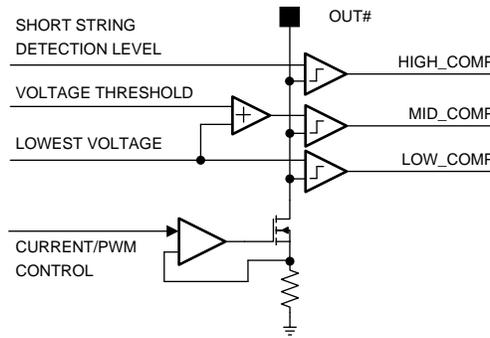


Figure 11. Comparators for Adaptive Voltage Control and LED Fault Detection

Figure 12 shows different cases which cause DC-DC voltage increase, decrease, or generate faults. In normal operation voltage at all the OUT# pins is between LOW_COMP and MID_COMP levels, and boost voltage stays constant. LOW_COMP level is the minimum for proper LED current sink operation, $1.1 \times V_{SAT} + 0.2 \text{ V}$ (typical). MID_COMP level is $1.1 \times V_{SAT} + 1.2 \text{ V}$ (typical) so typical headroom window is 1 V.

When voltage at all the OUT# pins increases above MID_COMP level, DC-DC voltage adapts downwards.

When voltage at any of the OUT# pins falls below LOW_COMP threshold, DC-DC voltage adapts upwards. In the condition where DC-DC voltage reaches the maximum and there are one or more outputs still below LOW_COMP level, an open LED fault is detected.

HIGH_COMP level, 6 V typical, is the threshold for shorted LED detection. When the voltage of one or more of the OUT# pins increases above HIGH_COMP level and at least one of the other outputs is within the normal headroom window, shorted LED fault is detected.

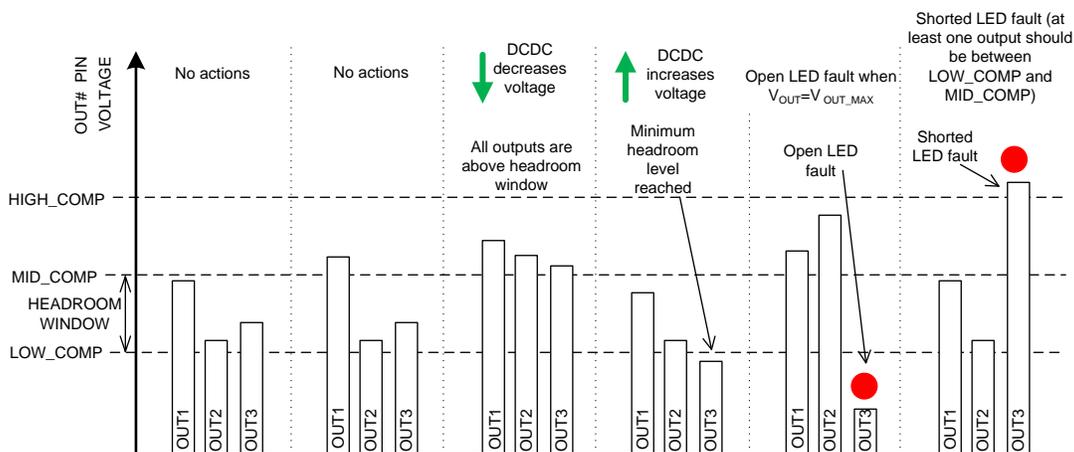


Figure 12. Protection and DC-DC Voltage Adaptation Algorithms

8.3.4.2 Overview of the Fault/Protection Schemes

A summary of the TPS61193-Q1 fault detection behavior is shown in Table 3. Detected faults (excluding LED open or short) cause device to enter FAULT_RECOVERY state. In FAULT_RECOVERY the DC-DC and LED current sinks of the device are disabled, and the FAULT pin is pulled low. The device recovers automatically and enters normal operating mode (ACTIVE) after a recovery time of 100 ms if the fault condition has disappeared. When recovery is successful, FAULT pin is released.

If a LED fault is detected, the device continues normal operation and only the faulty string is disabled. The fault is indicated via the FAULT pin which can be released by toggling VDDIO/EN pin low for a short period of 2 μs to 20 μs. LEDs are turned off for this period but the device stays in ACTIVE mode. If VDDIO/EN is low longer, the device goes to STANDBY and restarts when EN goes high again.

Table 3. Fault Detections

FAULT/ PROTECTION	FAULT NAME	THRESHOLD	FAULT PIN	FAULT RECOVERY STATE	ACTION
VIN overvoltage protection	VIN_OVP	1. $V_{IN} > 42\text{ V}$ 2. $V_{OUT} > V_{SET_DCDC} + 6..10\text{ V}$. V_{SET_DCDC} is voltage value defined by logic during adaptation	Yes	Yes	1. Overvoltage is monitored from the beginning of soft start. Fault is detected if the duration of overvoltage condition is 100 μs minimum. 2. Overvoltage is monitored from the beginning of normal operation (ACTIVE mode). Fault is detected if over-voltage condition duration is 560 ms minimum (t_{filter}). After the first fault, detection filter time is reduced to 50 ms for following recovery cycles. When the device recovers and has been in ACTIVE mode for 160 ms, filter time is increased back to 560 ms .
VIN undervoltage lockout	VIN_UVLO	Falling 3.9 V Rising 4 V	Yes	Yes	Detects undervoltage condition at VIN pin. Sensed in all operating modes. Fault is detected if undervoltage condition duration is 100 μs minimum.
Open LED fault	OPEN_LED	LOW_COMP threshold	Yes	No	Detected if the voltage of one or more current sinks is below threshold level, and DC-DC adaptive control has reached maximum voltage. Open string is removed from the DC-DC voltage control loop and current sink is disabled. Fault pin is released by toggling VDDIO/EN pin. If VDDIO/EN is low for a period of 2 μs to 20 μs, LEDs are turned off for this period but device stays ACTIVE. If VDDIO/EN is low longer, device goes to STANDBY and restarts when EN goes high again.
Shorted LED fault	SHORT_LED	Shorted string detection level 6 V	Yes	No	Detected if the voltage of one or more current sinks is above shorted string detection level and at least one OUTx voltage is within headroom window. Shorted string is removed from the DC-DC voltage control loop and current sink is disabled. Fault pin is released by toggling VDDIO/EN pin. If VDDIO/EN is low for a period of 2...20 μs, LEDs are turned off for this period but device stays ACTIVE. If VDDIO/EN is low longer, device goes to STANDBY and restarts when EN goes high again..
Thermal protection	TSD	165°C Thermal shutdown hysteresis 20°C	Yes	Yes	Thermal shutdown is monitored from the beginning of soft start. Die temperature must decrease by 20°C for device to recover.

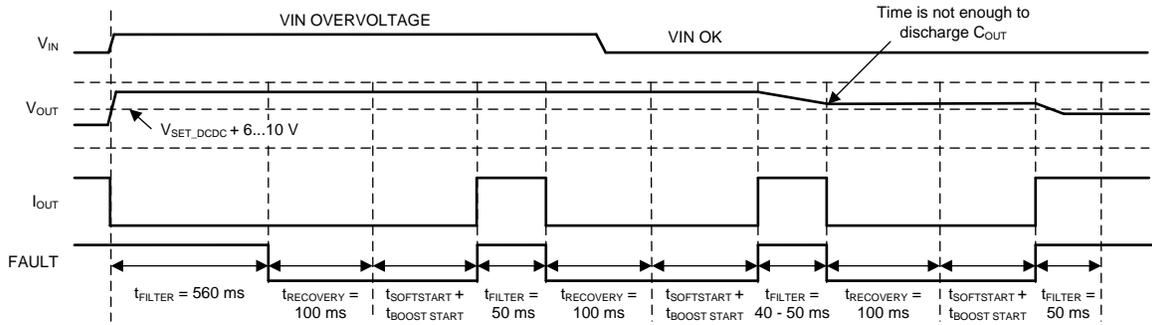


Figure 13. V_{IN} Overvoltage Protection (DC-DC OVP)

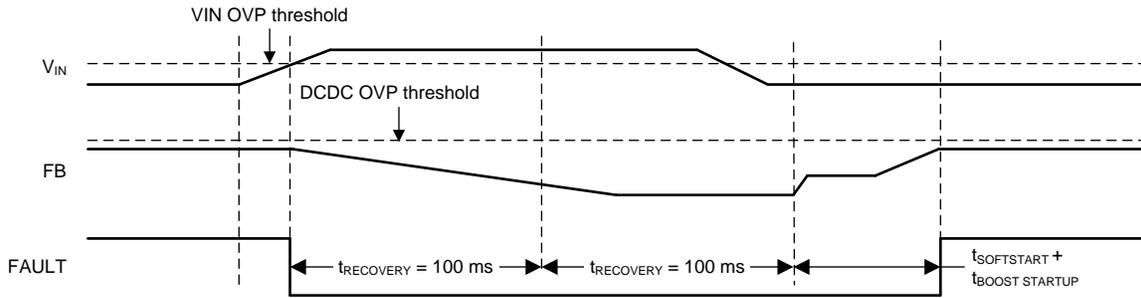


Figure 14. V_{IN} Overvoltage Protection (V_{IN} OVP)

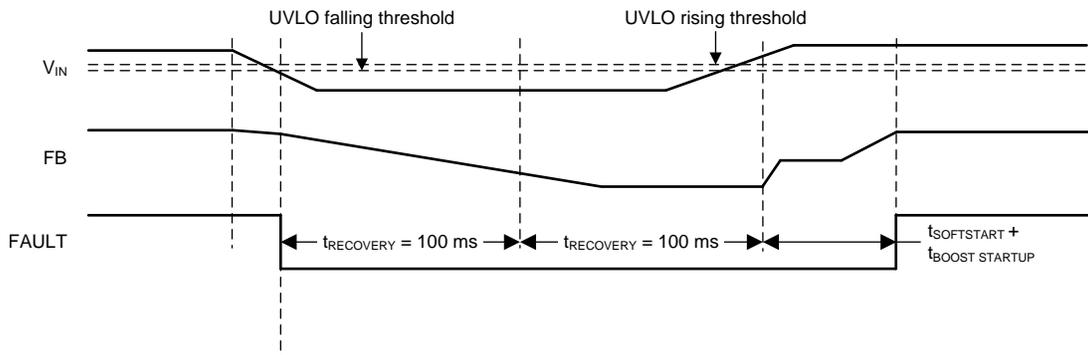
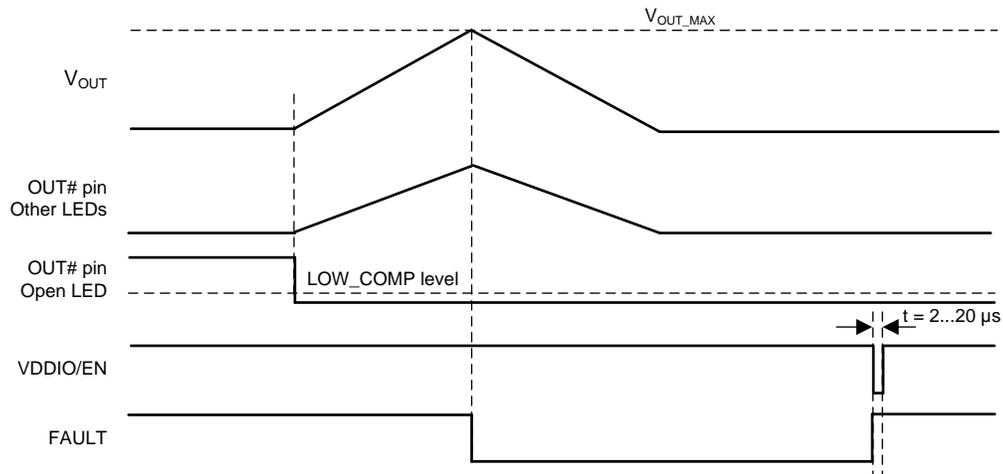
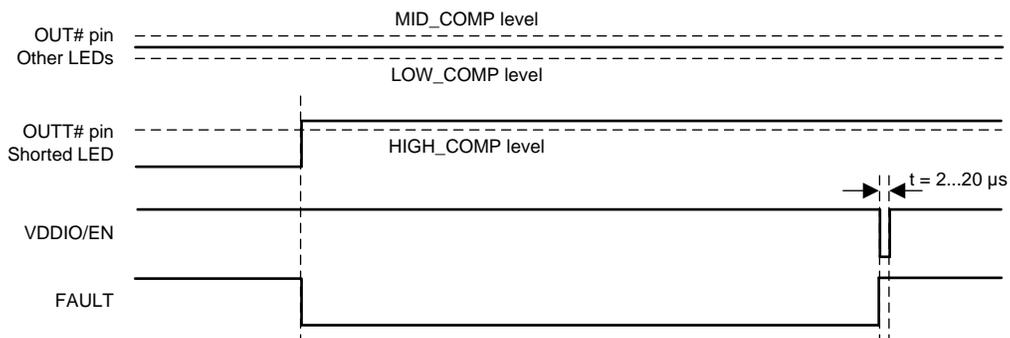


Figure 15. V_{IN} Undervoltage Lockout


Figure 16. LED Open Fault

Figure 17. LED Short Fault

8.4 Device Functional Modes

8.4.1 Device States

The TPS61193-Q1 enters STANDBY mode when the internal LDO output rises above the power-on reset level, $V_{LDO} > V_{POR}$. In STANDBY mode the device is able to detect VDDIO/EN signal. When VDDIO/EN is pulled high, the device powers up. After start LED outputs are sensed to detect grounded outputs. Grounded outputs are disabled and excluded from the adaptive voltage control loop of the DC-DC.

If a fault condition is detected, the device enters FAULT_RECOVERY state. Faults that cause the device to enter FAULT_RECOVERY are listed in [Table 3](#). When LED open or short is detected, the faulty string is disabled, but device stays in ACTIVE mode.

Device Functional Modes (continued)

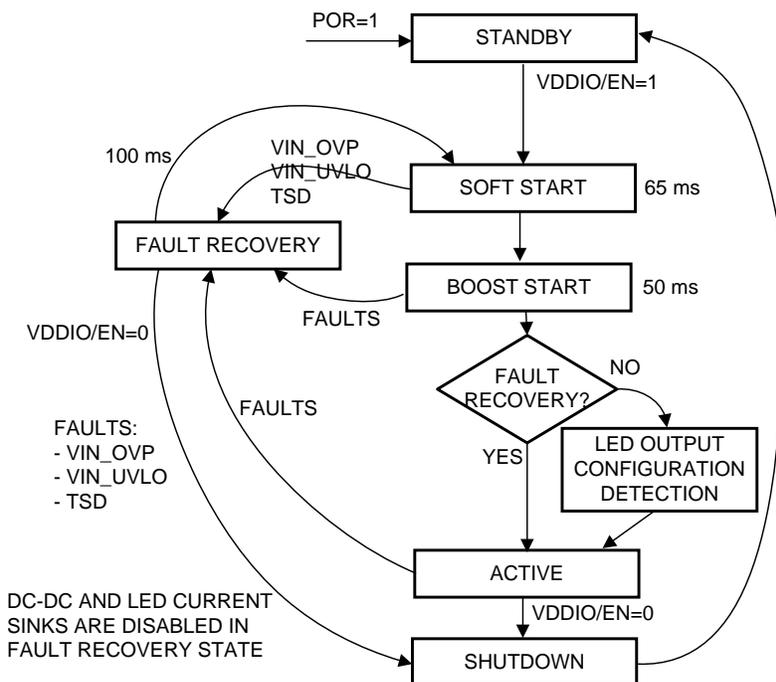


Figure 18. State Diagram

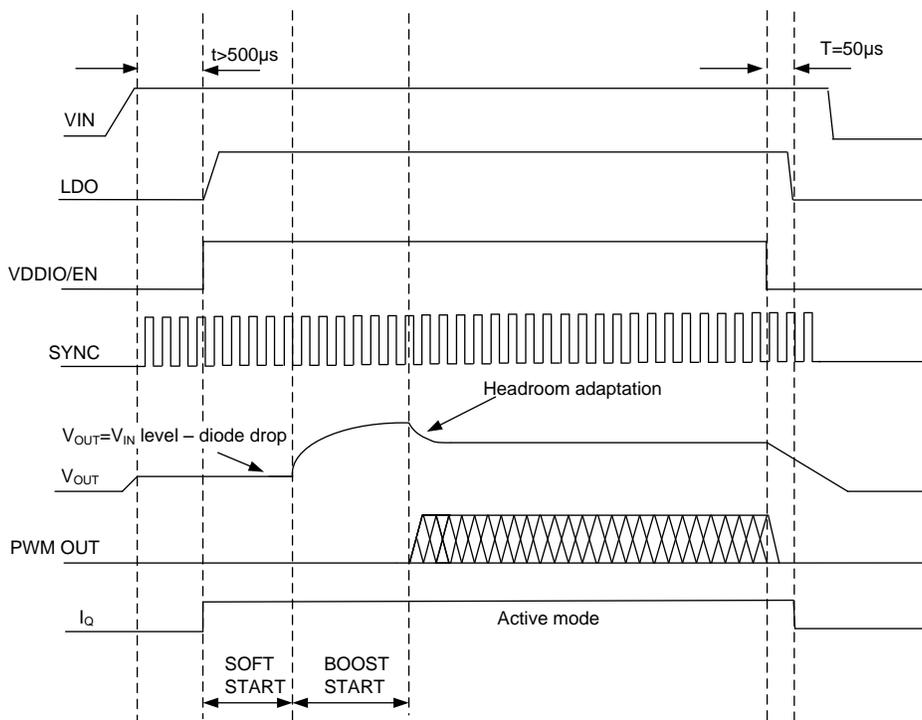


Figure 19. Timing Diagram for the Typical Start-Up and Shutdown

Typical Applications (continued)

9.2.1.1 Design Requirements

DESIGN PARAMETER	VALUE
V _{IN} voltage range	4.5 V – 28 V
LED string	3P8S LEDs (30 V)
LED string current	100 mA
Maximum boost voltage	37 V
Boost switching frequency	300 kHz
External boost sync	not used
Boost spread spectrum	enabled
L1	33 μH
C _{IN}	100 μF, 50 V
C _{IN BOOST}	2 × (10-μF, 50-V ceramic) + 33-μF, 50-V electrolytic
C _{OUT}	2 × (10-μF, 50-V ceramic) + 33-μF, 50-V electrolytic
C _{FB}	15 pF
C _{LDO}	1 μF, 10 V
R _{ISET}	24 kΩ
R _{FSET}	210 kΩ
R1	750 kΩ
R2	130 kΩ
R3	10 kΩ

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection

There are two main considerations when choosing an inductor; the inductor must not saturate, and the inductor current ripple must be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and are preferred. The saturation current must be greater than the sum of the maximum load current, and the worst case average-to-peak inductor current. Equation 4 shows the worst case conditions

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE} \quad \text{For Boost}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ and } D' = (1 - D)$$

- I_{RIPPLE} - peak inductor current
- I_{OUTMAX} - maximum load current
- V_{IN} - minimum input voltage in application
- L - min inductor value including worst case tolerances
- f - minimum switching frequency
- V_{OUT} - output voltage
- D - Duty Cycle for CCM Operation

(4)

As a result, the inductor should be selected according to the I_{SAT}. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit. A saturation current rating of at least 2.5 A is recommended for most applications. See Table 2 for recommended inductance value for the different switching frequency ranges. The inductor's resistance should be less than 300 mΩ for good efficiency.

See detailed information in *Understanding Boost Power Stages in Switch Mode Power Supplies*. Power Stage Designer™ Tool can be used for the boost calculation: <http://www.ti.com/tool/powerstage-designer>.

9.2.1.2.2 Output Capacitor Selection

A ceramic capacitor with $2 \times V_{MAX_BOOST}$ or more voltage rating is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Capacitance recommendations for different switching frequencies are shown in Table 2. To minimize audible noise of ceramic capacitors their physical size should typically be minimized.

9.2.1.2.3 Input Capacitor Selection

A ceramic capacitor with $2 \times V_{IN_MAX}$ or more voltage rating is recommended for the input capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Capacitance recommendations for different boost switching frequencies are shown in Table 2.

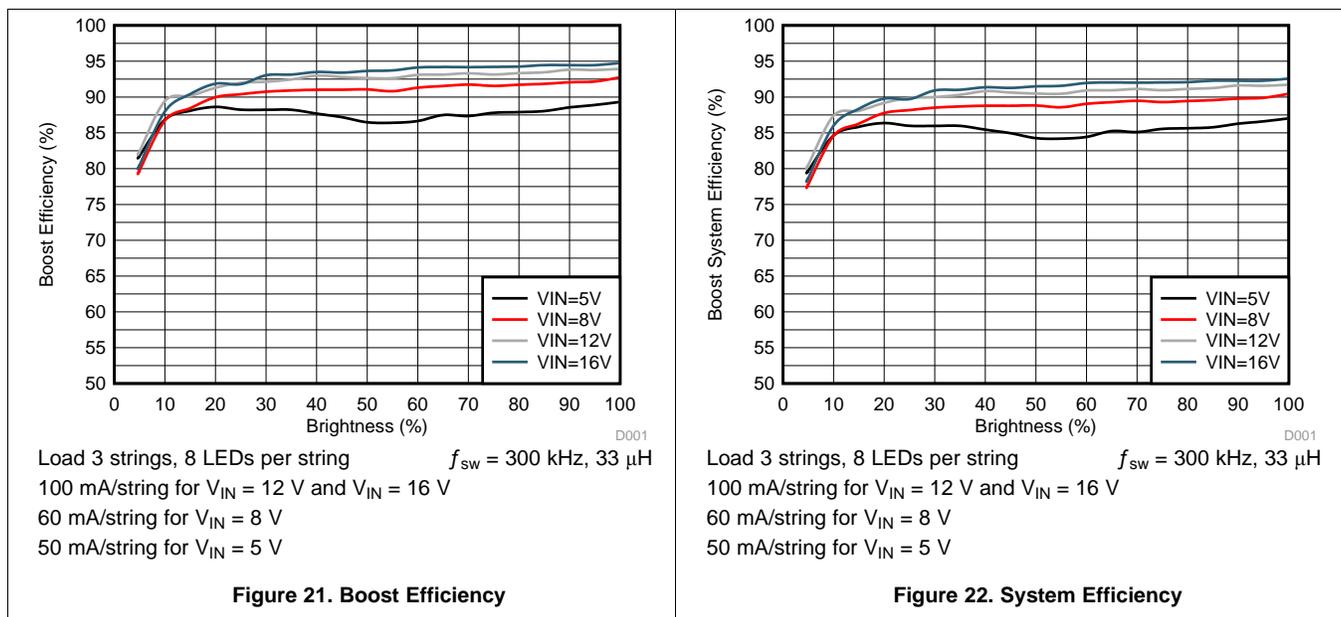
9.2.1.2.4 LDO Output Capacitor

A ceramic capacitor with at least 10-V voltage rating is recommended for the output capacitor of the LDO. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Typically a 1-μF capacitor is sufficient.

9.2.1.2.5 Diode

A Schottky diode should be used for the boost output diode. Do not use ordinary rectifier diodes because slow switching speeds and long recovery times degrade the efficiency and the load regulation. Diode rating for peak repetitive current should be greater than inductor peak current (up to 3 A) to ensure reliable operation in boost mode. Average current rating should be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. Choose a reverse breakdown voltage of the Schottky diode significantly larger than the output voltage.

9.2.1.3 Application Curves



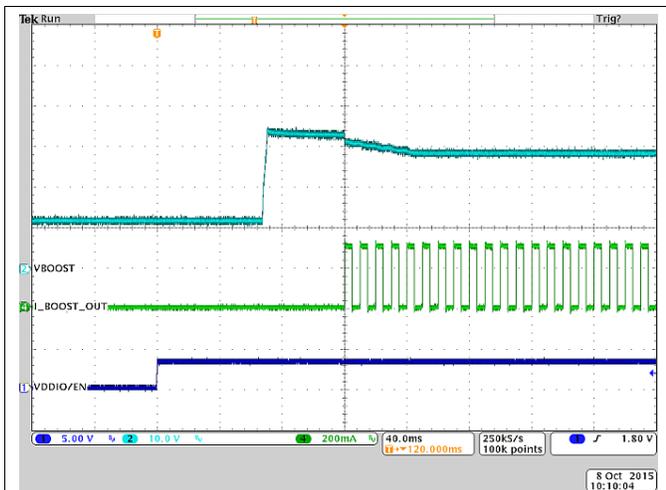


Figure 23. Typical Start-Up

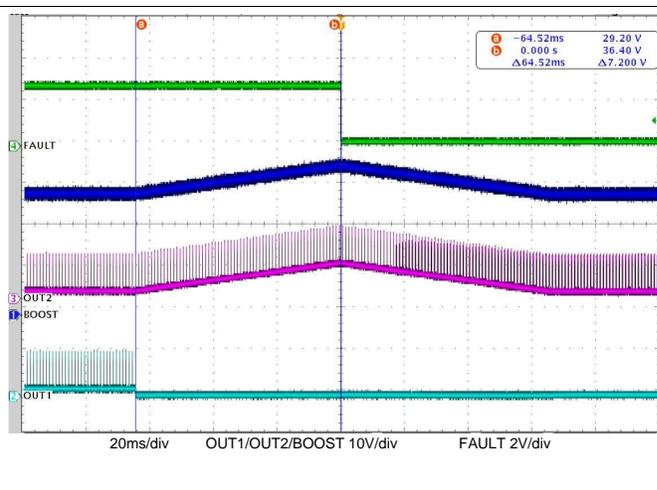


Figure 24. Open LED Fault

9.2.2 SEPIC Mode Application

When LED string voltage can be above or below V_{IN} voltage, SEPIC configuration can be used. In this example, two separate coils are used for SEPIC. This can enable lower height external components to be used, compared to a coupled coil solution. On the other hand, coupled coil typically maximizes the efficiency. Also, in this example, an external clock is used to synchronize SEPIC switching frequency. External clock input can be modulated to spread switching frequency spectrum.

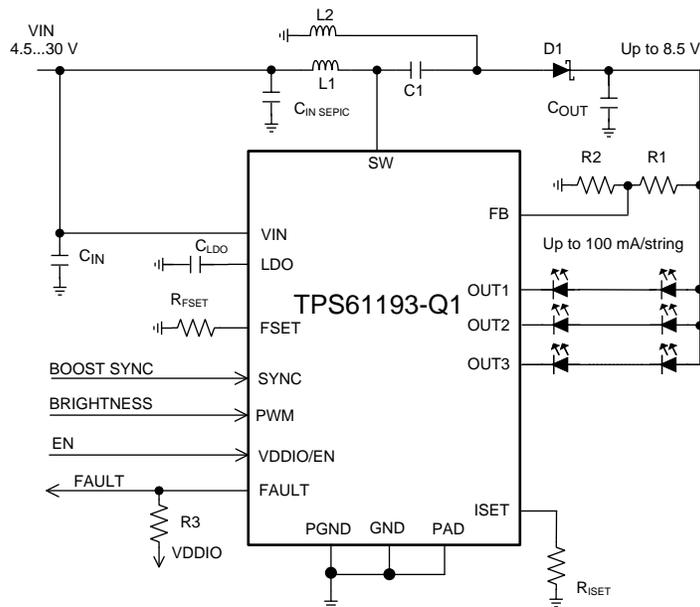


Figure 25. SEPIC Mode, 3 Strings, 100 mA/String Configuration

9.2.2.1 Design Requirements

DESIGN PARAMETER	VALUE
V_{IN} voltage range	4.5 V – 30 V
LED string	3P2S LEDs (7.2 V)
LED string current	100 mA
Maximum output voltage	10 V
SEPIC switching frequency	2.2 MHz
External sync for SEPIC	used
Spread spectrum	Internal spread spectrum disabled (external sync used)
L1, L2	10 μ H
C_{IN}	10 μ F 50 V
$C_{IN\ SEPIC}$	2 \times 10- μ F, 50-V ceramic + 33 μ F 50-V electrolytic
C1	10- μ F 50-V ceramic
C_{OUT}	2 \times 10- μ F, 50-V ceramic + 33 μ F 50-V electrolytic
C_{LDO}	1 μ F, 10 V
R_{ISET}	24 k Ω
R_{FSET}	24 k Ω
R1	184 k Ω
R2	130 k Ω
R3	10 k Ω

9.2.2.2 Detailed Design Procedure

In SEPIC mode the maximum voltage at the SW pin is equal to the sum of the input voltage and the output voltage. Because of this, the maximum sum of input and output voltage must be limited below 50 V. See [Detailed Design Procedure](#) for general external component guidelines. Main differences of SEPIC compared to boost are described below.

Power Stage Designer™ Tool can be used for modeling SEPIC behavior: <http://www.ti.com/tool/powerstage-designer>. For detailed explanation on SEPIC see Texas Instruments Analog Applications Journal [Designing DC/DC Converters Based on SEPIC Topology](#).

9.2.2.2.1 Inductor

In SEPIC mode, currents flowing through the coupled inductors or the two separate inductors L1 and L2 are the input current and output current, respectively. Values can be calculated using *Power Stage Designer™ Tool* or using equations in [Designing DC/DC Converters Based on SEPIC Topology](#).

9.2.2.2.2 Diode

In SEPIC mode diode peak current is equal to the sum of input and output currents. Diode rating for peak repetitive current should be greater than SW pin current limit (up to 3 A for transients) to ensure reliable operation in boost mode. Average current rating should be greater than the maximum output current. Diode voltage rating must be higher than sum of input and output voltages.

9.2.2.2.3 Capacitor C1

Ti recommends a ceramic capacitor with low ESR. Diode voltage rating must be higher than maximum input voltage.

9.2.2.3 Application Curves

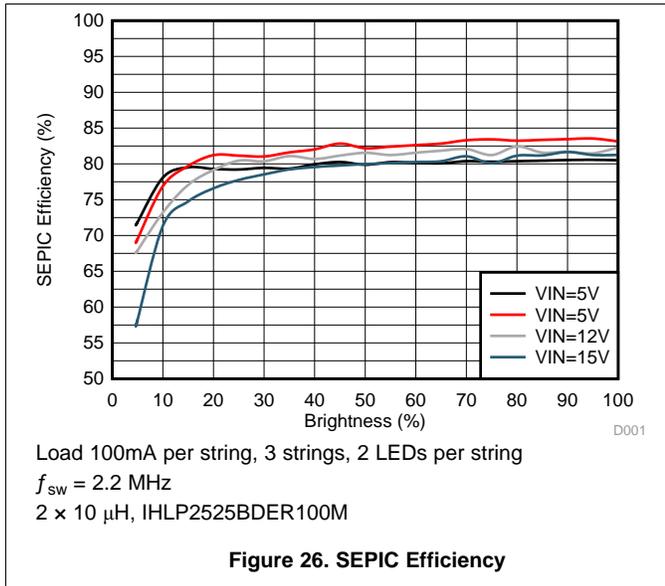


Figure 26. SEPIC Efficiency

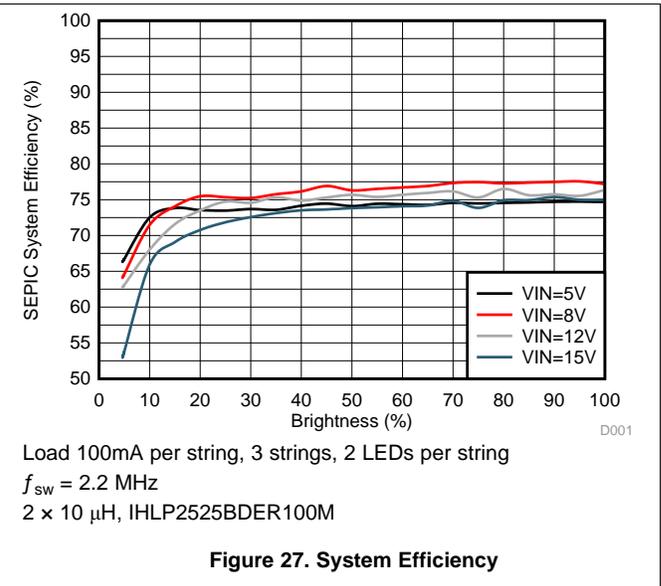


Figure 27. System Efficiency

10 Power Supply Recommendations

The device is designed to operate from an automotive battery. Device should be protected from reversal voltage and voltage dump over 50 V. The resistance of the input supply rail must be low enough so that the input current transient does not cause too high drop at TPS61193-Q1 VIN pin. If the input supply is connected by using long wires additional bulk capacitance may be required in addition to the ceramic bypass capacitors in the V_{IN} line.

11 Layout

11.1 Layout Guidelines

Figure 28 is a layout recommendation for TPS61193-Q1 used to demonstrate the principles of a good layout. This layout can be adapted to the actual application layout if or where possible. It is important that all boost components are close to the chip, and the high current traces must be wide enough. By placing boost components on one side of the chip it is easy to keep the ground plane intact below the high current paths. This way other chip pins can be routed more easily without splitting the ground plane. Bypass LDO capacitor must as close as possible to the device.

Here are some main points to help the PCB layout work:

- Current loops need to be minimized:
 - For low frequency the minimal current loop can be achieved by placing the boost components as close as possible to the SW and PGND pins. Input and output capacitor grounds must be close to each other to minimize current loop size.
 - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High-frequency return currents find a route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the *positive* current route in the ground plane, if the ground plane is intact under the route.
- The GND plane must be intact under the high current boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
- Current loops when the boost switch is conducting and not conducting must be on the same direction in optimal case.
- Inductors must be placed so that the current flows in the same direction as in the current loops. Rotating inductor 180° changes current direction.
- Use separate power and noise-free grounds. Power ground is used for boost converter return current and noise-free ground for more sensitive signals, such as LDO bypass capacitor grounding as well as grounding the GND pin of the device.
- Boost output feedback voltage to LEDs must be taken out *after* the output capacitors, not straight from the diode cathode.
- Place LDO 1- μ F bypass capacitor as close as possible to the LDO pin.
- Input and output capacitors require strong grounding (wide traces, many vias to GND plane).
- If two output capacitors are used they must have symmetrical layout to get both capacitors working ideally.
- Output ceramic capacitors have a DC-bias effect. If the output capacitance is too low, it can cause boost to become unstable on some loads, and this increases EMI. DC-bias characteristics should be obtained from the component manufacturer; they are not taken into account on component tolerance. TI recommends X5R/X7R capacitors.

11.2 Layout Example

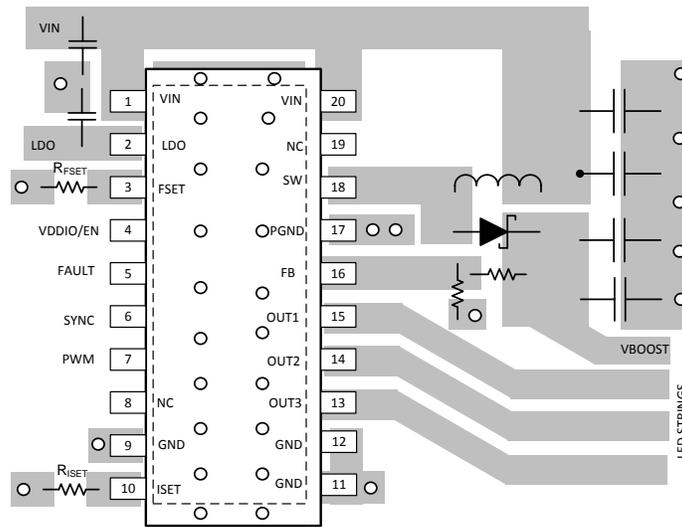


Figure 28. TPS61193-Q1 Boost Layout

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

Power Stage Designer™ 工具可用于升压和 SEPIC 模式: <http://www.ti.com.cn/tool/cn/powerstage-designer>

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档:

- 《使用 [TPS61193EVM](#) 和 [TPS61193-Q1EVM](#) 评估模块》
- 《[PowerPAD™](#) 散热增强型封装》
- 《了解开关模式电源中的升压功率级》
- 《基于 [SEPIC](#) 拓扑设计 [DC/DC](#) 转换器》

12.3 接收文档更新通知

要接收文档更新通知, 请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的 [通知我](#) 进行注册, 即可收到任意产品信息更改每周摘要。有关更改的详细信息, 请查看任意已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点; 请参阅 TI 的 [《使用条款》](#)。

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设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

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All other trademarks are the property of their respective owners.

12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时, 我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本, 请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61193PWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	61193Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

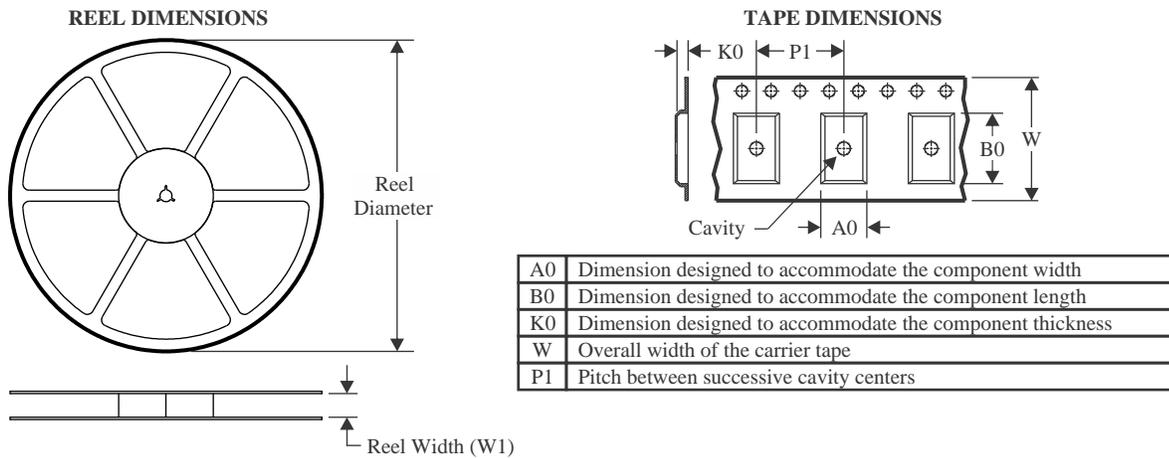
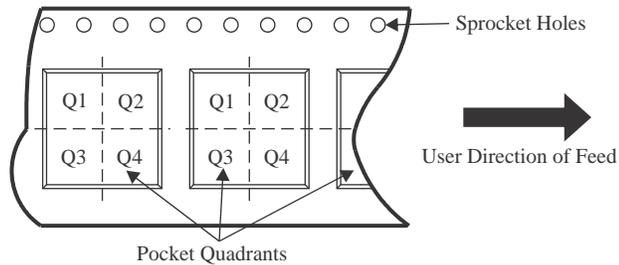
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

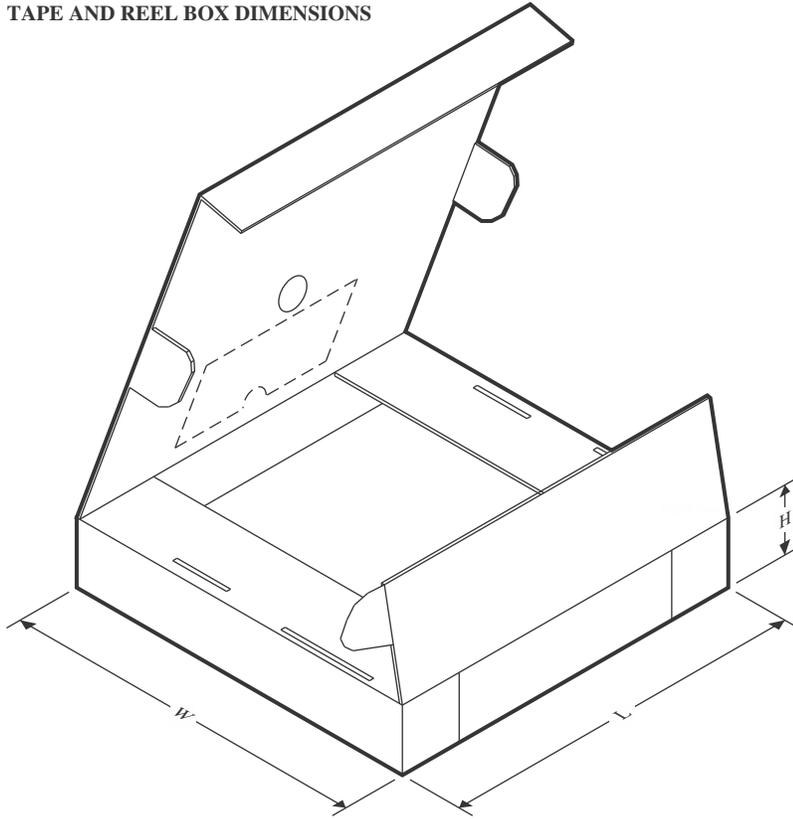
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61193PWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS61193PWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61193PWPRQ1	HTSSOP	PWP	20	2000	356.0	356.0	35.0
TPS61193PWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

THERMAL PAD MECHANICAL DATA

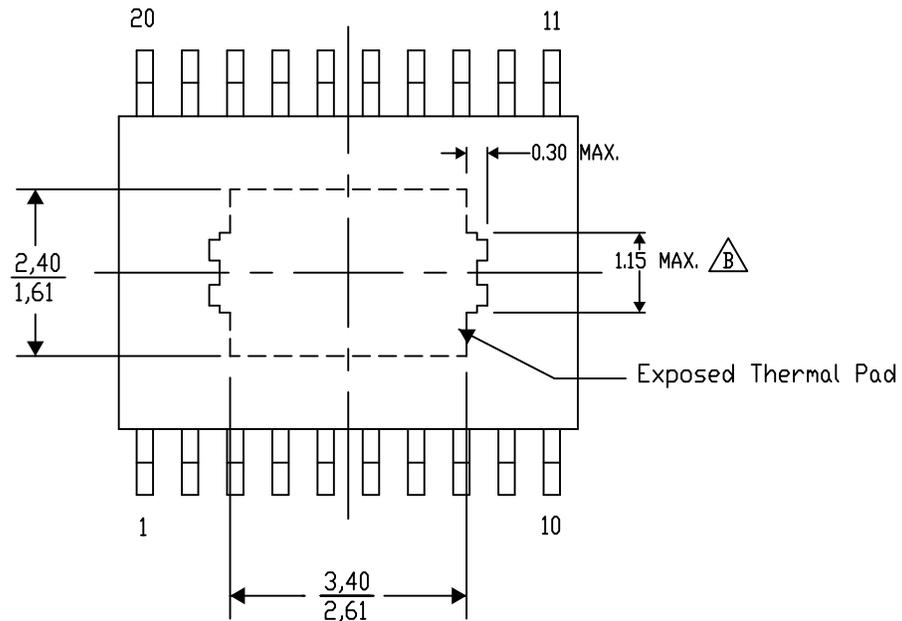
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-15/AO 01/16

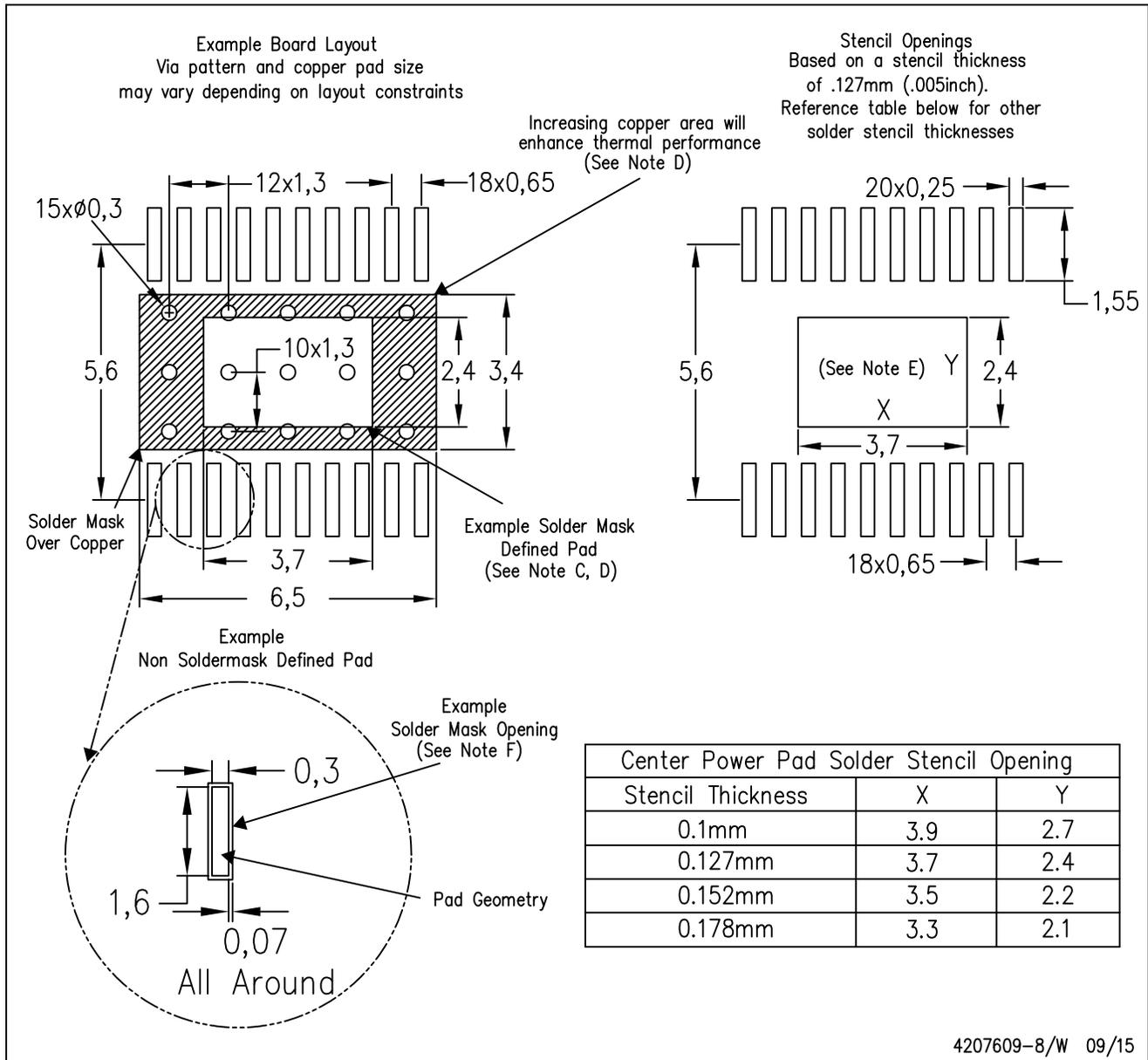
NOTE: A. All linear dimensions are in millimeters

$\triangle B$ Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20)

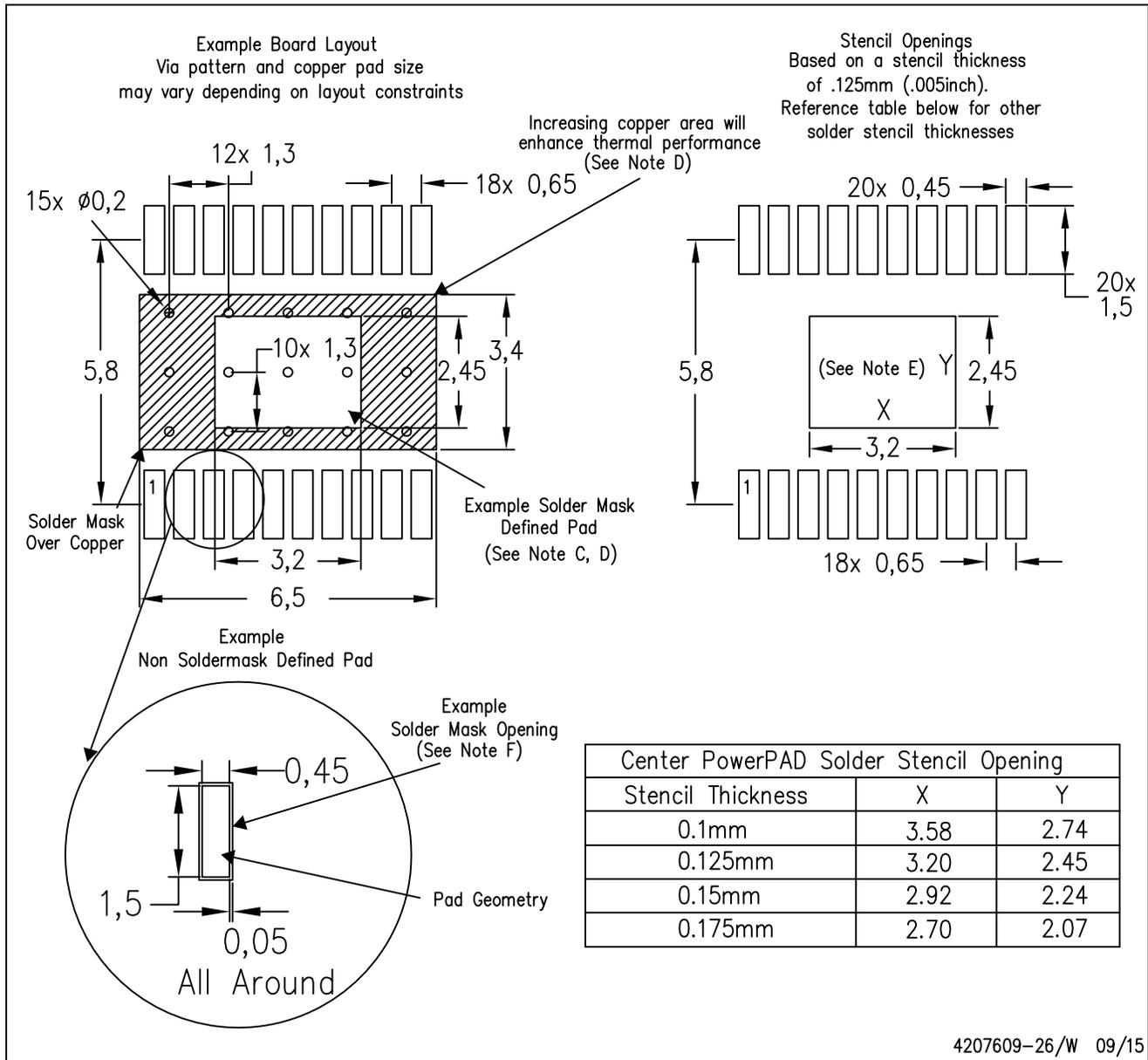
PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



4207609-26/W 09/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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