

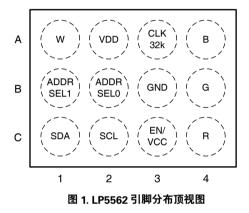
使用说明书 ZHCA653—2016年4月

LP5562 中间引脚的布线

Jussi Tikkanen

摘要

LP5562采用12焊锡凸点芯片尺寸球栅阵列 (DSBGA) 封装,间距0.4mm。这对于成本敏感型应用会是一个限制因素,因为中间焊锡凸点的单独布线需要高密度互连 (HDI) 印刷电路板 (PCB) 技术,而这会增加 PCB 生产过程的成本。



然而,在大多数应用中,可以通过其它焊盘来对中间引脚进行布线,从而避免了使用微导孔。这份使用说明书描述 了不同配置和示例布局布线。



更新 DLP LightCrafter 软件

1 这份报告中所使用的 LP5562 引脚概述

1.1 ADDR0 和 ADDR1

ADDR0 和 ADDR1 引脚被用来选择 LP5562 I2C ID。表 1 中列出了 7 位格式组合,其中没有 R/W 位。ADDR 引脚 必须与接地相连,或接至正电源(VDD 或 EN/VCC)。

表 1. I²C ID

ADDR0	ADDR1	I ² C ID (7-bit)	
0	0	30h	
1	0	31h	
0	1	32h	
1	1	33h	

1.2 CLK 32k

CLK_32k 是为 LED 引擎提供外部 32kHz 时钟的外部时钟引脚。这个引脚可被用来使多个 LP5562 器件同步,并且 减少待机模式功耗。LP5562 还有一个可以使用的内部 32kHz 振荡器,不过会将功耗典型值增加 0.24mA。如果这 个引脚未被使用,它必须被接地,以避免浮置输入。

1.3 LED 驱动器引脚 W, R, G和 B

LED 驱动器引脚 W, R, G和 B 被内部连接至灌电流(或低侧)类型 LED 驱动器。这样可以在不使用驱动器引脚 时将其接地。

1.4 VDD 和 GND

VDD 和 GND 引脚是器件的正电源引脚和接地引脚。始终需要用到这些引脚,并且这份报告中的大多数布线示例都是基于不同的 GND 引脚布线拓扑。TI 建议在这些引脚上使用一个去耦合电容器。

Two-Layer Applications With an External Clock

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2 具有一个外部时钟的 2 层应用

图 2、图 3、图 4 和图 5 显示了在一个系统中实现一个 2 层布局布线的不同方法;这个系统使用主机提供的外部时钟。 在图 3、图 4 和图 5 中,LED 驱动器引脚 G 被用来为接地布线。如果只使用 3 个 LED 驱动器,比如说,使用的是 一个 RGB LED 的话,这是可以实现的。

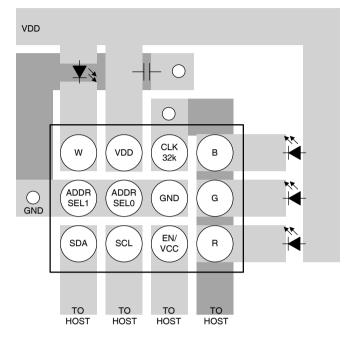


图 2. 外部时钟, I²C ID = 30h

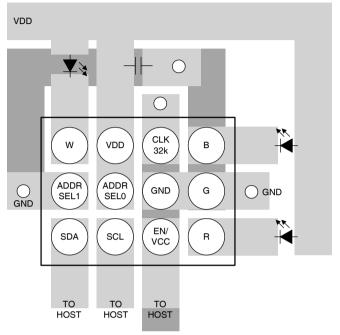
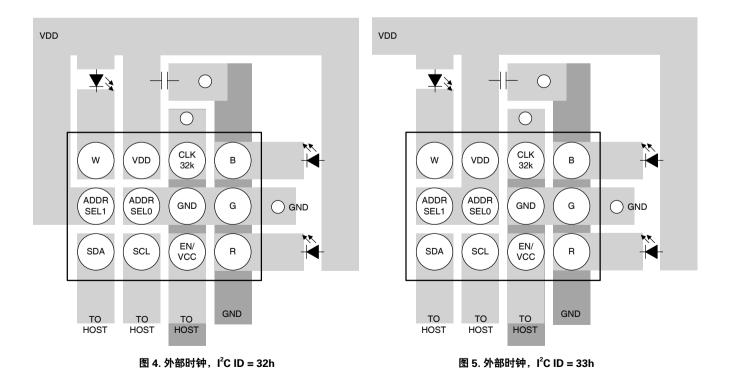


图 3. 外部时钟,I²C ID = 31h





Two-Layer Applications Without an External Clock

['] 使外部时钟引脚接地可以在不使用外部时钟功能的系统中通过 CLK_32k 引脚进行接地布线。图 6、图 7、图 8 和 图 9 显示的是针对不同 I2C ID 的 2 层电路板布线。

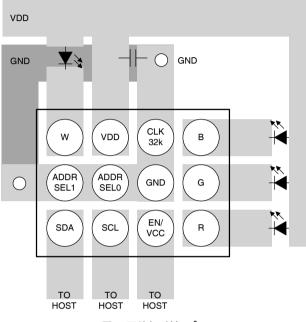


图 6. 无外部时钟, I²C ID = 30h

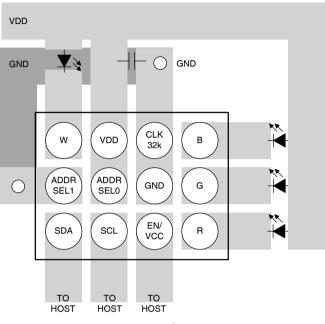
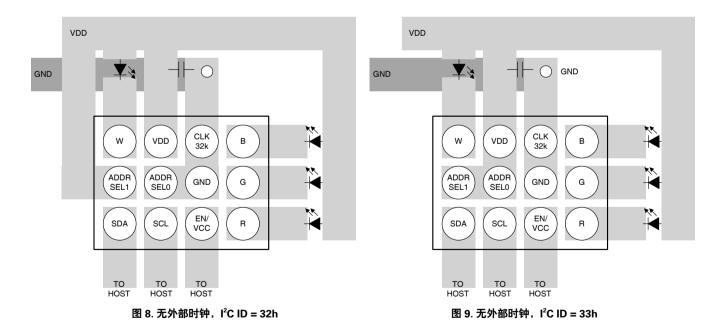


图 7. 无外部时钟,l²C ID = 31h

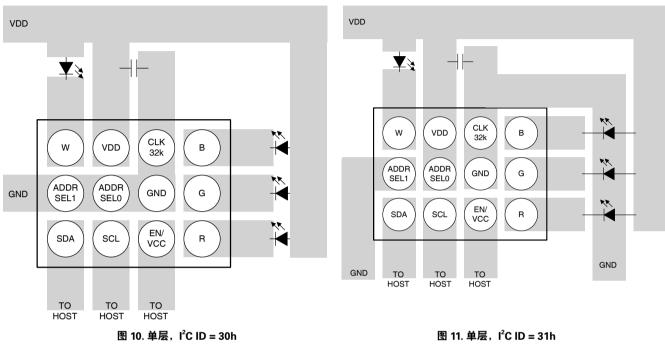


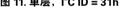
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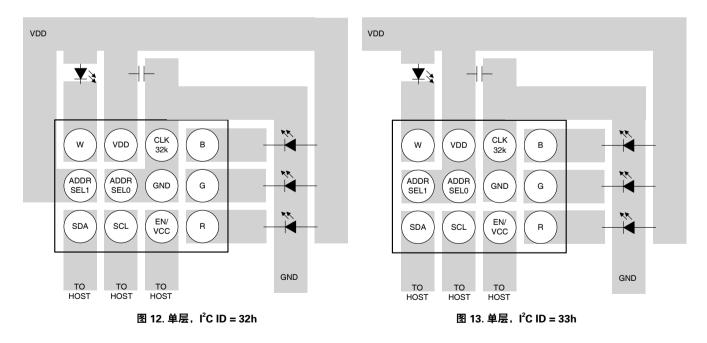
Single-Layer Applications Without an External Clock

4 无外部时钟的单层应用

在某些应用中,布线层的数量受到限制,只有一层 PCB。图 10、图 11、图 12 和图 13 显示了只使用一层对 ADDR 引脚进行布线的示例。它们全都基于之前没有外部时钟的示例,这是因为这些示例可以通过 CLK 32k 引脚 实现接地布线。









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Summary

5 总结

采用 12 焊锡凸点 DSBGA 封装的 LP5562 也适用于那些低成本电路板,这些电路板在应用中对引脚用法的限制很小。 由于没有外部时钟,还有可能实现 LP5562 的单层走线。

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- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
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