# Design Guide: TIDA-010240 Scalable Multi-Pack Smart Battery Charger Reference Design

# TEXAS INSTRUMENTS

## Description

This reference design is a smart high-efficiency charger design for dual smart battery packs of up to 100 Watt hours (Wh) implemented as 1S-5S Lithiumion (Li-ion) batteries in a parallel configuration. To achieve this an onboard MCU manages the communication and safety features needed for the charging system to interface with a battery pack designed to the Smart Battery Data Specification Revision 1.1 (SBD 1.1). This communication allows the MCU to initialize two independent battery charger ICs to the correct charging parameters, as well as inhibit charging when the batteries are outside of safe specifications. This design also demonstrates a highefficiency system power MUX for selecting between the input adapter and efficient discharge of the two smart batteries simultaneously. These features make this reference design highly applicable for portable medical devices, such as oxygen concentrators.

### Resources

TIDA-010240 BQ25731 LM7480-Q1, LM74700-Q1 MSP430FR2475, PCA9546A Design Folder Product Folder Product Folder Product Folder



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#### Features

- Provides a complete drop-in battery charging system for charging and communication with two smart Lithium-Ion batteries
- Supports 1S–5S packs with charge currents of up to 16-A per battery
- Onboard MCU for charge control and upstream communication with system host
- Onboard MCU communicates with smart battery gauges to read charging information and monitor alerts

### Applications

- Oxygen concentrator
- CPAP machine
- Multiparameter patient monitor
- Dialysis machine



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# **1** System Description

All portable equipment carried in aircrafts – including life-critical medical equipment such as portable ventilators, electrocardiogram devices (ECGs), and continuous positive-airway-pressure (CPAP) machines – are subjected to safety restrictions implemented by the Transportation Security Administration (TSA). Lithium batteries with more than 100 watt-hours (Wh) are generally not permitted in carry-on luggage, and any exceptions to this rule lie at the discretion of airlines and require prior approval. This disruption is not ideal for passengers who require these devices out of medical necessity. With the capabilities of Li-ion battery charging technology today, medical instrument manufacturers can alleviate this patient burden. To satisfy travel restrictions while also doubling the backup time of the equipment, *two* 100-Wh batteries can be implemented in the system design. This configuration will also require fewer spare batteries, increasing convenience for the end user during travel. This design guide details the implementation of two BQ25731 chargers managed by an onboard MCU to achieve these requirements for airline travel.

# 2 System Overview

## 2.1 Block Diagram

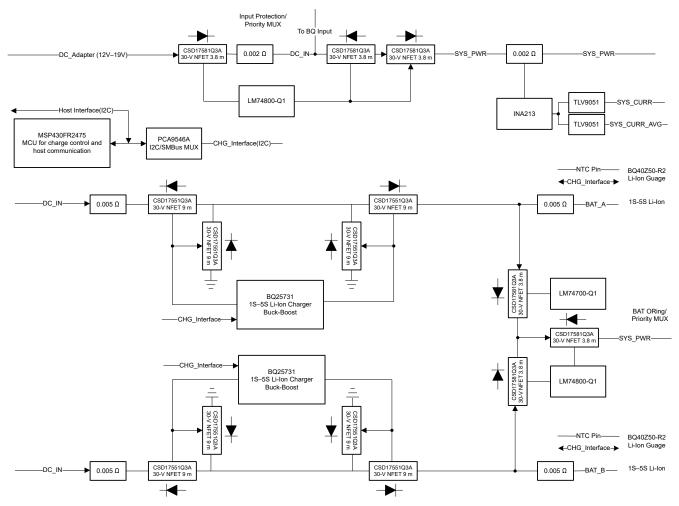


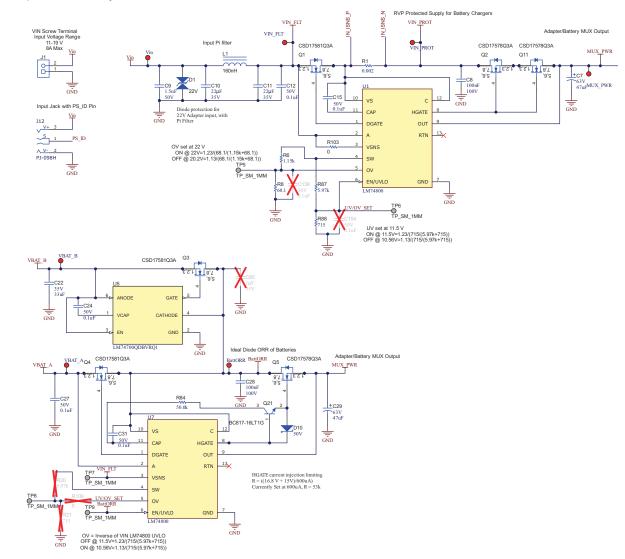
Figure 2-1. TIDA-010240 Block Diagram



#### 2.2 Design Considerations

#### 2.2.1 Power Multiplexing Circuit Design Parameters

Figure 2-2 illustrates the input and battery MUX circuit schematic.







#### 2.2.2 Input Connections and Filter

The reference design board includes a screw terminal (J1) for input connections to a power supply. This board was tested with supplies ranging from 12 V to 19 V, but can function with inputs of 11 V to 22 V. The design also includes a barrel jack connector (J12) for easy connection to existing adapters. There is also a common PI filter at the input of this board for EMI filtering.

Calculate the corner frequency for a PI filter using Equation 1.

$$F_{\mathcal{C}} = \frac{1}{2\pi \times \sqrt{LC}}$$

(1)

In this case, L1 = 160 nH and C10, C11 = 22 µF, resulting in a corner frequency of about 85 kHz.

#### 2.2.3 Reverse Polarity Protection

For reverse polarity protection (RVP) the LM74800 (U1) monitors the voltage across Q1. When the reverse voltage across Q1, monitored with the A and C pins, exceeds –4.5 mV, the device turns off Q1 using the DGATE pin. This circuit acts a high-efficiency replacement for a Schottky diode.

#### 2.2.4 Battery Charger Input

After the reverse polarity protection, a 2-m $\Omega$  sense resistor is added to monitor the overall system input current. After this sense resistor, a VIN\_PROT rail is defined. The VIN\_PROT rail acts as an *always on* supply from the input with reverse polarity protection. This rail directly powers the BQ25731 charger devices.

#### 2.2.5 Battery Ideal Diode-OR

To discharge the two independent batteries in the design, an ideal diode-ORing circuit is used. In this circuit, Q3 and Q4 are driven by U5 and U7 to regulate the FET forward voltage drop to 20 mV. This allows for the efficient discharge of both batteries at the same time, while also preventing current from traveling from one battery to the other. This circuit also allows for passive battery pack voltage balancing to occur in the system by drawing more current from the battery with a higher voltage. Equation 2 shows an example calculation of battery discharge current based on voltage and equivalent series resistance (ESR). For this example, it is assumed that BAT\_A is at 16.8 V and has an ESR of 50 m $\Omega$ , BAT\_B is at 16.6 V and also has an ESR of 50 m $\Omega$ , and the system is drawing 8 A.

 $I_{LOAD} = I_{BATA} + I_{BATB}$ 

 $V_{Load} = V_{BATA} - V_{Af} - \left(I_{BATA} \times ESR_{BATA}\right)$ 

 $V_{Load} = V_{BATB} - V_{Bf} - (I_{BATB} \times ESR_{BATB})$ 

 $V_{BATA} - V_{Af} - (I_{BATA} \times ESR_{BATA}) = V_{BATB} - V_{Bf} - (I_{BATB} \times ESR_{BATB})$ 

 $16.8 V - 20 mV - (I_{BATA} \times 50 m\Omega) = 16.7 V - 20 mV - (I_{BATB} \times 50 m\Omega)$ 

 $I_{BATA} = I_{BATB} + 2.0$ , where  $I_{BATB} \ge 0$ 

In this example, BAT\_A supplies 2 A more current that BAT\_B until the higher current discharge causes the voltage differential between the batteries to be reduced.

#### 2.2.6 Input and Battery Switchover Mechanics

This design provides an input and battery MUX that prioritizes the input adapter in all cases where the adapter voltage exceeds the UVLO setting of U1. When the UVLO threshold is triggered, the input adapter is disconnected from the system and the batteries are connected to power the system load. This prevents the batteries from discharging while an input adapter is present.

This threshold is set by the resistor divider consisting of R87 and R88. For U1 (input adapter connection) the UVLO thresholds are 1.13 V falling for turn off, and 1.23 V rising for turn on. For U7 (battery connection) the OV pin is connected to the same divider and the thresholds operate inversely. These thresholds are 1.13 V falling for

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(2)

(3)

turn on, and 1.23 V rising for turn off. In the schematic this voltage is connected to the net labeled UV/OV\_SET. In the current schematic the switchover from input adapter to battery is triggered when VIN reaches 10.56 V and the switchover from battery to input adapter is triggered when VIN reaches 11.5 V.

Equation 3 shows an example of the resistor divider calculation:

Battery to Input Adapter Transition =  $\frac{1.23 V}{\frac{R88}{R87 + R88}}$ 

Input Adapter to Battery Transition =  $\frac{1.13 V}{\frac{R88}{R87 + R88}}$ 

 $R87 = 5.97 \ k\Omega, \ R88 = 715 \ \Omega$ 

 $Battery \ to \ Input \ Adapter \ Transition = \frac{1.23 \ V}{\frac{715 \ \Omega}{5.97 \ k\Omega + 715 \ \Omega}} = 11.5 \ V$ 

Input Adapter to Battery Transition =  $\frac{1.13 V}{\frac{715 \Omega}{5.97 k\Omega + 715 \Omega}} = 10.56 V$ 

#### 2.2.7 LM74800 (U1) HGATE

The HGATE design for U1 includes two back-to-back NFETs (Q2 and Q11). Q11 was added to the design to prevent any current from flowing from the batteries to the VIN\_FLT rail when the batteries are connected to the system. When only Q2 is placed and (V\_SYS > VIN\_PROT + 0.8 V) a current is conducted through the body diode of Q2. This allows a current loop to form between the output of both BQ25731 devices and the input of the BQ25731 devices.

#### 2.2.8 Battery LM74800 HGATE

Adjustments were made to the HGATE design of U7 to reduce the turn on time of Q5. This reduction is made by increasing the gate current delivered to Q5 from 55  $\mu$ A to 600  $\mu$ A. To increase the HGATE current that can be delivered by U7, a circuit including D10, Q21, and R84 was added. This circuit amplifies the source current of the HGATE pin by driving an NPN transistor (Q21) that is connected between the charge pump output (CAP, U7 pin 11) and the gate of Q5. A series resistance (R84) is also added to this path to limit the current injection. Diode (D10) is also added between the gate of Q5 and HGATE (U7 pin 8) to allow the HGATE pin to sink current when turning the FET off. Equation 4 provides an example calculation for the HGATE current injection limit. The charge pump of the LM74800 provides an output of VS + 13.2 V. In this case VS is connected to the output of the batteries and is assumed to be 16.8 V. The charge pump can supply a maximum current of 2.4 mA. The current design has the injection current set to be 600  $\mu$ A, but this current can be increased by reducing R84.

Example 1.

 $R84 = \frac{V_{VS} + V_{CHGPUMP}}{I_{gate}}$ 

Example 2.

$$R84 = \frac{16.8 \, V + 13.2 \, V}{600 \, \mu A} = 50.0 \, k\Omega$$

$$R84 = \frac{16.8 \, V + 13.2 \, V}{2.0 \, mA} = 15.0 \, k\Omega$$

(4)



#### 2.2.9 BQ25731 Design Considerations

Figure 2-3 illustrates the BQ25731 component selection.

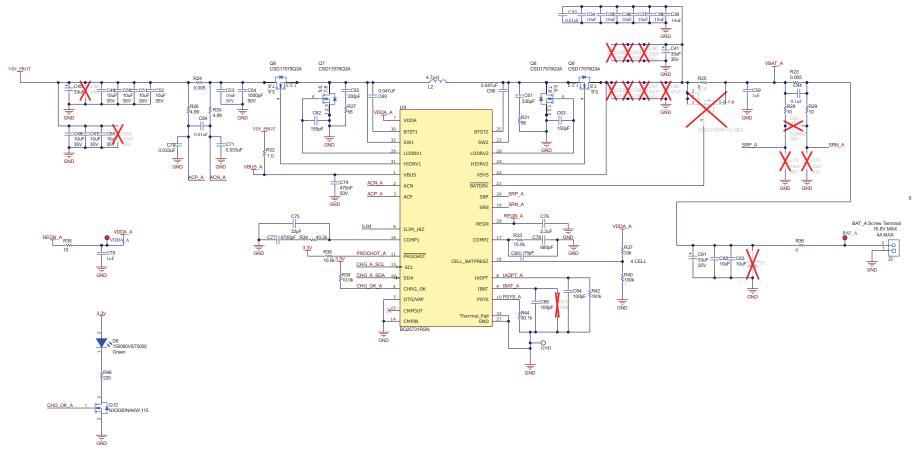


Figure 2-3. BQ25731 Component Selection

(5)

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#### 2.2.10 BQ25731 Component Selection

Components for the BQ25731 Charge Controllers were selected to be as flexible as possible for this reference design. For a more detailed guide on component selection specific to your design, see the *Detailed Design Procedure* section in the *BQ25731 I2C 1- to 5-Cell Buck-Boost Battery Charge Controller with USB-C PD 3.0 OTG Output* data sheet.

#### 2.2.11 ILIM Circuit

For this design a circuit was added to limit the system current to 8 A. This is most impactful when the device is being used with a 12-V car adapter and can pull the battery voltage below the input threshold of the system. This circuit includes the INA213B to amplify the current across a 2-m $\Omega$  sense resistor. This INA213B has a gain of 50 V/V so an input of 8 A results in an 800-mV output.

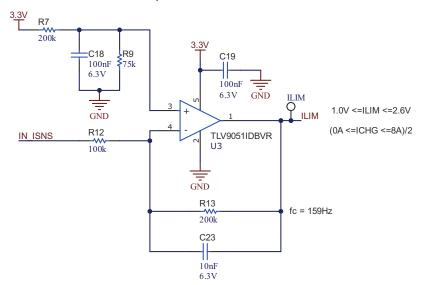


Figure 2-4. Current-Limit Circuit

To convert this signal into a usable voltage for the ILIM pin of the BQ25731 devices, an op amp configured as a difference amplifier was used. The voltage on the BQ25731 ILIM pin is converted to charge current based on Equation 5.

$$V(ILIM_HIZ) = 1V + 40 \times IDPM \times Rac$$

where

- · IDPM is the target input current limit
- Rac is the 5- or 10-m $\Omega$  resistor chosen for the BQ25731

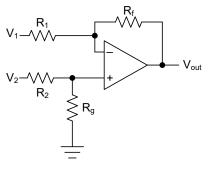


Figure 2-5. Difference Amplifier

For the difference amplifier when:

$$V_{out} = V_2 - V_1$$

where

• 
$$R_1 = R_2 = R_f = R_g$$
,  $V_{out} = V_2 - V_1$ 

To correctly set the BQ25731 charge current, set the ILIM pin at 1.0 V with 8 A of system current and 1.8 V with 0-A system current. Limit the charge current for each of the 2 charger devices to between 0 A and 4 A.

Set V2 at 1.8 V in this case. With V2 at 1.8 V, the voltage at the amplifiers positive input is equal to V2/2, which is 0.9 V. This voltage then needs to be created with the system 3.3-V rail and a resistor divider to match the calculated set point. This was implemented with a R7 and R9 as shown in the schematic above.

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(6)



#### 2.2.12 MCU and I2C Bus Design Considerations

Figure 2-6 shows the MSP430FR2475, TPS62177, PCA9546A MCU and I<sup>2</sup>C bus schematic.

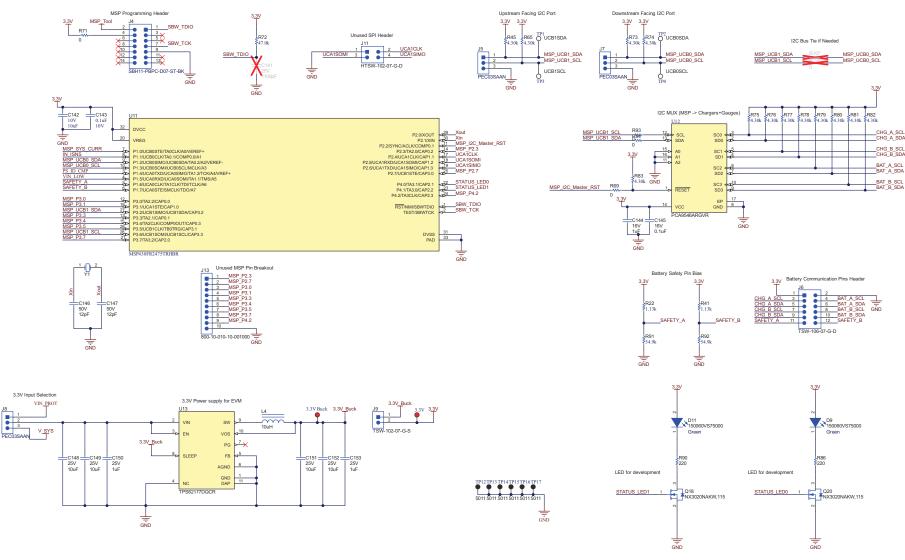


Figure 2-6. MSP430FR2475, TPS62177, PCA9546A MCU and I<sup>2</sup>C Bus Schematic



#### 2.2.13 MSP430FR2475

The MSP430FR2475 was chosen for this application because of its low cost, two eUSCI\_B channels supporting I<sup>2</sup>C, eight 12-bit ADC channels, and small footprint. The two eUSCI\_B I<sup>2</sup>C channels allow for two independent interfaces, one between the MCU and Host controller, and one between the MCU and downstream devices such as the battery chargers and gauges included in the smart battery packs.

#### 2.2.14 I<sup>2</sup>C Bus Overview

The I<sup>2</sup>C bus for this design was broken into two separate communication channels. One of these channels uses the UCB0 peripheral to communicate with an upstream host. This allows for data and control registers to be maintained in the MSP430 that can be read from or written to by the system host. This peripheral also allows for a hardware I<sup>2</sup>C address to be assigned in the firmware, providing a system that can be configured to communicate directly with a host that is using existing hardware and firmware.

The other I<sup>2</sup>C channel using UCB1 acts as a downstream facing port to control the charging system for this design. The PCA9546A I<sup>2</sup>C MUX is used to interface directly with multiple downstream devices using the same address. This uses all four channels of the PCA9546A to communicate with two BQ25731 devices at address 0x6B, and two gauges at address 0x16, as is outlined by the *Smart Battery Data Specification 1.1*.

#### 2.2.15 MSP430 Connectors

This reference design includes an MSP Programming header that is compatible with TI's MSPFET device for programming and debugging. Headers are also included for UCA1(J11), UCB0(J5), and UCB1(J7) to enable direct connection to the communication interfaces used by this design. Header J6 has also been added to allow for connection of the smart battery communication and safety signal pins.

#### 2.2.16 MSP430 Power Supply

The onboard MSP430 is powered by the TPS62177 device , a high-efficiency synchronous step-down DC/DC converter. The input of this converter is selected by J8, and can either be powered by V\_SYS or VIN\_PROT. This also allows for the converter to be easily supplied by an external source by connecting it directly to pin 2 of J8. The output of this converter is 3.3 V and is used to supply the MSP430, op amps, and comparators in the design. The device also has a sleep pin that is not currently being used, but can be enabled in later designs.

#### 2.2.17 Sensing Circuits

This reference design includes multiple sensing circuits that enable the MCU to monitor multiple items in the system. This includes input current and voltage, system current and voltage, input voltage comparator, and a Power Supply ID (PS\_ID) comparator.



#### 2.2.18 Current Sensing

Two INA213B devices are used for current sensing in this design. The INA213 is a current-shunt monitor design for both high- and low-side current measurements. Both of these devices are supplied by 3.3 V, referenced to ground, and provide a gain of 50 V/V. U2 measures the current across the 2-m $\Omega$  sense resistor R1, which provides an input current measurement for both the system rail and battery charge currents. U4 measures the current across the 2-m $\Omega$  sense resistor R2, which provides a measurement of the current on the system output rail.

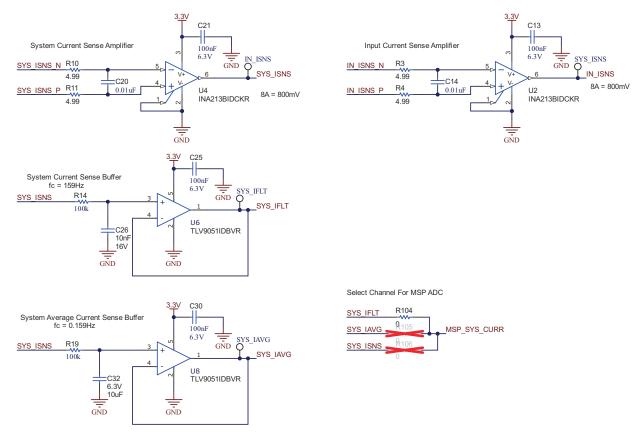


Figure 2-7. Current Sensing Schematic

There are also two current-sense buffers that are used to filter the system current rail. The buffer including U6 includes a low-pass filter with a corner frequency of 159 Hz. This provides the MCU with an accurate measurement of the system current while mitigating high-frequency noise. The buffer including U8 includes a low-pass filter with a corner frequency of 0.159 Hz. This provides the MCU with an average current signal over about 6 seconds.

The MCU only has one ADC pin available for current sensing so a  $0-\Omega$  resistor was added in series with each of these outputs to provide the ability to manually select between which current sense output is delivered to the MCU.

#### 2.2.19 Voltage Sensing

There are three voltage dividers in the system that allow the MCU to monitor V\_SYS, VIN\_FLT, and PS\_ID. The V\_SYS and VIN\_FLT dividers output a scaled voltage based on the input to the dividers. Figure 2-8 shows the scaled voltage. All three of the dividers also include a Schottky barrier diode to provide overvoltage protection to the MCU.

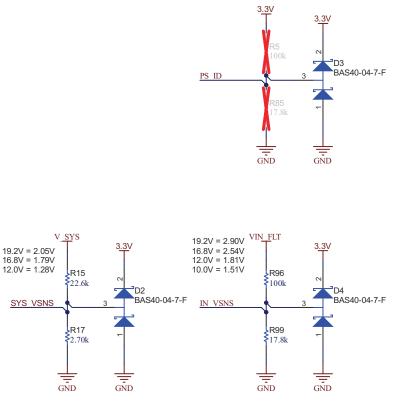


Figure 2-8. Voltage Sensing Schematic

The PS\_ID pin is made available here as well. This type of pin is commonly included in barrel jack input adapters and provides a specific voltage based on the voltage and current capability of the adapter.



#### 2.2.20 Input Comparators

Two comparators are included to monitor VIN\_FLT and PS\_ID. These signals can be used to provide interrupt generation for the MCU when a specific type of adapter has been inserted or if an input adapter voltage threshold has been met. The TLV7031 nano-power, low-voltage comparator is used to provide a small footprint and low power draw while waiting for input events. Because these devices are powered by the battery when no input adapter is present, the ultra-low quiescent current of 315 nA is a key design feature.

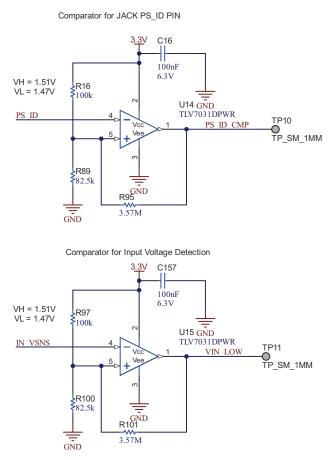


Figure 2-9. Input Capacitor Schematic

The voltage setting and hysteresis for these comparators can be calculated and adjusted according to Equation 7.

$$V_{TH} = V_{CC} \times \frac{R100}{R97 | |R101 + R100}$$
$$V_{TL} = V_{CC} \times \frac{R100 | |R101}{R97 + R100 | |R101}$$
$$V_{TH} = 3.3 V \times \frac{82.5 k\Omega}{100 k\Omega | |3.57 M\Omega + 82.5 k\Omega} = 1.51 V$$
$$V_{TL} = 3.3 V \times \frac{82.5 k\Omega | |3.57 M\Omega}{100 k\Omega + 82.5 k\Omega | |3.57 M\Omega} = 1.47 V$$

(7)

#### 2.2.21 Software Flow Chart

Figure 2-10 illustrates the software flow chart.

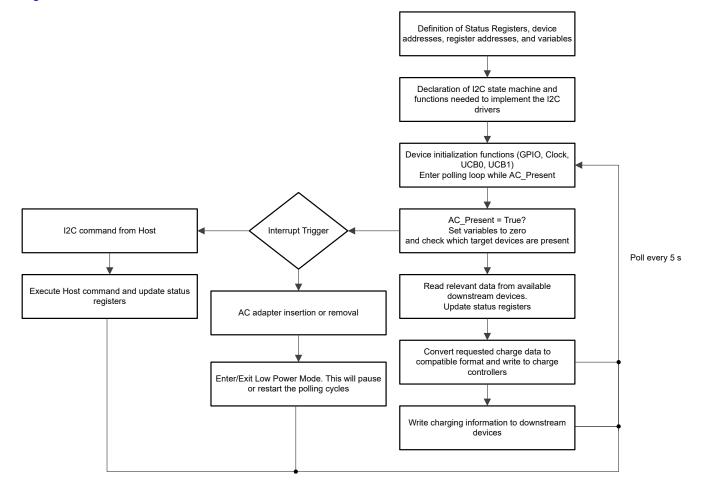


Figure 2-10. Software Flow Chart

#### 2.3 Highlighted Products

#### 2.3.1 BQ25731

The BQ25731 is a synchronous buck-boost battery charge controller to charge a 1- to 5-cell battery from a wide range of input sources including USB adapter, high voltage USB-C Power Delivery (PD) sources, and traditional adapters. It offers a low component count, high efficiency solution for space constrained, 1- to 5-cell battery charging applications. During power up, the charger sets the converter to a buck, boost, or buck-boost configuration based on the input source and battery conditions. The charger seamlessly transits between the buck, boost, and buck-boost operation modes without host control.

#### 2.3.2 LM7480-Q1

The LM7480-Q1 ideal diode controller drives and controls external back to back N-channel MOSFETs to emulate an ideal diode rectifier with power path ON and OFF control and overvoltage protection. The wide input supply of 3 V to 65 V allows protection and control of 12-V and 24-V supply rails. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. With a second MOSFET in the power path the device allows load disconnect (ON and OFF control) and overvoltage protection using HGATE control. The device features an adjustable overvoltage cutoff protection feature.



#### 2.3.3 LM74700-Q1

The LM74700-Q1 is an automotive AEC Q100 qualified ideal diode controller which operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low-loss reverse polarity protection with a 20-mV forward voltage drop. The wide supply input range of 3.2 V to 65 V allows control of many popular DC bus voltages such as 12-V and 24-V battery systems. The device controls the GATE of the MOSFET to regulate the forward voltage drop at 20 mV. The regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. Fast response (< 0.75  $\mu$ s) to Reverse Current Blocking makes the device suitable for systems with output voltage holdup requirements during ISO7637 pulse testing as well as power fail and input micro-short conditions.

#### 2.3.4 MSP430FR2475

The MSP430FR247x microcontrollers (MCUs) are part of the MSP430<sup>™</sup> MCU value line portfolio of ultra-lowpower low-cost devices for sensing and measurement applications. MSP430FR247x MCUs integrate a 12-bit SAR ADC and one comparator. The MSP430FR247x MCUs support an extended temperature range from –40°C up to 105°C, so higher temperature industrial applications can benefit from the FRAM data-logging capabilities of the devices. The TI MSP430 family of low-power microcontrollers consists of devices with different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The MCU features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the MCU to wake up from low-power modes to active mode in less than 10 µs (typical).

#### 2.3.5 PCA9546A

The PCA9546A is a quad bidirectional translating switch controlled via the I<sup>2</sup>C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register. An active-low reset (RESET) input allows the PCA9546A to recover from a situation in which one of the downstream I<sup>2</sup>C buses is stuck in a low state. Pulling RESET low resets the I<sup>2</sup>C state machine and causes all the channels to be deselected, as does the internal power-on reset function. The pass gates of the switches are constructed such that the VCC pin can be used to limit the maximum high voltage, which will be passed by the PCA9546A. This allows the use of different bus voltages on each pair, so that 1.8-, 2.5-, or 3.3-V parts can communicate with 5-V parts without any additional protection. External pullup resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5-V tolerant.



# 3 Hardware, Testing Requirements, and Test Results

The key performances of TIDA-010240 were tested in a TI lab, the equipment used, test processes, and results are described in this section.

Table 3-1 lists the TIDA-010240 board connections.

Table 3-1. TIDA-010240 Board Connections				
Connector	Description			
J1	Input Supply connector (V <sub>IN</sub> )			
J2	Battery A power connector			
J3	Battery B power connector			
J4	MSPFET Programming header			
J5-1	MSP-MUX SCL			
J5-2	MSP-MUX SDA			
J5-3	GND Connection			
J7-1	Host-MSP SDA			
J7-2	Host-MSP SCL			
J7-3	GND Connection			
J6-1	BQ25731 Device A SCL			
J6-2	Battery Pack A SCL			
J6-3	BQ25731 Device A SDA			
J6-4	Battery Pack A SDA			
J6-5	BQ25731 Device B SCL			
J6-6	Battery Pack B SCL			
J6-7	BQ25731 Device B SDA			
J6-8	Battery Pack B SDA			
J6-9	3.3-V Connection			
J6-10	GND Connection			
J8-1	VIN +			
J8-2	3.3-V Buck Converter Supply			
J8-3	VSYS +			
J9-1	3.3-V Buck Converter Output			
J9-2	System 3.3-V Rail			
J9-3	MSPFET 3.3-V pin			
J10	System Output Connector (VSYS)			

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#### 3.1 Hardware Requirements

Table 3-2 shows the equipment used for testing.

Table 3-2. Equipment Used for Testing

Equipment	Rating	Description		
DC Power Supply	12 V to 20 V, 8 A	Power supply representing 19-V wall adapter input		
Electronic Load (E-Load)	160 W	Electronic load used to simulate the system load up to 160 W		
Smart Batteries	Up to 4S, 2P Li-ion	Smart battery packs for charge, discharge and communications testing		
Oscilloscope		Tektronix DPO 2024B		
Multimeter		Agilent 34401A		
Logic Analyzer		Logic analyzer used for communication monitor		
USB2ANY		USB2ANY device used for generating host commands		

# 3.2 Test Setup

Table 3-3 shows the connections to the TIDA-010240 board for testing.

Connector	Description
J1	Connected to DC Power supply (12 V to 20 V)
J2	Battery A + and – connections
J3	Battery B + and – connections
J10	Connected to > 160-W E-Load
J4	MSPFET Connected for software monitoring
J5-1	Logic Analyzer SCL monitoring downstream
J5-2	Logic Analyzer SDA monitoring downstream
J5-3	Logic Analyzer GND Connection
J7-1	Host-MSP SDA connection for USB2ANY
J7-2	Host-MSP SCL connection for USB2ANY
J7-3	GND Connection for USB2ANY
J6-1	BQ25731 Device A SCL
J6-2	Battery Pack A SCL
J6-3	BQ25731 Device A SDA
J6-4	Battery Pack A SDA
J6-5	BQ25731 Device B SCL
J6-6	Battery Pack B SCL
J6-7	BQ25731 Device B SDA
J6-8	Battery Pack B SDA
J8	J8-2 jumper to J8-3. Ties VSYS to 3.3-V buck input
J9	J9-1 jumper to J9-2. Ties 3.3-V buck to 3.3-V system rail

#### Table 3-3. TIDA-010240 Board Connections for Testing



### 3.3 Test Results

This section describes the test procedures used to verify the functionality of this design. Test results for Charge Current Limiting, Battery ORRing, and Adapter or Battery Switchover are shown, and the procedures used during the testing are discussed.

All tests run in this section follow the connections in Table 3-3, unless otherwise stated.

#### 3.3.1 Adaptive Charge Current Limiting

The reference design has an ILIM circuit used for limiting the total input current of the system to 8 A (described in Section 2.2.11). The test detailed in this sections confirms the functionality of this adaptive current limiting circuit.

For this test DMMs are connected in series with the positive terminals of both batteries to measure the charge current of each. The system load current is set using the E-Load in CC mode. The input current is monitored on the DC power supply input. The connected battery pack voltages are approximately 14.5 V. After setup, the board is powered up with the 19-V supply.

Table e H / table e enarge earrent Einning Bata				
Input Current (A)	System Current (A)	Battery A Charge Current (A)	Battery B Charge Current (A)	ILIM Voltage
5.38	0	3.00	2.99	1.54
5.79	1	2.60	2.78	1.46
6.11	2	2.24	2.40	1.34
6.75	4	1.52	1.63	1.26
7.39	6	0.75	0.80	1.13
8.09	8	0.00	0.00	0.99

#### Table 3-4. Adaptive Charge Current Limiting Data

#### 3.3.2 Battery ORing System

This design discharges the batteries through ideal diodes. This results in a discharge current proportional to the battery voltage until the batteries are discharged to an even voltage. Battery A measured 14.429 V and Battery B measured 13.858 V at the beginning of the test. Multimeters were hooked up in series with the positive terminals of the batteries to measure discharge current. The E-Load was set to draw a 5-A constant current from the system rail (the DMMs used for testing were only rated for 3 A each).

System Current (A)	Battery A Discharge Current (A)	Battery A Voltage (V)	Battery B Discharge Current (A)	Battery B Voltage (V)
5	3.11	12.425	1.91	12.407
2	1.33	13.34	0.68	13.28

#### Table 3-5. Battery ORing Data

#### 3.3.3 Circuit Switchover From Adapter to Battery

Texas

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INSTRUMENTS

This test is designed to demonstrate the adapter-to-battery switchover capabilities of the design. The test is run with 19 V on the input supply. The E-Load is then connected to the system rail and draws a constant current of 8 A. The input supply is then removed and the VIN, VSYS, and VBAT rails are monitored for the switchover timings. The test is then repeated while replacing the 19-V input supply with a 13-V supply to mimic a car charging adapter.

In Figure 3-1 through Figure 3-4, VIN is measured by CH1 (Blue), VBAT is measured by CH2 (Red) and, VSYS is measured by CH3 (Green). For these captures all channels are based at 0 V with no offset to better illustrate the switchover mechanism.

Figure 3-1 shows the 19 V to battery switchover with a time division of 200  $\mu$ s. The minimum voltage at VSYS is 9.21 V. The approximate switchover timing is 10  $\mu$ s and the VSYS rail has increased to 12.87 V by 20  $\mu$ s after the switchover event.

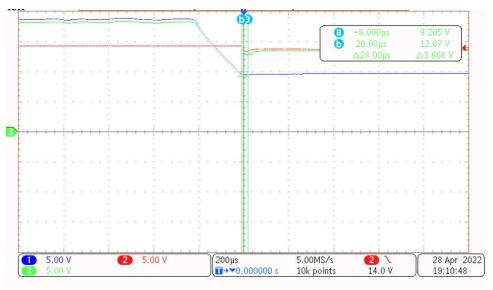


Figure 3-1. 19 V to Battery Switchover 200-µs Time Division

Figure 3-2 shows the 19 V to battery switchover with a time division of 20  $\mu$ s. The minimum voltage at VSYS is 9.28 V. The approximate switchover timing is 10  $\mu$ s and the VSYS rail has increased to 11.82 V by 10  $\mu$ s after the switchover event.

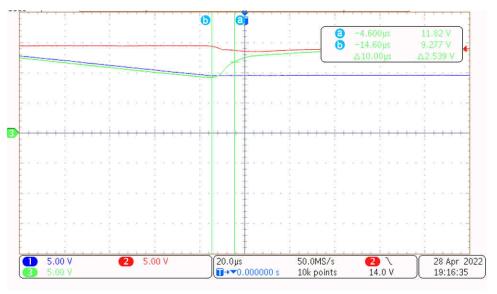


Figure 3-2. 19 V to Battery Switchover 20-µs Time Division



Figure 3-3 shows the 12 V to battery switchover with a time division of 100  $\mu$ s. The minimum voltage at VSYS is 9.12 V. The approximate switchover timing is 10  $\mu$ s and the VSYS rail has increased to 12.73 V by 20  $\mu$ s after the switchover event.

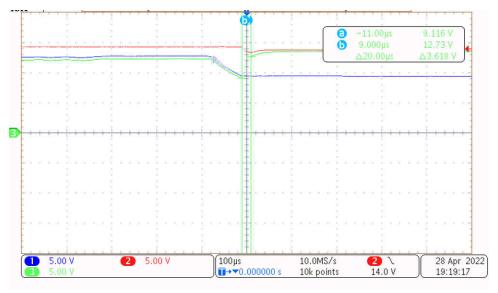


Figure 3-3. 12 V to Battery Switchover 10-µs Time Division

Figure 3-4 shows the 12 V to battery switchover with a time division of 20  $\mu$ s. The minimum voltage at VSYS is 9.31 V. The approximate switchover timing is 10  $\mu$ s and the VSYS rail has increased to 10.63 V by 10  $\mu$ s after the switchover event.

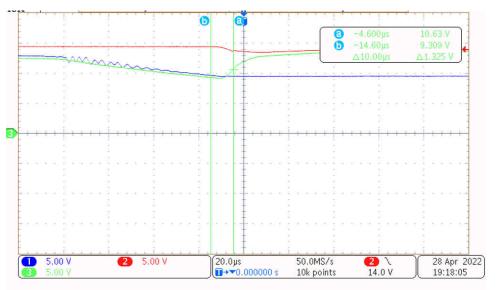


Figure 3-4. 12 V to Battery Switchover 20-µs Time Division



# 4 Design and Documentation Support

#### 4.1 Design Files

#### 4.1.1 Schematics

To download the schematics, see the design files at TIDA-010240.

#### 4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010240.

#### 4.2 Documentation Support

- 1. Texas Instruments, BQ25731 I2C 1- to 5-Cell Buck-Boost Battery Charge Controller with USB-C PD 3.0 OTG Output data sheet
- 2. Texas Instruments, LM7480-Q1 Ideal Diode Controller with Load Dump Protection data sheet
- 3. Texas Instruments, LM74700-Q1 Low IQ Reverse Battery Protection Ideal Diode Controller data sheet
- 4. Texas Instruments, MSP430FR247x Mixed-Signal Microcontrollers data sheet
- 5. Texas Instruments, *PCA9546A Low Voltage 4-Channel I<sup>2</sup>C and SMBus Switch with Reset Function* data sheet

#### 4.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 4.4 Trademarks

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#### **5 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	Changes from Revision * (June 2022) to Revision A (June 2022)			
•	Removed text in the System Overview section	2		

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