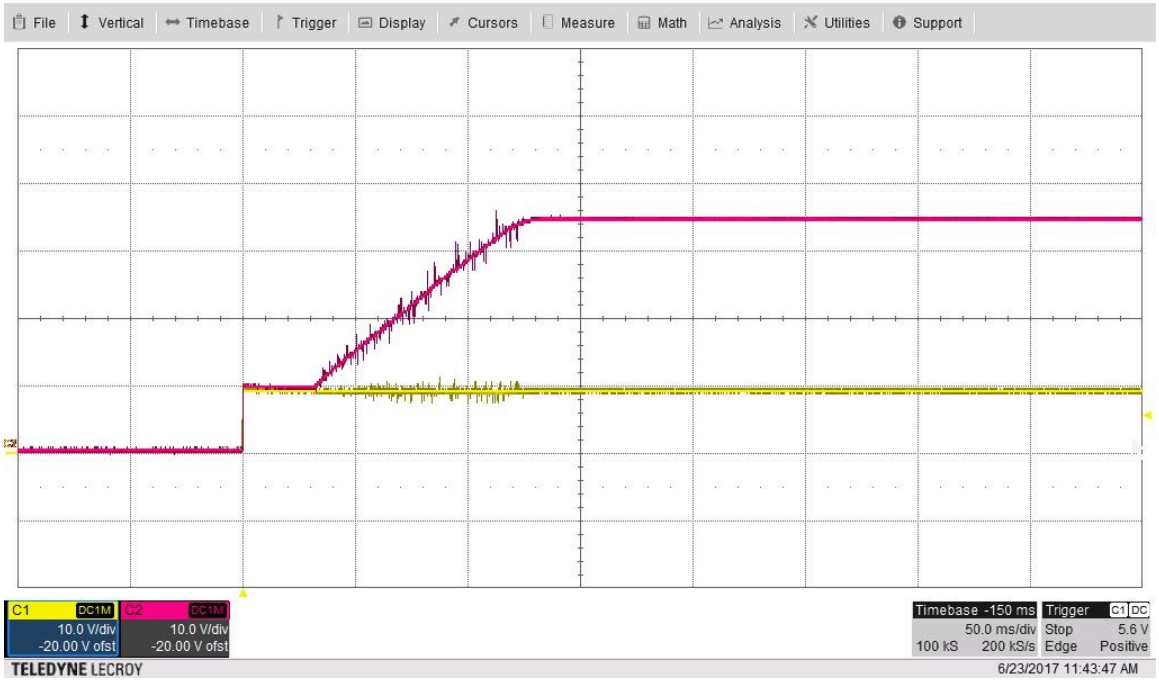
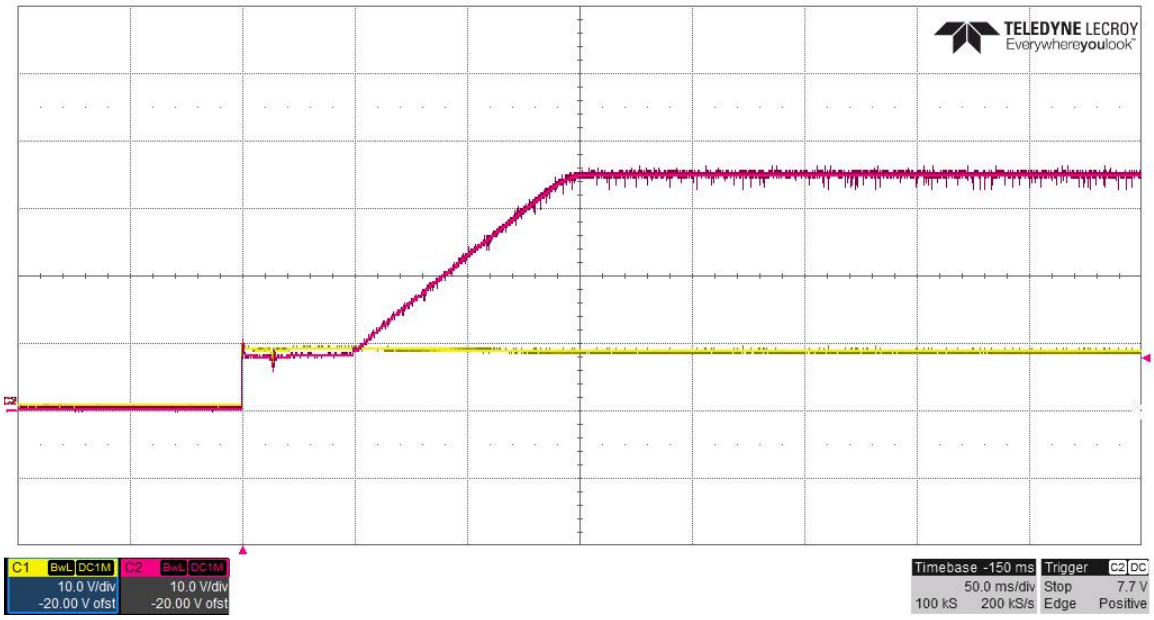
1 Startup

The photo below shows the output voltage startup waveform after the application of 9V in. The 35V output was loaded to 0A. (10V/DIV, 50mS/DIV)

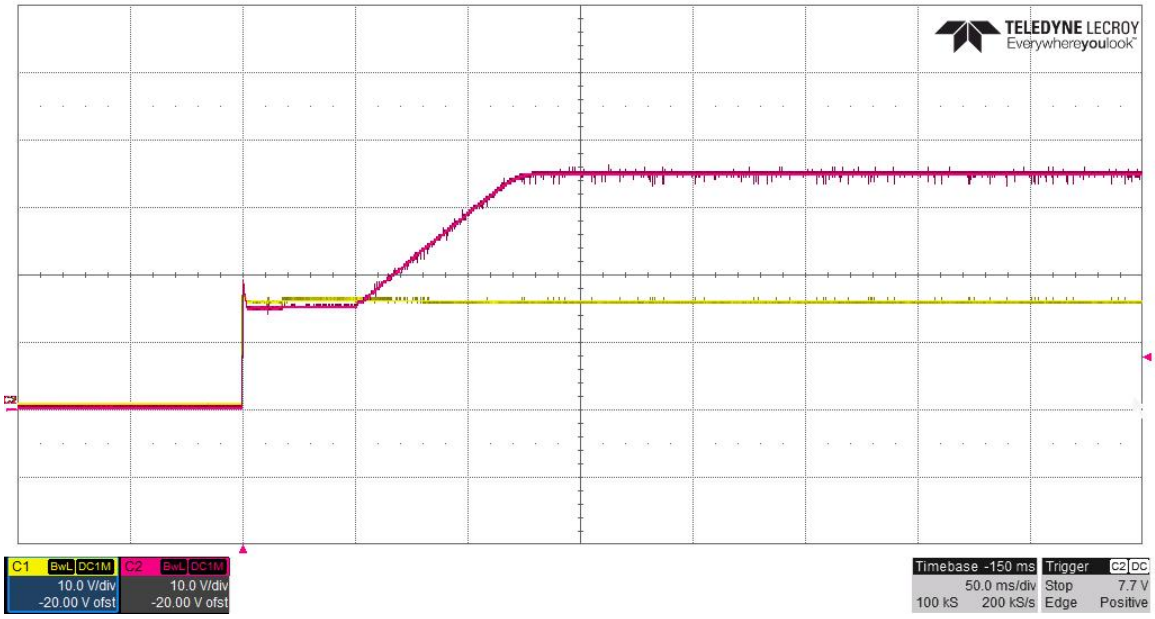


The photo below shows the output voltage startup waveform after the application of 16V in. The 35V output was loaded to 0A. (10V/DIV, 50mS/DIV)

The photo below shows the output voltage startup waveform after the application of 9V in. The 35V output was loaded to 5.72A (200W). (10V/DIV, 50mS/DIV)

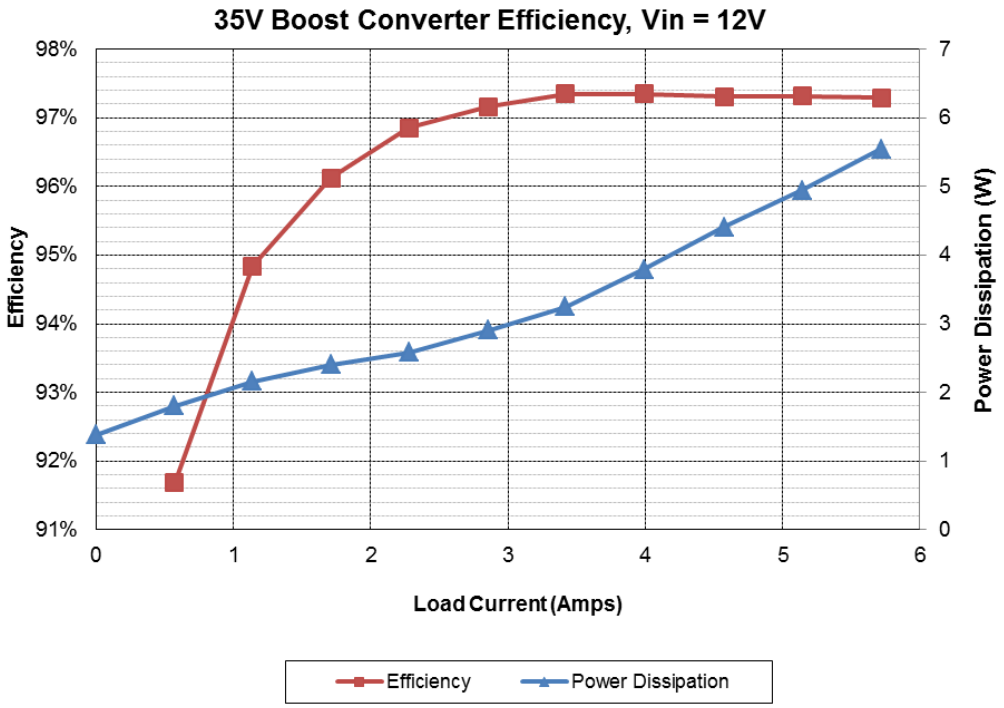


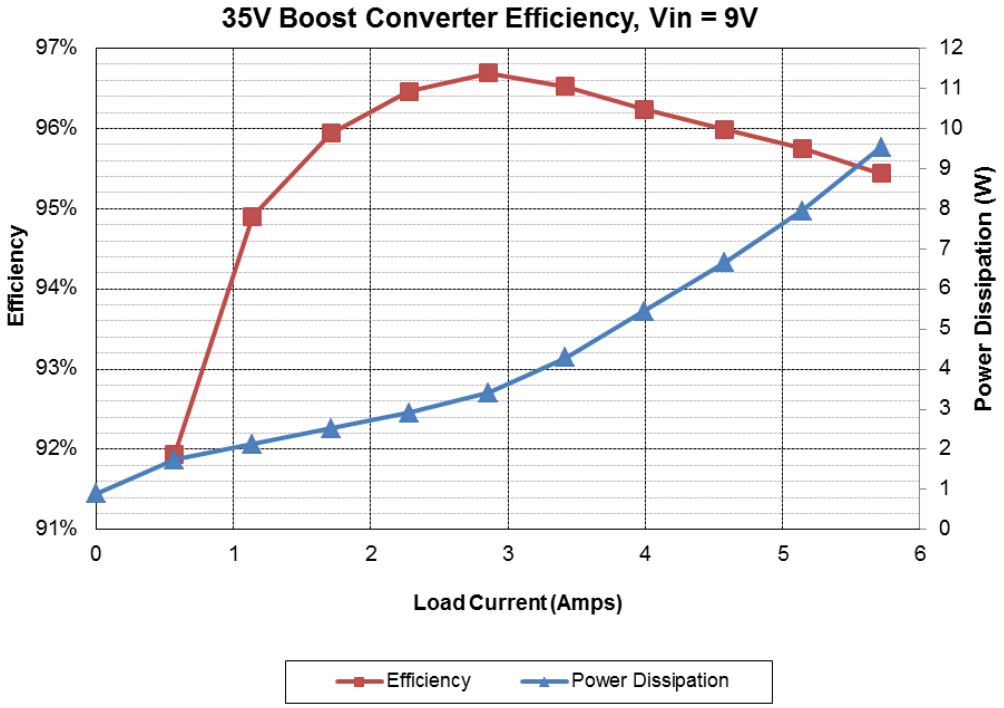
The photo below shows the output voltage startup waveform after the application of 16V in. The 35V output was loaded to 5.72A (200W). (10V/DIV, 50mS/DIV)

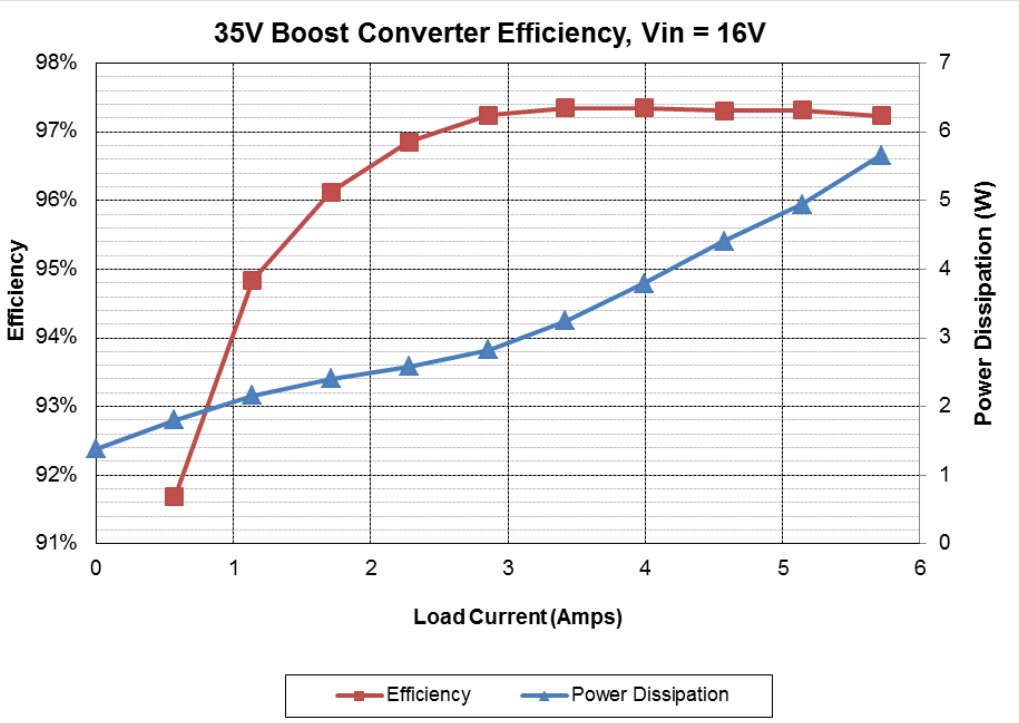


2 Efficiency

The converter efficiency is shown below.

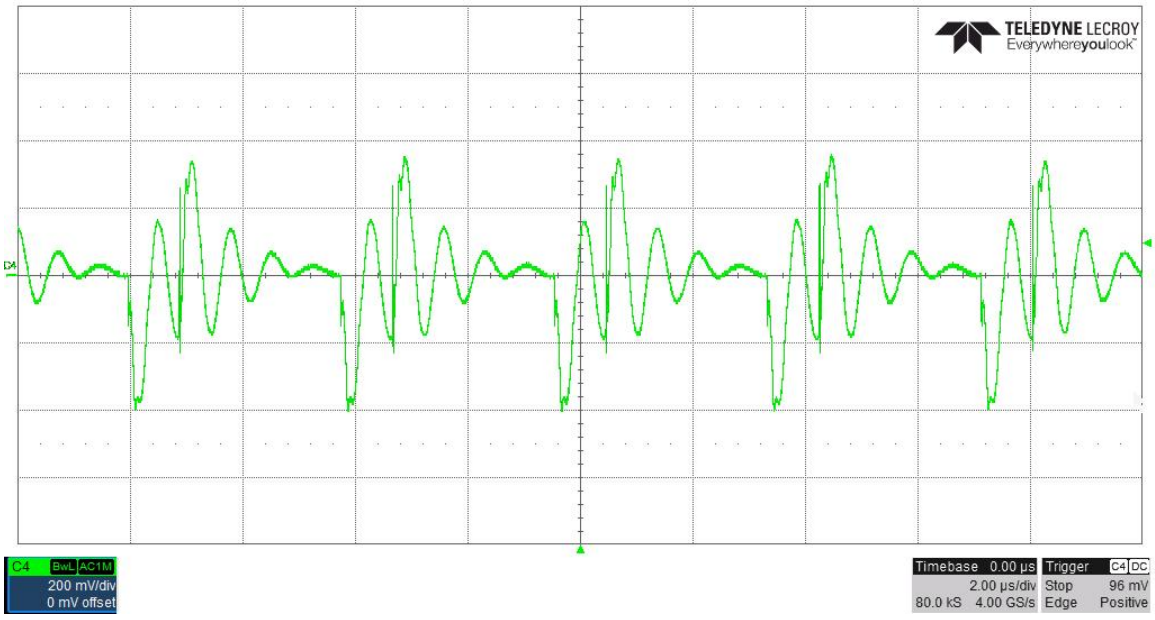




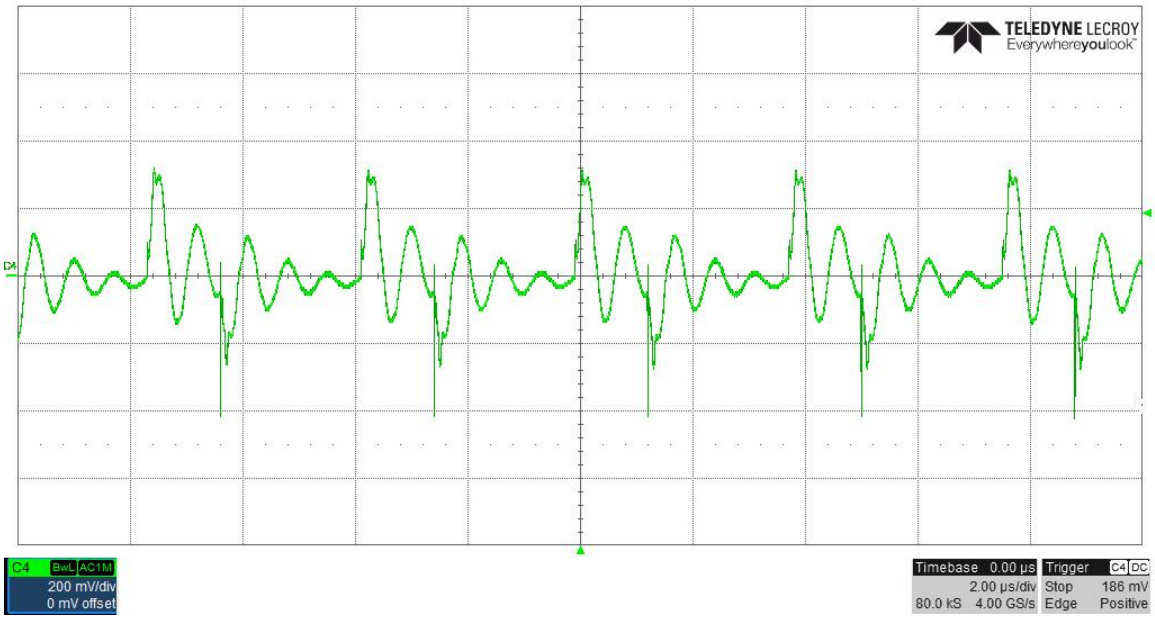

35V Boost Converter Efficiency, Vin = 16V
Efficiency
Power Dissipation (W)
Load Current (Amps)
98%
97%
96%
95%
94%
93%
92%
91%
7
6
5
4
3
2
1
0
0
1
2
3
4
5
6
Efficiency
Power Dissipation

3 Output Ripple Voltage

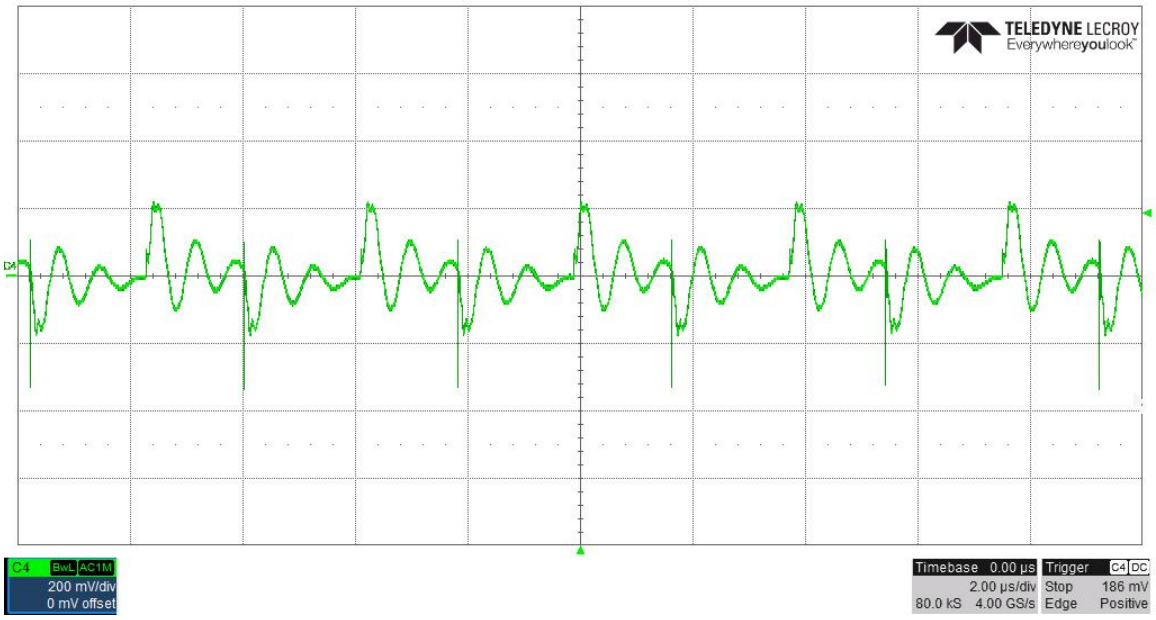
The 35V output ripple voltage (AC coupled) is shown in the figure below. The image was taken with the output loaded to 5.72A (200W). The input voltage is set to 9V. (200mV/DIV, 2uS/DIV)



The 35V output ripple voltage (AC coupled) is shown in the figure below. The image was taken with the output loaded to 5.72A (200W). The input voltage is set to 12V. (200mV/DIV, 2uS/DIV)

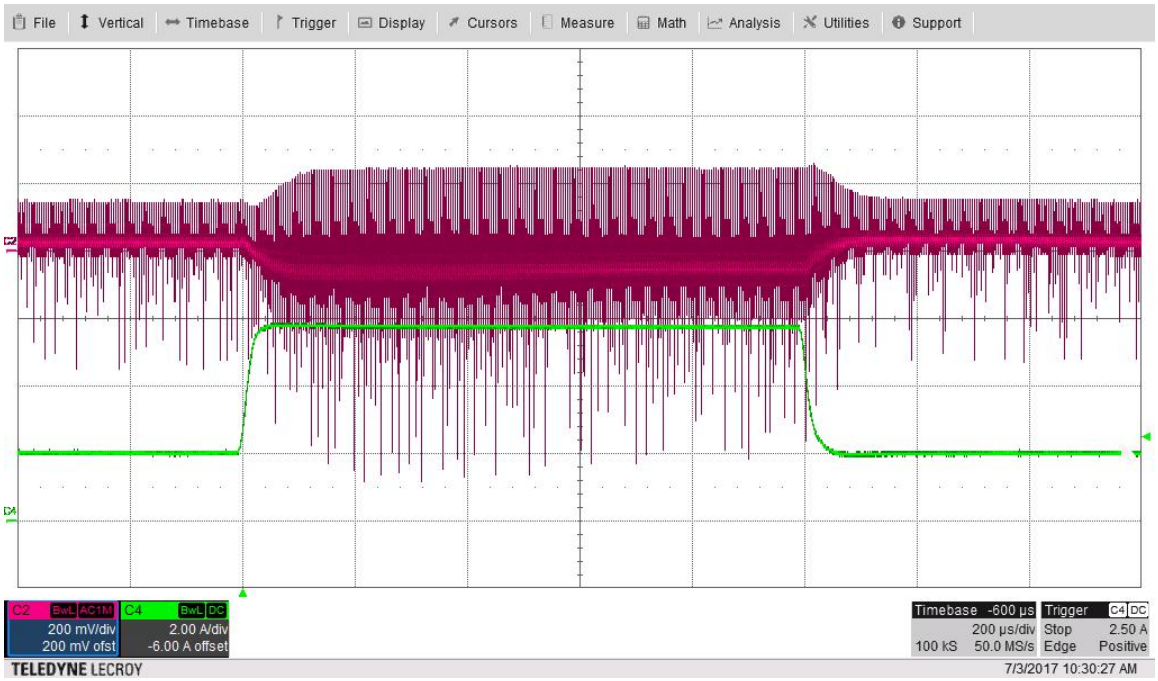


The 35V output ripple voltage (AC coupled) is shown in the figure below. The image was taken with the output loaded to 5.72A (200W). The input voltage is set to 16V. (200mV/DIV, 2uS/DIV)

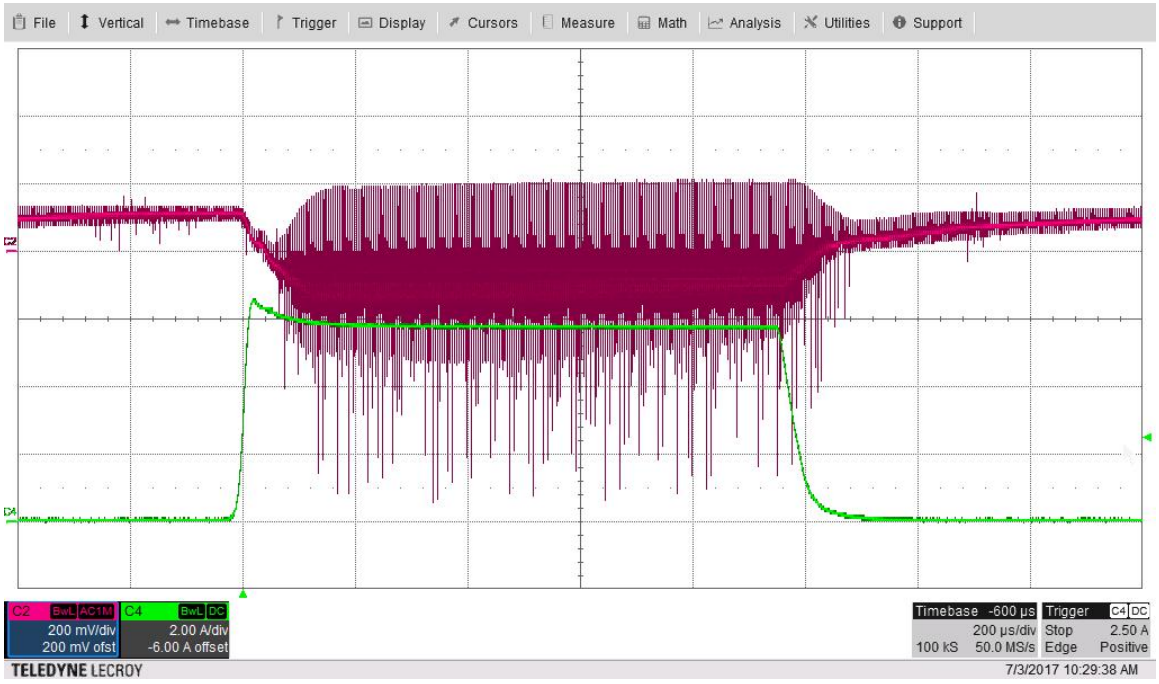


4 Load Transients

The photo below shows the 35V output voltage (ac coupled) when the load current is stepped between 2A and 5.72A. Vin = 12V. (200mV/DIV, 2A/DIV, 200uS/DIV)

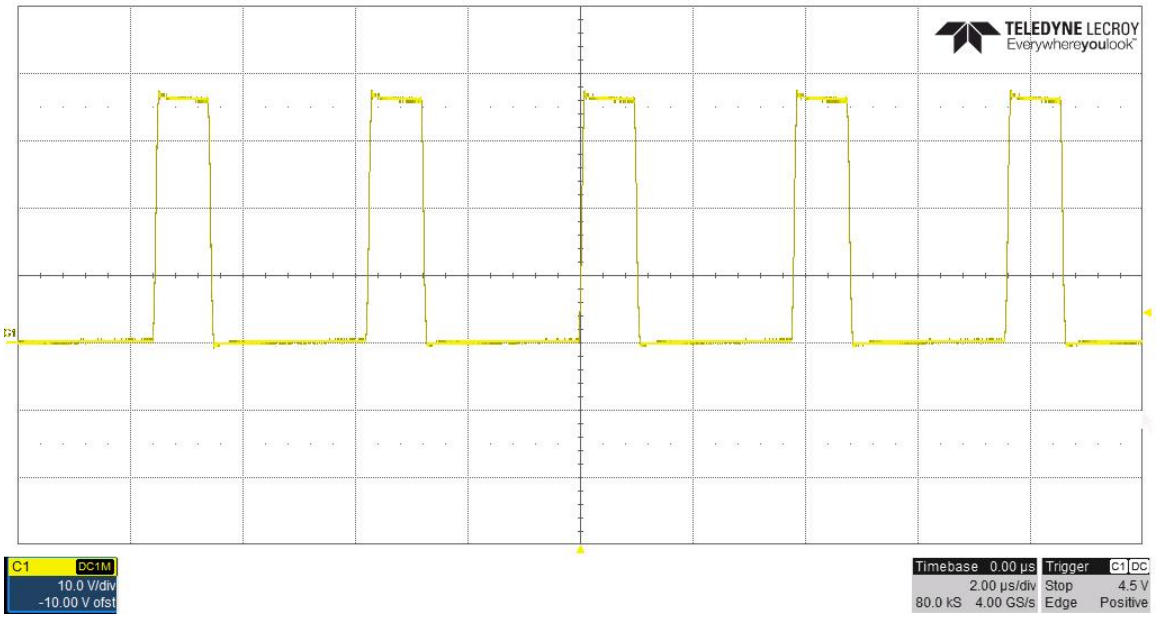


The photo below shows the 35V output voltage (ac coupled) when the load current is stepped between 0A and 5.72A. Vin = 12V. (200mV/DIV, 2A/DIV, 200uS/DIV)

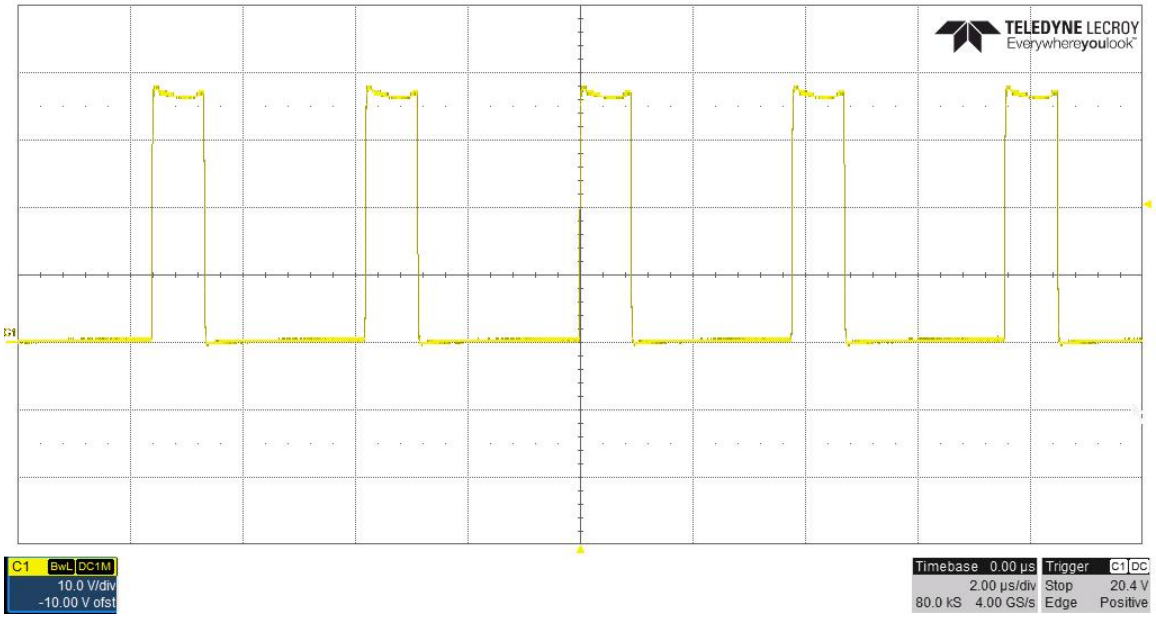


5 Switch Node Waveforms

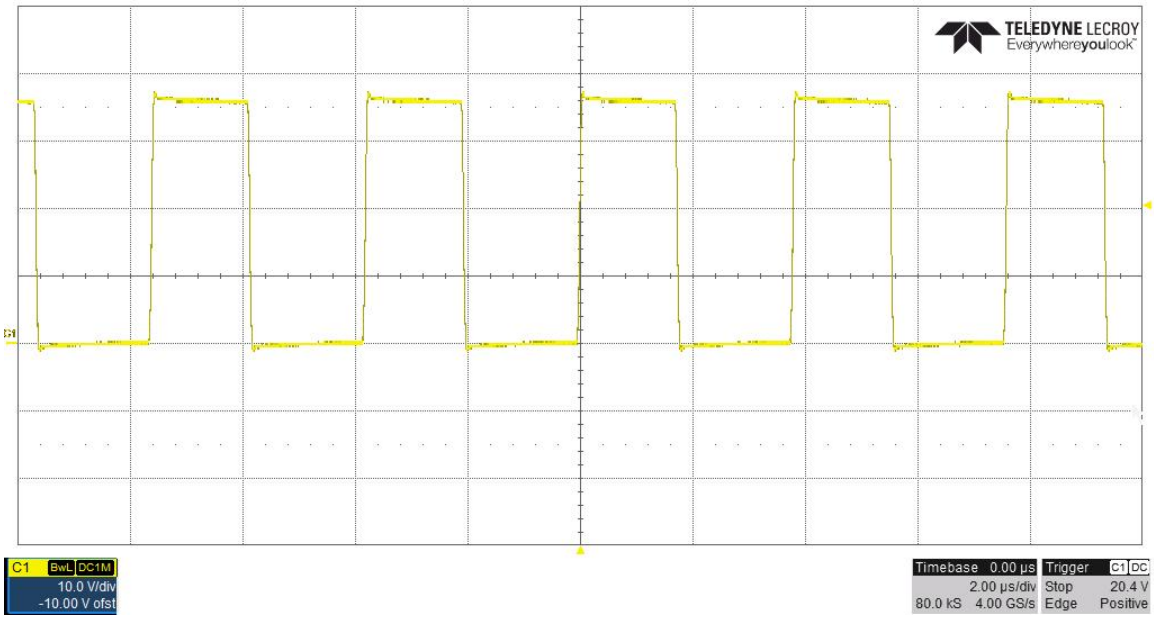
The photo below shows the FET switching voltage for an input voltage of 9V and a 0A load. (10V/DIV, 2uS/DIV)



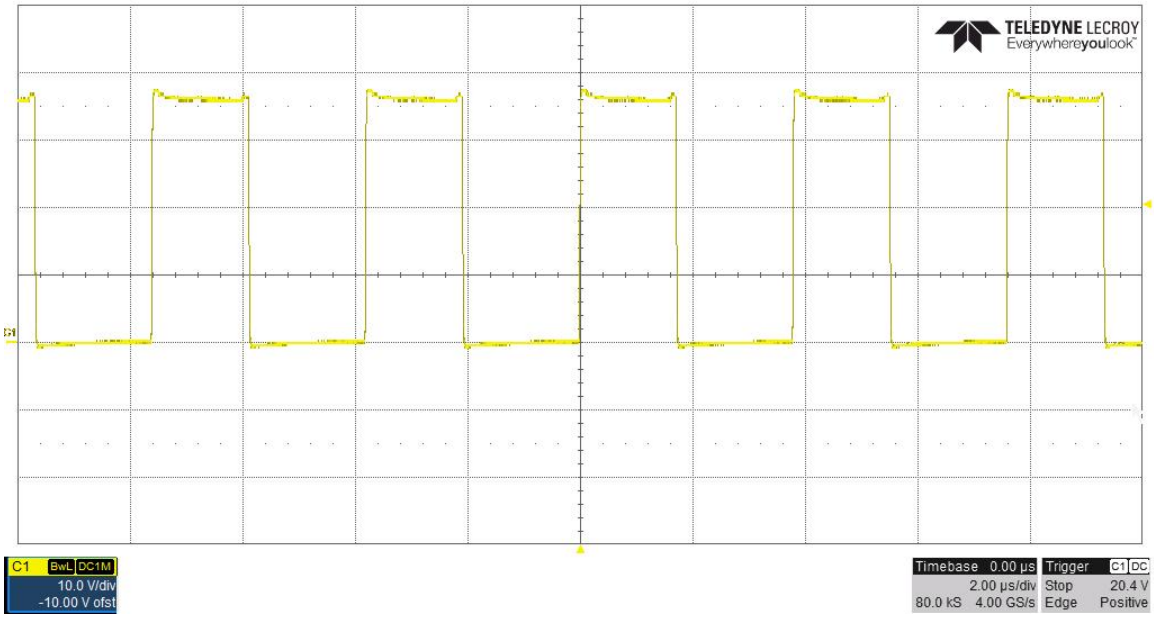
The photo below shows the FET switching voltage for an input voltage of 9V and a 5.72A load. (10V/DIV, 2uS/DIV)



The photo below shows the FET switching voltage for an input voltage of 16V and a 0A load.
(10V/DIV, 2uS/DIV)



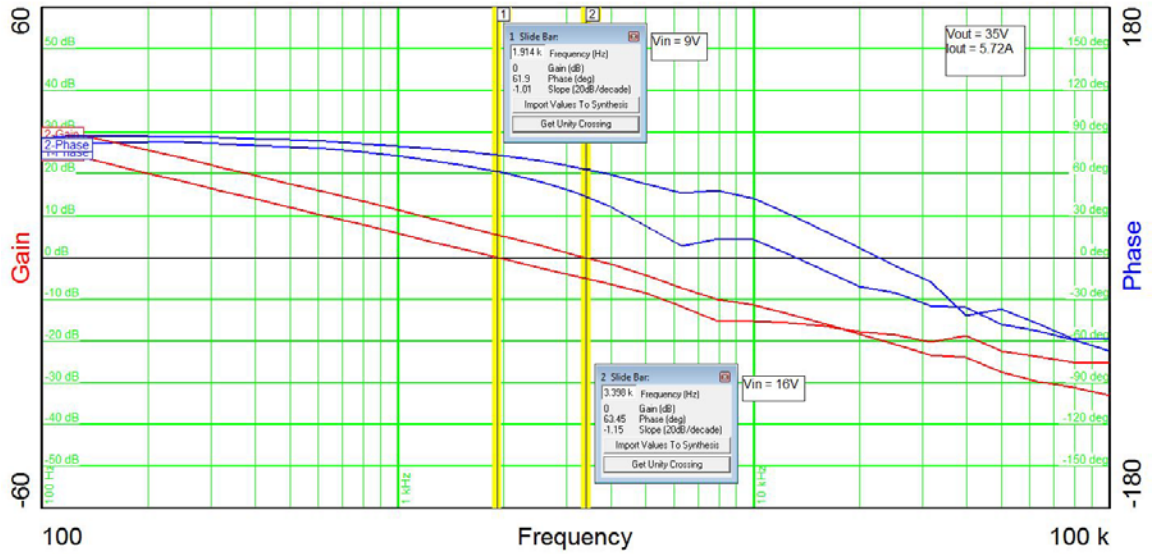
The photo below shows the FET switching voltage for an input voltage of 16V and a 5.72A load.
(10V/DIV, 2uS/DIV)



6 Loop Gain

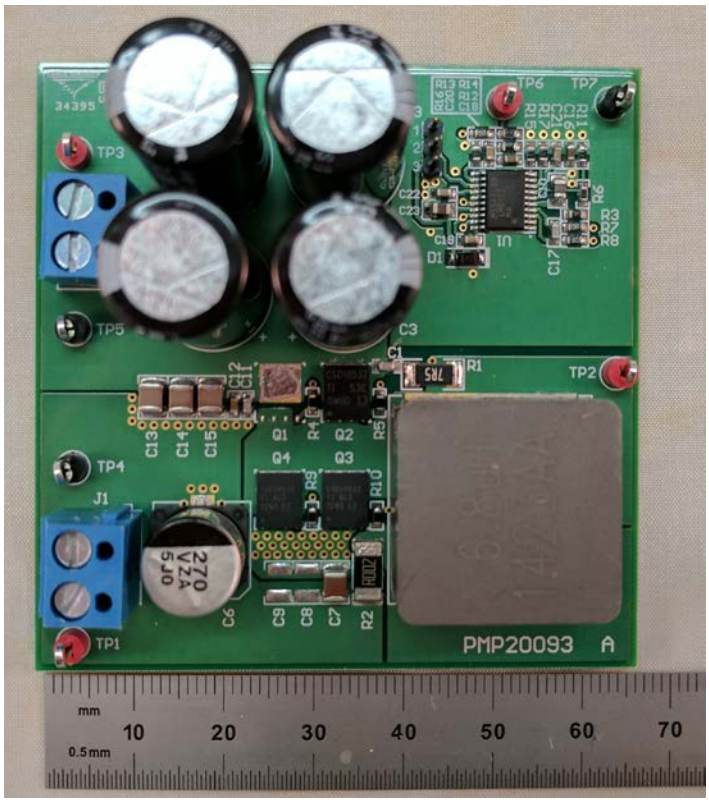
The plot below shows the loop gain with the input voltage set to 9V and 16V for an output load of 5.72A (200W).

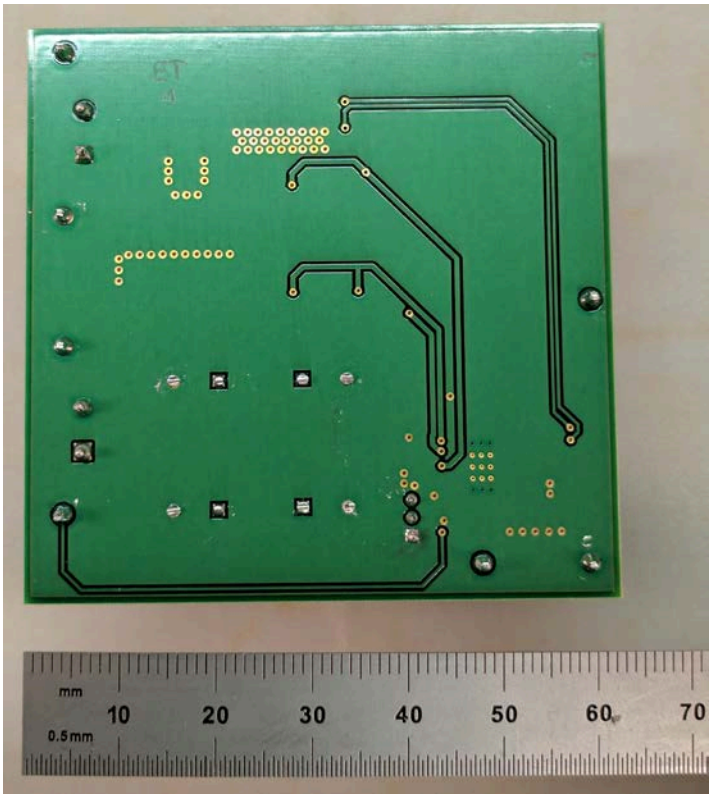
Loop Gain (Vin = 16V)	BW: 3.40KHz	PM: 63 degrees
Loop Gain (Vin = 9V)	BW: 1.91KHz	PM: 62 degrees



7 Photo

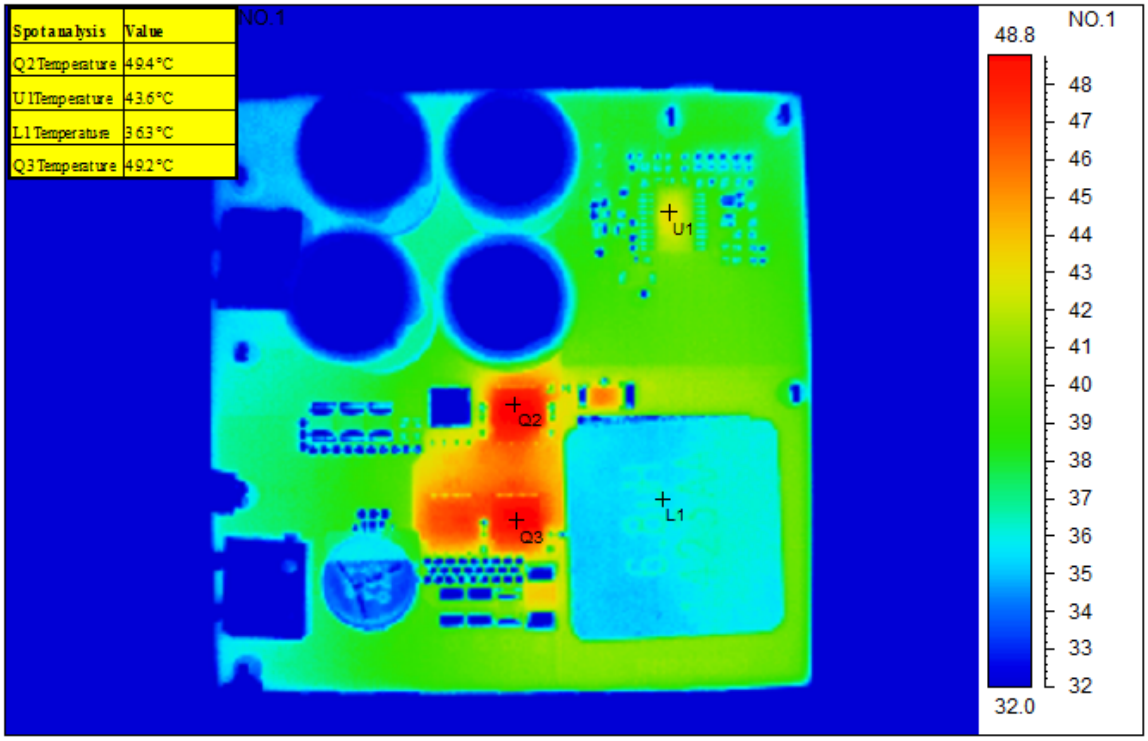
The photo below shows the PMP20093 REVC assembly.



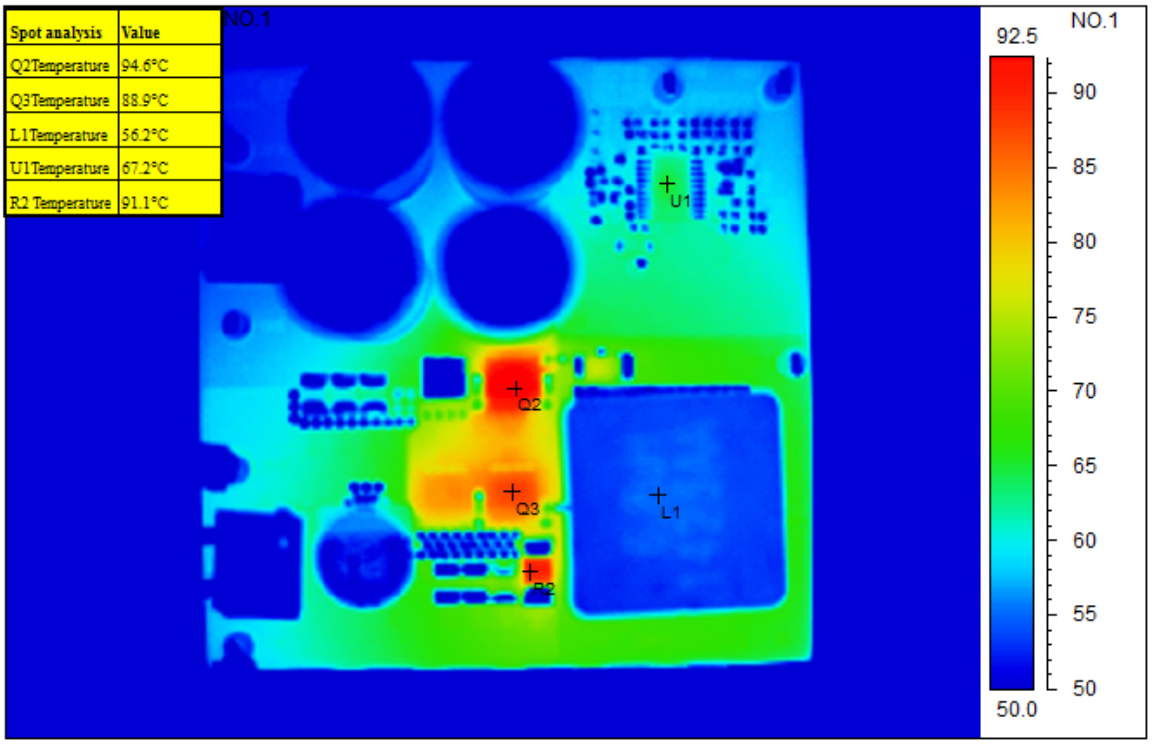


8 Thermal Image

A thermal image is shown below operating at 12V input and 35V@2A (70W) output at room temp and no airflow.



A thermal image is shown below operating at 12V input and 35V@5.72A (200W) output at room temp and no airflow.



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