Design Guide: TIDA-010133

High-Impedance, 500MHz Bandwidth Oscilloscope Analog Front End Reference Design

Description

High Bandwidth data acquisition systems, like a digital storage oscilloscope (DSO), require the analog front-end (AFE) signal chain to have wide (-3dB) bandwidth to measure a wide range of signals, optional high input impedance to prevent loading of the measured signal, low noise to prevent degradation of signal to noise ration (SNR), and good distortion performance to maintain signal fidelity. Typical implementations of an AFE typically requires either a complex discrete design or the development of a custom front-end ASIC. This reference design provides a simpler cost-effective AFE without sacrificing performance.

Resources

TIDA-010133	Design Folder
BUF802, LMH6518	Product Folder
OPA2140, LMH6552	Product Folder
DAC80508, TPL0102	Product Folder
TLV3605	Product Folder

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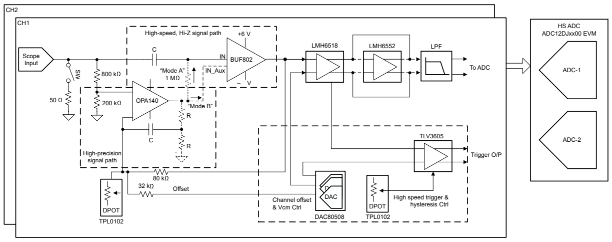
Features

- 500MHz input bandwidth
- Selectable impedance (50Ω or 1MΩ)
- Support DC/AC coupling
- Wide dynamic range of 40dB programmable gain
- Support trigger function
- Precision DAC for offset control and common-mode control
- SMA connector to support TI high-speed ADC EVM

Applications

- Oscilloscope (DSO) - Benchtop
- Digitizer (>= 50MSPS)
- Precision multifunction input and output DAQ



1 System Description

This reference design showcases the implementation of a AFE signal path utilizing the BUF802, an open-loop unity gain buffer with a Junction-Gate Field-Effect (JFET) input stage for end equipment such as Digital Storage Oscilloscopes (DSO) and Digitizers. Specifications for the design in this guide include, but are not limited to, a DC-500MHz bandwidth, selectable input impedance (1MΩ or 50Ω), support for AC and DC coupling at the input and output.

There are several additional key devices, which are highlighted in this reference design. The LMH6518, a digitally controlled variable gain amplifier (DVGA) provides 40dB of dynamic range and additional features, including auxiliary output and overvoltage clamp. The DAC80508, a 16-bit, eight-channel, buffered voltage-output digital-to-analog converter (DAC) is used for offset, trigger reference, calibration and common mode voltage control.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input Channels	2
Input Type	Single-Ended
Input Impedance	1MΩ or 50Ω
Output Type	AC or DC Coupled
Analog Bandwidth	DC - 500MHz
Maximum Input Voltage	1Vpp
Maximum System Gain	40dB
Dynamic Range	40dB
System SNR	66dB
System ENOB	10.6
Operating Temperature	25 °C
Trigger Propagation Delay	800pS
Trigger Rise/Fall Time	350pS

2 System Overview

2.1 Block Diagram

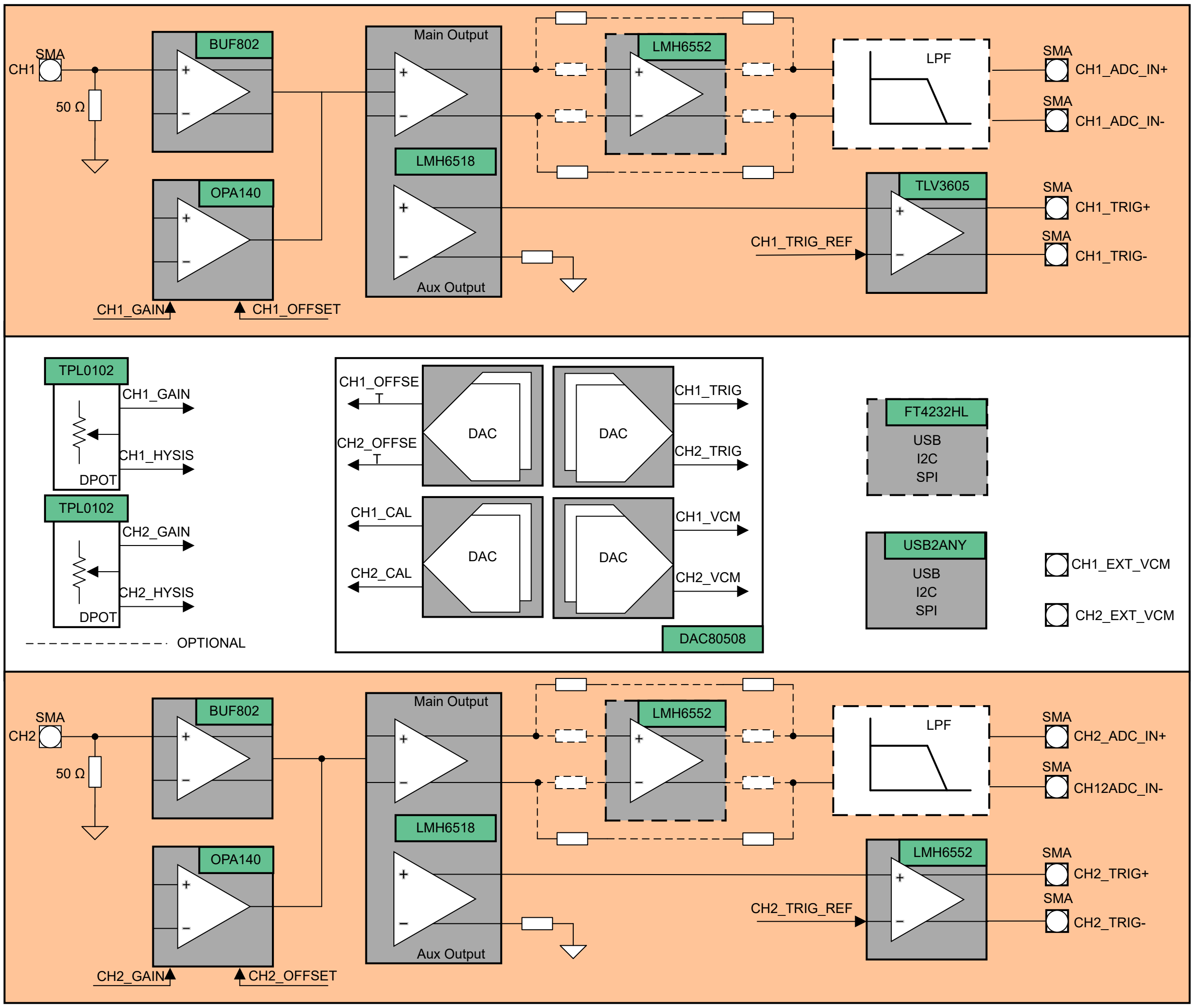


Figure 2-1. Block Diagram

2.2 Design Considerations

Figure 2-1 shows the subsystem block diagram.

Multichannel digital storage oscilloscopes require a signal chain with a wideband AFE, high dynamic range (SFDR), high SNR, and low channel-to-channel skew. Most high-speed oscilloscopes use 8-bit vertical resolution for waveform visualization, but due to technological advancements, newer generation oscilloscopes need 12+ bits of resolution. The analog bandwidth in the 200MHz to 5GHz range requires a sampling rate from five to hundreds of GSPS.

Typically, oscilloscopes have wide embedded displays and advanced triggering, with the probing capability necessary for debugging high-speed digital systems, high-speed serial protocols, and radar and wideband communication systems.

In contrast with digital oscilloscopes, high-speed wideband digitizers require a higher resolution and a wide dynamic range. Typically, these systems have a minimum level of front-end attenuation and maximum input ranges are limited. The data captured is transferred to a controller via a high-speed, multilane PCIe bus or a high-speed SERDES interface. After post-processing, results are displayed in the frequency domain. Most of the analysis is done in application software and displayed at the controller so there is no need for an embedded display used in an oscilloscope. The digitizer is useful for ATE applications and high-density multi-channel systems. The addition of advanced triggering and user programmability enables the digitizer to be used as a wideband oscilloscope and vice versa.

2.3 System Design Theory

2.3.1 Analog Front-End

The AFE of a DSO measures a voltage signal without disturbing the measured quantity. To reliably capture high-frequency signals and fast transient pulses, the AFE requires high-performance signal chains which must have a large bandwidth, support both a 50Ω and high input impedance, and offer good SNR and distortion performance.

Systems which require a high-input impedance mode usually follow one of two approaches: a custom front-end ASIC or a discrete JFET implementation. Either approach incurs the high cost of developing and manufacturing a custom ASIC or a complex discrete circuit which comes with its own set of design challenges. The BUF802 provides a single chip alternative to both ASIC and FET-based implementations by providing an all-in-one design which provides a simpler and more cost-effective design without sacrificing performance.

2.3.1.1 Input Buffer Amplifier

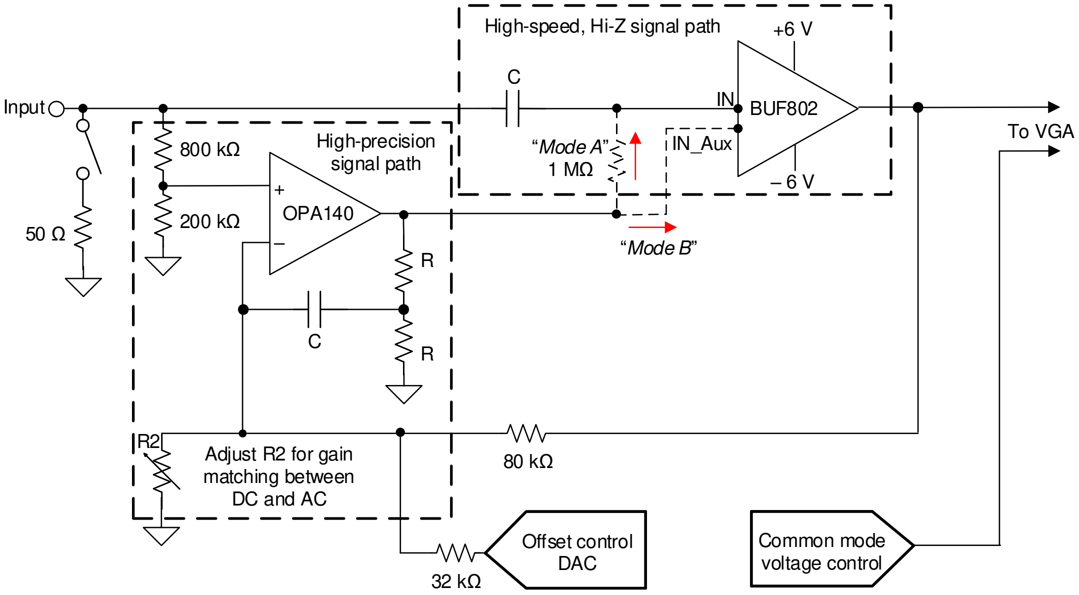


Figure 2-2. BUF802 Composite Loop

To overcome the design challenges which come with discrete JFET implementation, designers consider a composite loop based approach which interleaves the low- and high-frequency signal chain to achieve DC precision and a wide large signal bandwidth.

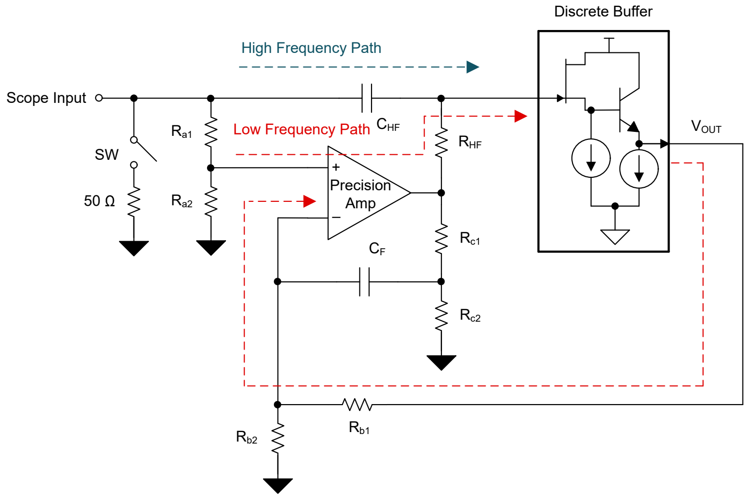


Figure 2-3. Discrete JFET Architecture

The typical discrete implementation, Figure 2-3, uses a precision amplifier and a discrete JFET configured in a composite loop. The low-frequency path gives the net transfer function good DC precision, whereas the JFET source follower-based high-frequency path enables the net transfer function to have a wide large signal bandwidth, as well as low noise and distortion.

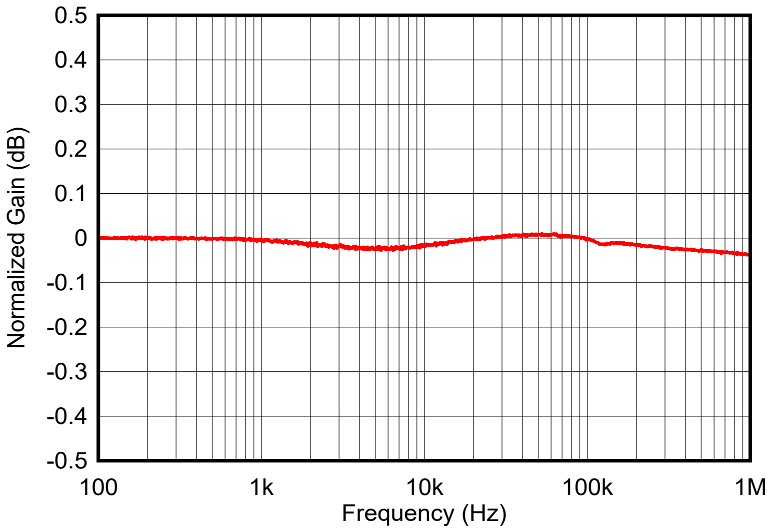


Figure 2-4. Cross-Over Region Frequency Response Flatness

For this reference design, all component values for the composite loop architecture have been carefully chosen and are recommended to achieve a flat bandwidth response for the crossover region (see Figure 2-4). For a detailed design overview on how to properly implement the values for the composite loop, please refer to the BUF802 datasheet section *9.2.1.2 Detailed Design Procedure*. To read more on the composite loop architecture, please refer to the TI blog post, *Achieving high-DC precision and wide large signal bandwidth with Hi-Z buffers*.

Input Impedance

Data acquisition systems typically have the option for both a selectable 50Ω input and 1MΩ input termination option. The BUF802 has the flexibility to be used in both 1MΩ and 50Ω terminated systems. The reference design, by default, is configured with a 50Ω input impedance, but users can configure the input impedance of the reference design between Hi-Z or 50Ω by removing or installing a parallel 50Ω resistor at each channel.

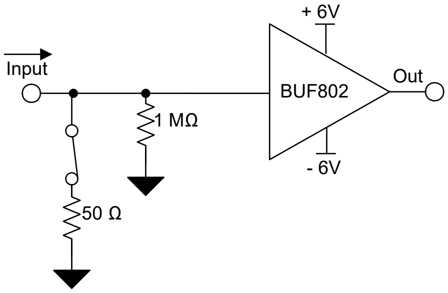


Figure 2-5. BUF802 with Optional 1MΩ/50Ω Termination

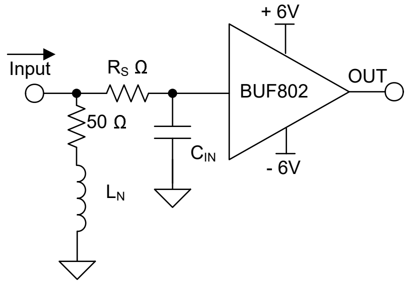


Figure 2-6. Effective Input Impedance with R_S and L_N

	Resistor	Input Impedance
Channel 1	R3 Installed	50Ω
Channel 1	R3 DNI	1MΩ
Channel 2	R4 Installed	50Ω
Channel 2	R4 DNI	1MΩ

While possible to mount an exact 50Ω termination to achieve the resistance at the input of the front-end composite loop circuit, the parasitic capacitance of the BUF802 (C_{IN}) appears in parallel with the 50Ω resistance resulting in a non-ideal termination across frequency. For a detailed design overview on how to properly implement the values for optimized S11 and S21 parameters, please refer to the BUF802 datasheet section *9.2.1.2 Detailed Design Procedure*.

Adjustable Quiescent Current

The BUF802 includes an adjustable quiescent current feature to allow the system designer to trade-off the current consumed versus the distortion performance obtained. A higher resistor value between the R_Bias pin and V_{s-} lowers the quiescent current but increases the THD and Bandwidth of the BUF802.

In this design, the value of the resistor for R_Bias was chosen to be 17.8K as recommended by the datasheet. But the R_Bias resistor can be updated to fit the needs of different system requirements. A higher R_Bias value results in less power consumption but will degrade performance. (see Figure 2-7 and Figure 2-8)

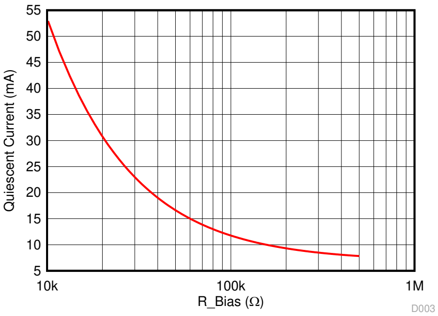


Figure 2-7. Quiescent Current versus R_Bias

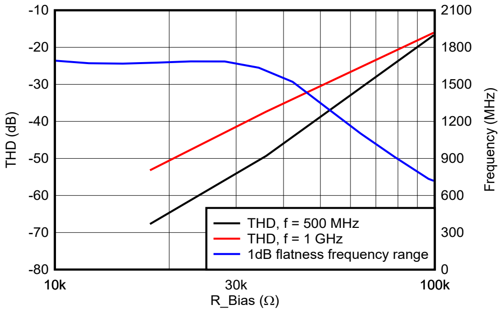


Figure 2-8. THD and Bandwidth versus R_Bias

DC Offset

The reference design also includes user adjustable DC analog offset. DC offset is used in data acquisition systems when a user desires to adjust the DC voltage level of signals that are being measured. For a DSO application, this translates to adjusting the vertical reference level of signals shown on the screen of the DSO. In other words, moving the horizontal reference line of the DSO vertically up and down.

The DC offset signal originates from the DAC80508, an 8-channel 16-bit precision DAC. However the DAC output is only unipolar which only allows for positive offset correction. To have offset control for both positive and negative adjustments, an OPA2140 precision amplifier circuit is used to convert from unipolar to bipolar, as shown in Figure 2-9.

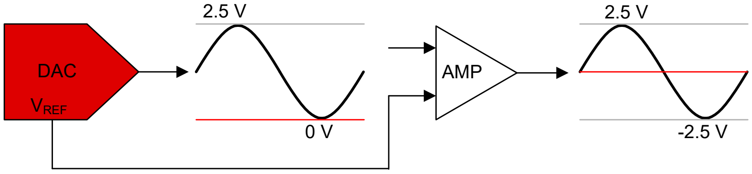


Figure 2-9. Unipolar to Bipolar

Due to the LMH6518 differential input absolute maximum rating of ∓1V, the offset voltage must be limited depending on the input source signal as to not exceed the absolute max rating.

PCB Layout

Just as the input impedance circuit needs to be optimized, as shown in BUF802 datasheet section *9.2.1.2 Detailed Design Procedure*, to maintain optimal performance across the frequency bandwidth of the system, there are also design considerations for the PCB layout. The signal path traces need to be designed with a 50Ω impedance characteristic.

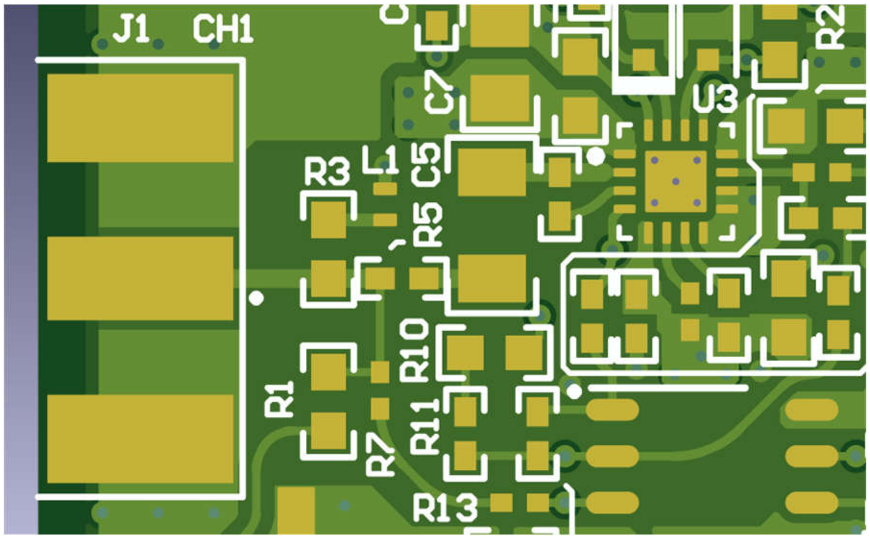


Figure 2-10. TIDA-010133 Input Layout

Failure to account for these design considerations can result in the signal trace not maintaining a 50Ω characteristic across the frequency bandwidth, leading to reflections which degrade the system performance.

2.3.1.2 Variable Gain Amplifier

The LMH6518 DVGA delivers excellent gain control and distortion performance with customizable features which enable precise signal acquisition and offers superior timing performance critical for real time signal measurements with additional features, including an auxiliary output and overvoltage clamp.

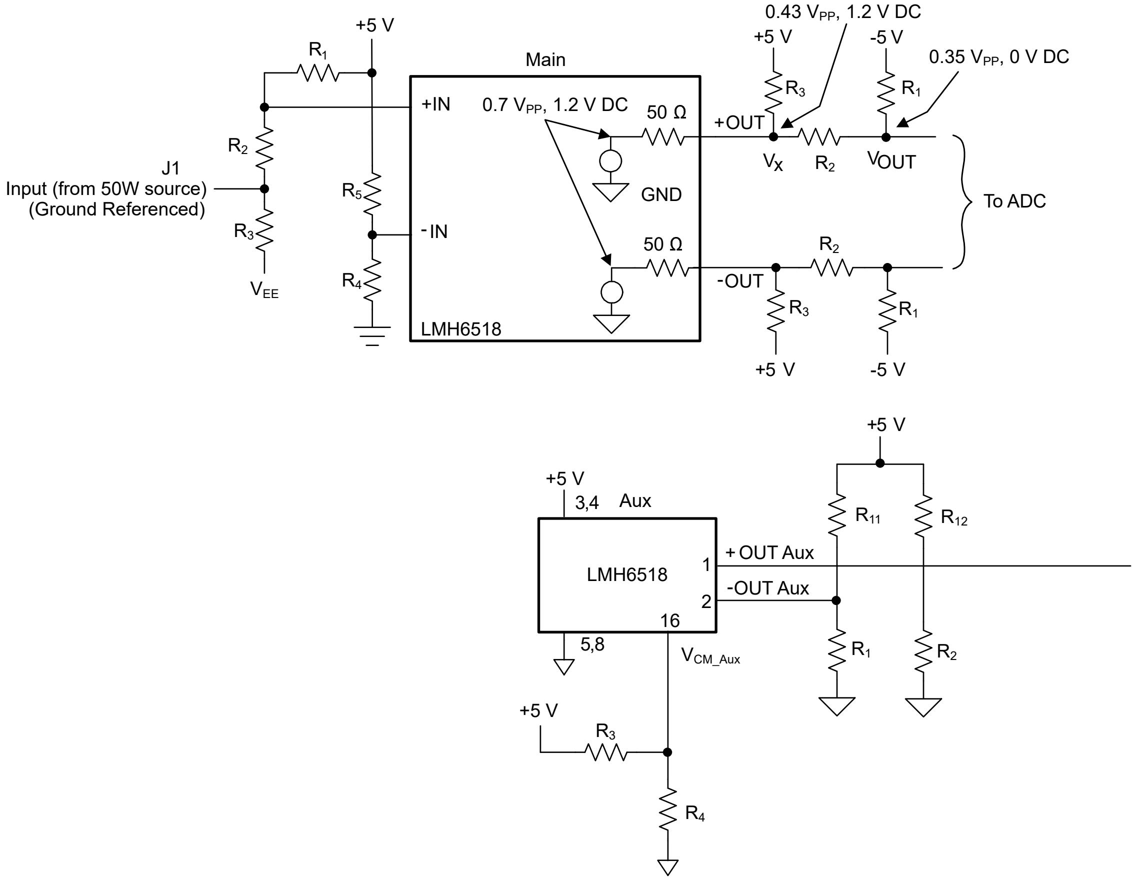


Figure 2-11. LMH6518 Functional Block Diagram

Single-to-Differential Conversion (Input Stage)

To drive differential ADC, the analog signal path contains a conversion stage to convert the input signal from single-ended to differential. The LMH6518 has a fully differential pre-amplifier which has a consistent 150kΩ impedance across all gain settings, which is also able to be driven with a single-ended signal source.

Table 2-1. LMH6518 Ideal Input and Output Conditions

IMPEDANCE FROM EACH INPUT TO GROUND (Ω)	COMMON MODE INPUT (V)	DIFFERENTIAL INPUT (V_{PP})	LOAD IMPEDANCE (Ω)	DIFFERENTIAL OUTPUT (V)	COMMON MODE OUTPUT (V)
≤50	1.5 to 3.1	<0.8	100 (differential) and 50 (single-ended)	<0.77	0.95 to 1.45

The LMH6518's differential input can be driven single-ended as long as the conditions of Table 2-1 are met, and there is good matching between the driven and undriven inputs from DC to the highest frequency of interest. If not, there is a settling time impact among other possible performance degradations.

In Figure 2-11, the inputs of the LMH6518 are biased with a voltage divider composed of resistors R2/R3 and R4/R5. To change the common mode voltage at the LMH6518 input (BUF802 output), only the resistor values of R43 and R42 (R44 and R45 for channel 2) need to be updated to the desired values. The common mode voltage must be within the operating range of the LMH6518. In this design, it's set at 2.5V.

$$V_{CM}=V_{5va}\ \text{x}\ (R2/(R1+R2)) \tag{1}$$

Where V_{5va} is the 5V analog rail and R1 and R2 corresponds to Channel 1's (R43 and R42) and 2's (R45 and R44) resistors.

In the reference design the undriven input of the LMH6518, which is biased to the desired $V_{CM,}$ is also in an adder circuit used for the system's offset voltage functionality.

The reference design configures the LMH6518 to drive an external ADC. However, the LMH6518 also provides limited capabilities to shift the common mode voltage without the use of an additional amplifier stage, through the use of another bias circuit.

Figure 2-11 shows the common mode shifting circuit that is recommended in the LMH6518 datasheet. Utilizing the +5V and -5V rails, we can shift the CM to 0Vs if desired to support ADCs with a common mode voltage requirement of 0Vs.

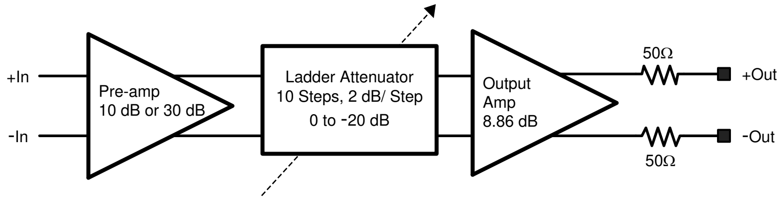


Figure 2-12. LMH6518 Internal Gain Blocks

The LMH6518 has digitally-controlled gain, voltage clamps. and bandwidth. If not used, this block can also disable the auxiliary amplifier. Programming is done via the SPI-1 compatible bus (3-wire SPI) interface which uses a bidirectional data line instead of two unidirectional ones.

The following LMH6518 functions are controlled using the SPI:

- Filters (20, 100, 200, 350, 650, 750 MHz or full bandwidth)
- Power mode (Full power or auxiliary high impedance, Hi-Z)
- Preamp (HG or LG)
- Attenuation ladder (0dB to 20dB, 10 states)
- LMH6518 state write or read back

The SPI-1 bus uses 3.3V logic. SDIO is the serial digital input-output which reads and writes to the LMH6518. SCLK is the bus clock and the chip select function controlled by CS.

The LMH6518 only has 1 register needed for programming, and Table 2-2 shows the adjustable fields.

Table 2-2. Data Field

							FILTER				PREAMP	LADDER ATTENUATION			
D15 (MSB)	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
X	0	0	0	0	0 = Full power 1 = Aux Hi-Z	0	See LMH6518 Datasheet Table 6-3			0	0 = LG 1 = HG	See LMH6518 Datasheet Table 6-4			

Note

Bits D5, D9, and D11 to D14 must be 0. Otherwise, device operation is undefined and specifications are not maintained.

The internal gain blocks consist of three stages; a pre-amplifier, a ladder attenuator, and a output amplifier. The main signal path passes through all three gain blocks, where the auxiliary signal path has a separate auxiliary output amplifier with the same characteristics of the main output path.

The most important user-adjustable settings for the LMH6518 are the filter and the gain settings. The LMH6518 is capable of operating for bandwidths up to 900MHz, but a selectable filter setting can allow the users to limit the bandwidth of the device to meet different system requirements. All filters are low-pass, single pole roll-off and operate on both main and auxiliary outputs. These filters limit the signal path bandwidth and noise.

Table 2-3. LMH6518 Gain Steps Available

Pre-Amp		Ladder Attenuation	Output Amp	Total Gain (dB)
LG	HG			
10	N/A	-20	8.86	-1.16
10	N/A	-18	8.86	0.8
10	N/A	-16	8.86	2.8
10	N/A	-14	8.86	4.8
10	N/A	-12	8.86	6.8
10	N/A	-10	8.86	8.8
10	N/A	-8	8.86	10.8
10	N/A	-6	8.86	12.8
10	N/A	-4	8.86	14.8
10	N/A	-2	8.86	16.8
10	N/A	0	8.86	18.8
N/A	30	-20	8.86	18.8
N/A	30	-18	8.86	20.8
N/A	30	-16	8.86	22.8
N/A	30	-14	8.86	24.8
N/A	30	-12	8.86	26.8
N/A	30	-10	8.86	28.8
N/A	30	-8	8.86	30.8
N/A	30	-6	8.86	32.8
N/A	30	-4	8.86	34.8
N/A	30	-2	8.86	36.8
N/A	30	0	8.86	38.8

2.3.1.3 ADC Driver with LMH6552

The LMH6552 is a fully differential amplifier that is included in this design as an additional optional common mode voltage shift stage in the signal path. The LMH6552 is to be used when the TIDA-010133 hardware is coupled with an ADC that does not support the default 1.2 VCM output from the LMH6518. The LMH6552 contains an integrated output common mode control that allows easy control of the common mode voltage through the VCM pin. In addition, the LMH6552 can be used to provide additional gain in the system. However the gain is fixed and set through the use of external resistors.

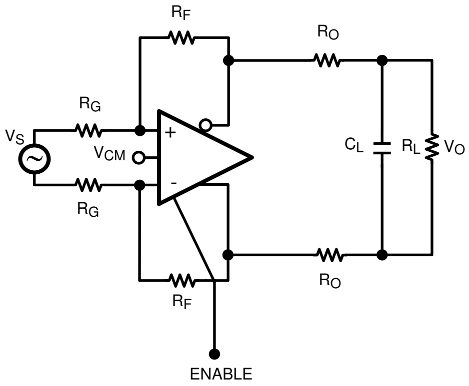


Figure 2-13. LMH6552 Typical Fully Differential Application

For the above configuration, a minimum of 0.1% tolerance resistors are recommended for optimal performance, and the amplifier is internally compensated to operate with optimum gain flatness with values of R_F between

270Ω and 390Ω depending on package selection, PCB layout, and load resistance. The following table provides R_F and R_G values and the respective gain.

Table 2-4. LMH6552 Gain with designated resistor values

Gain	R_F	R_G
0dB	275Ω	255Ω
6dB	275Ω	127Ω
12dB	275Ω	54.9Ω

2.3.1.4 Analog PI Filter

The final stage in the reference design is a passive 3rd order LC PI low pass filter. The filter is placed before the ADC to remove high frequency noise and interference from the input of the ADC to prevent any unwanted noise from coupling into the inputs.

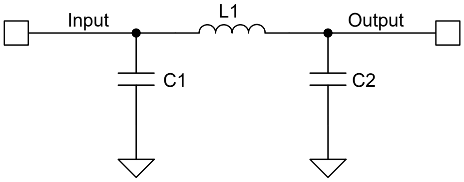


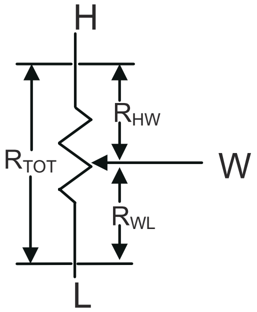
Figure 2-14. PI Filter

The filter design is composed of two capacitors and an inductor, where the values of the components determine the cutoff frequency of the filter. By having the capacitors as the shunt element in the design, the filter acts as a low pass filter. The cutoff frequency of the filter is determine by the following equation.

$$f_c = 1/(2 * \pi * \sqrt{(L * C)}) \tag{2}$$

2.3.1.5 Digital Potentiometer

The reference design uses a digital potentiometer, TPL0102, in each channel for two different purposes: providing a variable resistance to account for BUF802 trimming in the composite loop circuit, and providing hysteresis control for the high-speed comparator, TLV3605. TPL0102 provides 100kΩ end-to-end resistance as well as non-volatile memory which stores the internal wiper settings.



$R_{WL} = R_{TOT} \times D/256$

$R_{HW} = R_{TOT} \times (1 - (D/256))$

Where D = Decimal Value of Wiper Code

Figure 2-15. TPL0102 Equivalent Circuit

The configuration used in the design shorts the W (wiper) and L (low) pins, so the effective resistance is equal to R_{HW}. Figure 2-15 shows how the effective resistance is calculated. For use in the composite loop circuit, the recommended value for the digital potentiometer is approximately 6.7kΩ to account for any variance in the BUF802 and the resistors. For the hysteresis, the recommended value is 56kΩ to provide 60mV of hysteresis voltage to the input of the comparator. Both values are chosen as per recommended values in the datasheets, but can easily be adjusted via I2C to fit any system requirement.

Table 2-5. TPL0102 Settings for BUF802 and TLV3605

Function	Resistance (kΩ)	Hex	Binary
BUF802 Composite Loop	6.64	0xEFh	1110 1111

Table 2-5. TPL0102 Settings for BUF802 and TLV3605 (continued)

Function	Resistance (kΩ)	Hex	Binary
TLV3605 Hysteresis Control	60.16	0x66h	0110 0110

2.3.2 System Dynamic Range

Full Scale Input

In typical DSO front-ends and other data acquistion systems, there is an attenuator before the input of the AFE. The attenuators have selectable attenuations, such as 1:1, 2:1, 5:1, etc with a relay to allow for system control of the attenuator. An attenuator reduces the input signal before it is sent through the AFE. Overdriving the AFE can damage the signal chain devices or oversaturate the ADC input rendering the measurement useless. So the attenuator can reduce the input measurement down to a more suitable voltage for measurement.

In this reference design, there is no attenuator at the input so the user can implement their own attenuator for their specifications. The input of this reference design is not designed to be used with large signals, so the limiting factor for the input is the LMH6518. The LMH6518 has an absolute max differential input of ∓ 1V.

Dynamic Range

The overall system dynamic range can be calculated by summing maximum gain.

In the reference design, there is one gain stage, the LMH6518.

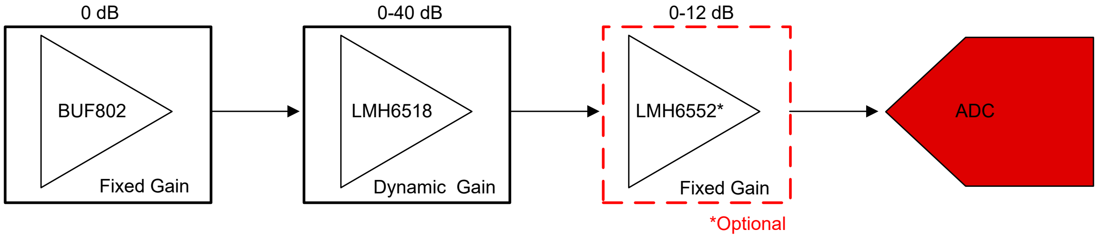


Figure 2-16. TIDA-010133 Gain Blocks

The LMH6518 is a digitally programable VGA that internally contains a pre-amp, ladder attenuator and an output amp. The user is able to configure the pre-amp and ladder attenuator stages to provide a total gain from -1.16dB to 38.8dB for a 40dB of range in 2dB steps. Looking at the tables in the *Digitally Programmable Gain* section, the user can configure the pre-amp between a gain of 10dB or 30dB. Also, the ladder attenuator can be configured between 0 and -20dB in steps of 2dB.

If LMH6552 is installed, total gain of the system is equal to the gain of the LMH6518 plus the LMH6552 when installed.

Dynamic Range$_{\text{System}}$=LMH6518 Dynamic Range+LMH6552 Dynamic Range

$$\text{Max\_Gain} = 50.8\text{dB} = 38.8\text{dB} \quad (\text{LMH6518}) + 12\text{dB} \quad (\text{LMH6552}) \tag{3}$$

$$\text{Min\_Gain} = -1.16\text{dB} = -1.16\text{dB} \quad (\text{LMH6518}) + 0\text{dB} \quad (\text{LMH6552}) \tag{4}$$

Table 2-6. System Gain

System Max Gain	System Min Gain	LMH6518 Max Gain	LMH6518 Dynamic Gain	LMH6552 Max Gain	LMH6552 Fixed Gain
50.8dB	-1.16dB	40dB	-1.16 to 38.8dB	12dB	0 to 12dB

2.4 Highlighted Products

2.4.1 BUF802

The BUF802 device is an open-loop, unity gain buffer JFET input stage that offers a low-noise, high-impedance stage. The device supports DC to 3.1GHz of bandwidth while offering excellent distortion and noise performance across the frequency range.

The BUF802 can be used as a standalone buffer, Buffer Mode (BF Mode), or in a composite loop with a precision amplifier, Composite Loop Mode (CL Mode), to achieve DC precision and a wide, large-signal bandwidth. The low output impedance and high output current drive strength enables the BUF802 to drive loads as high as 50Ω. The BUF802 comes with adjustable quiescent current to optimize system level power and performance.

2.4.2 LMH6518

The LMH6518 device is a digitally controlled variable gain amplifier with 40dB of dynamic gain and a bandwidth of 900MHz. The auxiliary output (+OUT AUX and −OUT AUX) follows the main output and is intended for use in oscilloscope trigger function circuitry but may have other uses in other applications. The LMH6518 gain is programmed through a SPI-1 compatible serial bus.

The LMH6518 is able to operate in both single-ended and differential applications. Inputs and outputs are DC-coupled. The outputs are differential with individual common mode (CM) voltage control (for main and auxiliary outputs), and have a selectable bandwidth limiting circuitry (common to both main and auxiliary) of 20, 100, 200, 350, 650, 750MHz or full bandwidth.

2.4.3 DAC80508

The DAC80508 is a pin-compatible family of low-power, eight-channel, buffered voltage-output digital-to-analog converters (DACs) with 16-, 14- and 12-bit resolution. The DACx0508 includes a 2.5V internal reference and user selectable gain configuration providing full scale output voltages of 1.25V (gain = ½), 2.5V (gain = 1) or 5V (gain = 2). The device operates from a single 2.7V to 5.5V supply, is specified monotonic, and provides high linearity of ±1 LSB INL.

2.4.4 TLV3605

The TLV3605 is a 800-ps, high-speed comparators with LVDS outputs and rail-to-rail inputs. These features, along with an operating voltage range of 2.4V to 5.5V and a high toggle frequency of 3Gbps, make the TLV3605 well suited for LIDAR, clock and data recovery applications, and test and measurement systems.

The Low-Voltage-Differential-Signal (LVDS) output of the TLV3605 also helps increase data throughput and optimizes power consumption. The complementary outputs reduce EMI by suppressing common mode noise on each output. The LVDS output is designed to drive and interface directly with downstream devices that accept a standard LVDS input, such as high-speed FPGAs and CPUs.

Other options for the high speed comparator are available. Table 2-7 lists some of the comparable options.

Table 2-7. High Speed Comparator Option

	TLV3604	TLV3605	TLV3801	LMH7220	LMH7324	LMH7322	TLV3603	TLV3601	TLV3502	TLV3501
Number of channels (#)	1	1	1	1	4	2	1	1	2	1
Output type	LVDS	LVDS	LVDS	LVDS	RSPECL	RSPECL	Push-pull	Push-pull	Push-pull	Push-pull
Propagation delay time (ns)	0.8	0.	0.225	2.9	0.7	0.7	2.5	2.5	4.5	4.5
Vs (Max) (V)	5.5	5.5	4.2	12	12	12	5.5	5.5	5.5	5.5
Vs (Min) (V)	2.4	2.4	2.7	2.7	5	2.7	2.4		2.7	2.7
Rail-to-rail	In	In	No	No	No	No	In-Out	In-Out	In-Out	In-Out

2.4.5 TPL0102

The TPL0102 has two linear-taper digital potentiometers (DPOTs) with 256 wiper positions. Each potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat. The TPL0102-100 has an end-to-end resistance of 100kΩ.

The TPL0102 has non-volatile memory (EEPROM) which can be used to store the wiper position. This is beneficial because the wiper position is stored even during power-off and is automatically reinstated after power-on. The internal registers of the TPL0102 can be accessed using the I2C interface.

Other options for the digital potentiometers are available. Table 2-8 lists some of the comparable options.

Table 2-8. Digital Potentiometer Option

	TPL0102-100	TPL0401A-10	TPL0401B-10	TPL0501-100	TPL0202-10
# of Steps	256	128	128	256	256
# of Channels	2	1	1	1	2
End-to-End Resistance (kΩ)	100	10	10	100	10
Resistance Taper	Linear	Linear	Linear	Linear	Linear
Interface Type	I2C	I2C	I2C	SPI	SPI
Memory	Non-Volatile	Volatile	Volatile	Volatile	Non-Volatile

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

This reference design is the analog front end (AFE) with connections provided to integrate with an external ADC EVM through its SMA connectors. An example for the full setup is shown below with ADC12J5200RFEVM. Other ADC EVM could also be used that are within these reference design levels.

This AFE reference design can be evaluated by itself using the USB2ANY controller as described in section Section 3.2.2

3.2 Test Setup

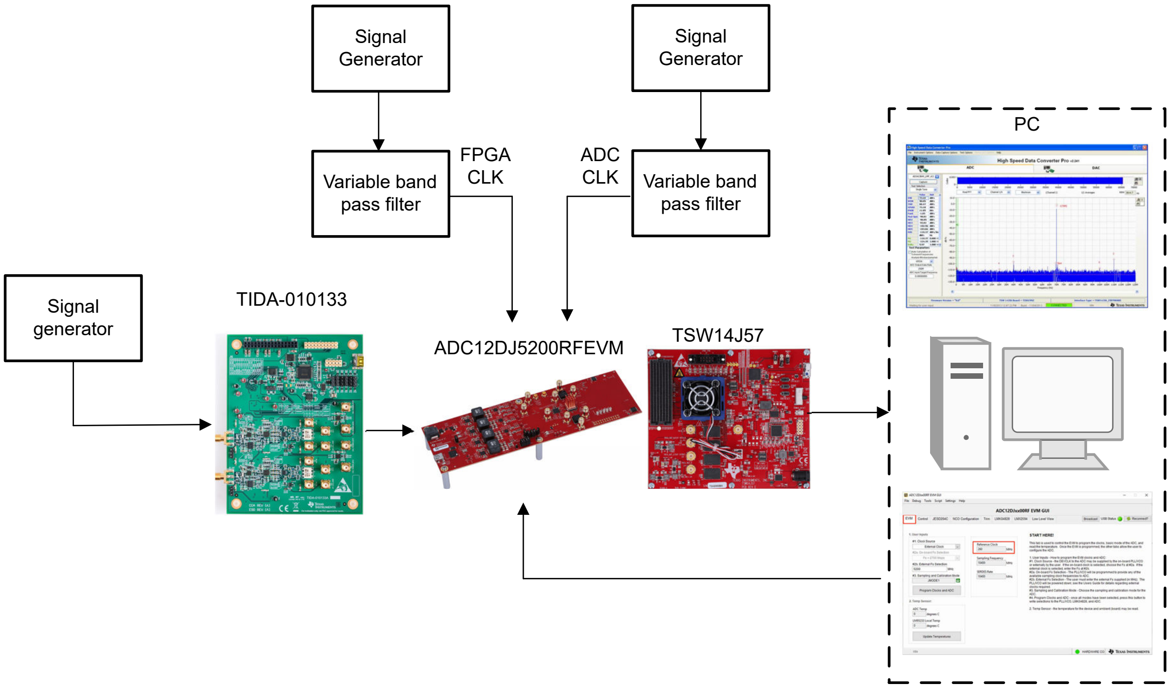


Figure 3-1. EVM Test Setup

3.2.1 ADC Configuration

ADC Hardware Setup

1. **Install the High Speed Data Converter (HSDC) Pro Software**
    a. Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.
2. **Install the Configuration GUI Software**
    a. Download the Configuration GUI software from the EVM tool folder at ADC12DJ5200RF GUI.
    b. Extract files from the .zip file.
    c. Run the executable file (setup.exe), and follow the instructions.
3. **Connect the EVM and TSW14J57EVM**
    a. With the power off, connect the ADCxxDJxx00RFEVM to the TSW14J57EVM through the FMC connector. Verify that the standoffs provide the proper height for robust connector connections.
4. **Connect the Power Supplies to the Boards (Power Off)**
    a. Confirm that the power switch on the TSW14J57EVM is in the off position. Connect the power cable to a 12V DC (minimum 3A) power supply. Verify the proper supply polarity by confirming that the outer

surface of the barrel connector is GND and the inner portion of the connector is 12V. Connect the power cable to the EVM power connector.

   b. Confirm that the power switch for the ADC12DJ5200EVM's power supply is in the off position. Connect the power cable to a 12V DC (minimum 2A) power supply. Verify the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12V. Connect the power cable to the EVM power connector.

5. **Connect the TIDA-010133 hardware to the EVM (RF Outputs Disabled Until Directed)**
   a. Using a short SMA cable, connect the output of the TIDA-010133 hardware to the VIN input of the ADC12DJ5200RFEVM. Either AC/DC coupled inputs work, just verify both hardware boards are configured the same.
6. **Turn On the TSW14J57EVM Power and Connect to the PC**
   a. Turn on the power switch of the TSW14J57EVM.
   b. Connect a mini-USB cable from the PC to the TSW14J57EVM.
   c. If this is the first time connecting the TSW14J57EVM to the PC, follow the on-screen instructions to automatically install the device drivers. See the TSW14J57EVM user's guide for specific instructions
7. **Turn On the ADC12DJ5200RFEVM Power Supplies and Connect to the PC**
   a. Turn on the 12V power supply to power up the EVM.
   b. Connect the EVM to the PC with the mini-USB cable.
8. **Turn On the Signal Generator RF Outputs**
   a. Turn on the RF signal output of the signal generator connected to the TIDA-10133 hardware. If external clocking is used, turn on the RF signal outputs connected to DEVCLK and Reference clock.
9. **Open the ADC12DJ5200RFEVM GUI and Program the ADC and Clocks**

   The Device Configuration GUI is installed separately from the HSDC Pro installation and is a stand-alone GUI.

When External Clocking is Used

1. Connect a signal generator to the DEVCLK input of the EVM through a bandpass filter. This signal generator must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal coming from the generator. Configure the signal generator for the desired clock frequency in the range of 0.8 to 5.2GHz. For best performance when using an RF signal generator, the power input to the CLK SMA connector must be 10 dBm (2.0 Vpp into 50 Ω). The signal generator must increase above 10 dBm by an amount equal to any additional attenuation in the clock signal path, such as the insertion loss of the bandpass filter. For example, if the filter insertion loss is 2dB, the signal generator must be set to 10dBm + 2 dB = 12dBm.
2. Connect a signal generator to the reference signal input of the EVM at REF CLK(J17). Configure the signal generator for the desired (260MHz) clock frequency. Set the output power to approximately 6–9dBm.

Note

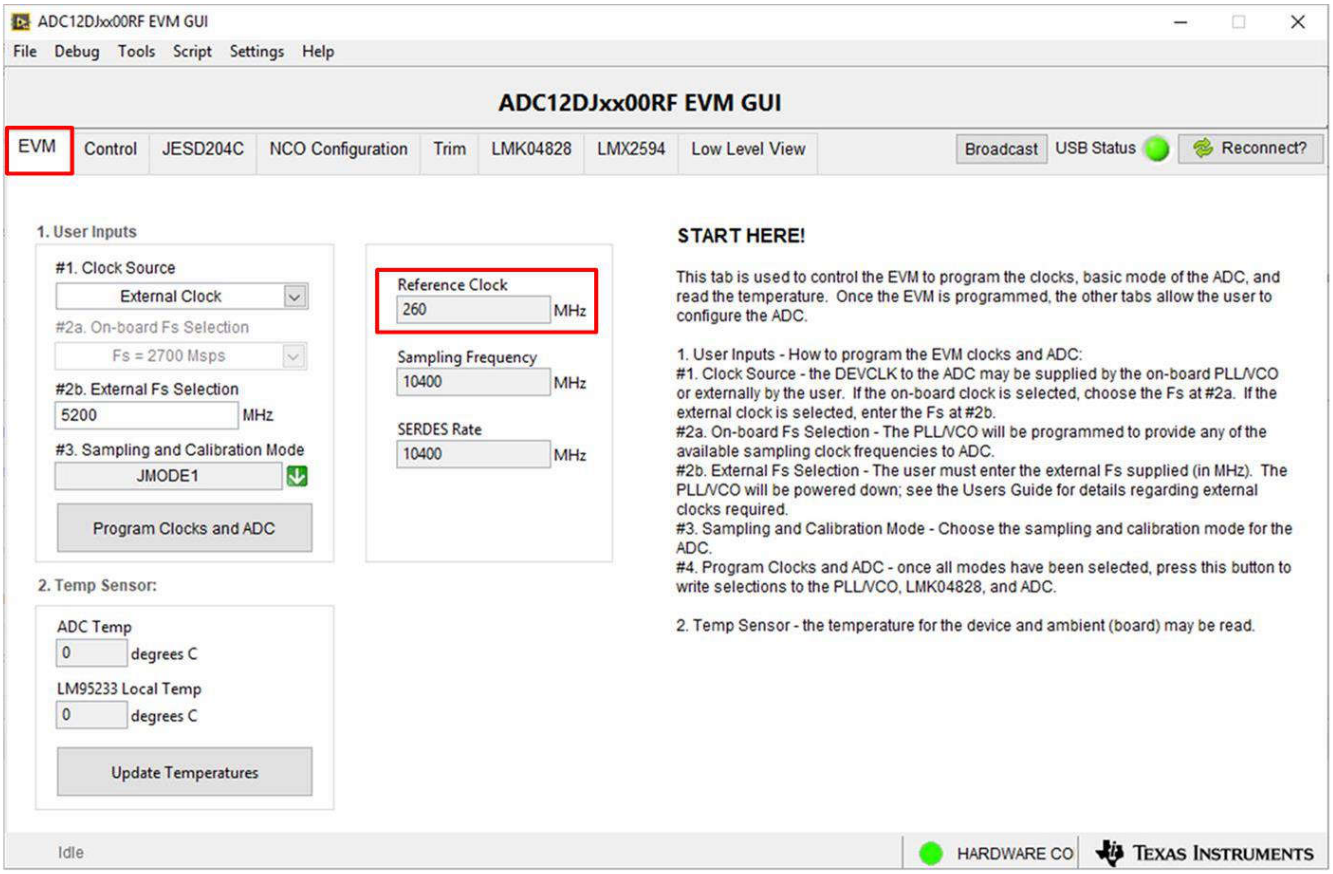
a. The Reference clock frequency can be obtained from the ADC12DJ5200RFEVM GUI. Once the ADC12DJ5200EVM GUI is configured to the desired JMODE mode and clock rate. The Reference Clock frequency required by the EVM is displayed on first page of the GUI.
b. Ensure that the DEVCLK and Reference clock sources are frequency-locked using a common 10-MHz reference to ensure functionality. Frequency locking the input signal generator to the other generators can also be done if coherent sampling is desired.
c. Do not turn on the RF output of any signal generator at this time.
d. When using the ADC in single-input mode, the device uses both edges of DEVCLK for sampling.

ADC Software Setup

The Device Configuration GUI is installed separately from the HSDC Pro installation and is a stand-alone GUI.

Note

The max clock rate supported by ADC12DJ4000RF is 4000MHz and only 8-bit mode are supported by ADC08DJ5200RF. All the 12-bit and 15-bit modes are disabled on ADC08DJ5200RF.



1. User Inputs

#1. Clock Source: External Clock

#2a. On-board Fs Selection: Fs = 2700 Msps

#2b. External Fs Selection: 5200 MHz

#3. Sampling and Calibration Mode: JMODE1

Reference Clock: 260 MHz

Sampling Frequency: 10400 MHz

SERDES Rate: 10400 MHz

2. Temp Sensor:

ADC Temp: 0 degrees C

LM95233 Local Temp: 0 degrees C

START HERE!

This tab is used to control the EVM to program the clocks, basic mode of the ADC, and read the temperature. Once the EVM is programmed, the other tabs allow the user to configure the ADC.

1. User Inputs - How to program the EVM clocks and ADC:
#1. Clock Source - the DEVCLK to the ADC may be supplied by the on-board PLL/VCO or externally by the user. If the on-board clock is selected, choose the Fs at #2a. If the external clock is selected, enter the Fs at #2b.
#2a. On-board Fs Selection - The PLL/VCO will be programmed to provide any of the available sampling clock frequencies to ADC.
#2b. External Fs Selection - The user must enter the external Fs supplied (in MHz). The PLL/VCO will be powered down; see the Users Guide for details regarding external clocks required.
#3. Sampling and Calibration Mode - Choose the sampling and calibration mode for the ADC.
#4. Program Clocks and ADC - once all modes have been selected, press this button to write selections to the PLL/VCO, LMK04828, and ADC.

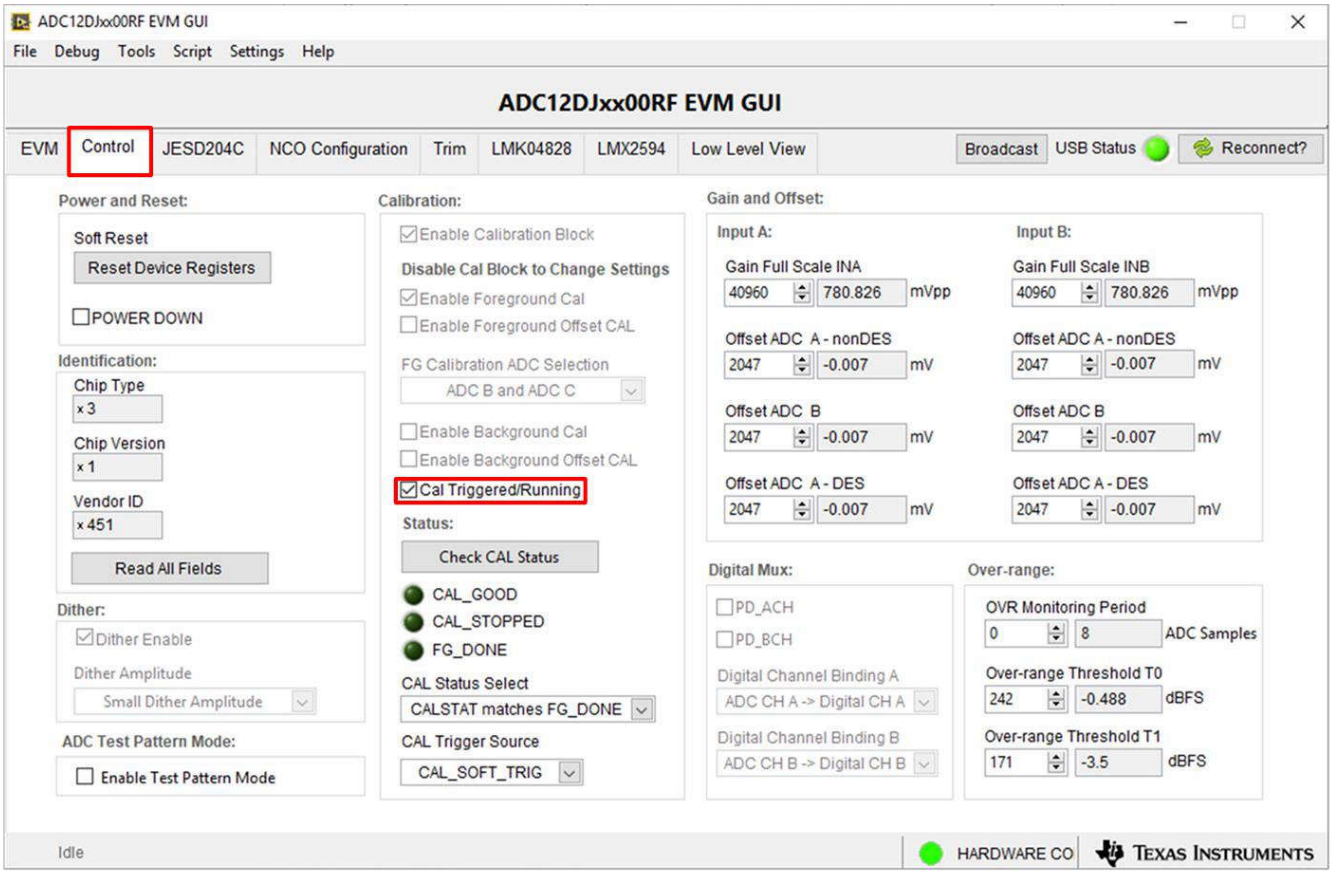
2. Temp Sensor - the temperature for the device and ambient (board) may be read.

Figure 3-2. Configuration GUI EVM Tab

Figure 3-2 shows the GUI open to the *EVM* tab and *Control* tab respectively. Tabs at the top of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has four configurable devices, namely the ADC12DJ5200RF, LMK04828, LMK61E2, and LMX2594.

1. Open the ADC12DJ5200RFEVM GUI.
2. Select the external clock as the clock source.
3. Enter Fs = 5200MHz MSPS as the external Fs selection.
4. Select JMODE1 for the sampling and Calibration mode.
5. Click *Program Clocks and ADC* (Note: This action will overwrite any previous device register settings.)
6. The Reference frequency required by the EVM is shown under indicator Reference Clock.

Calibrate the ADC Device on the EVM



Power and Reset:
☐ POWER DOWN

Identification:
Chip Type: x3
Chip Version: x1
Vendor ID: x451

Dither:
☑ Dither Enable
Dither Amplitude: Small Dither Amplitude

ADC Test Pattern Mode:
☐ Enable Test Pattern Mode

Calibration:
☑ Enable Calibration Block
☑ Enable Foreground Cal
☐ Enable Foreground Offset CAL
FG Calibration ADC Selection: ADC B and ADC C
☐ Enable Background Cal
☐ Enable Background Offset CAL
☑ Cal Triggered/Running
CAL Status Select: CALSTAT matches FG_DONE
CAL Trigger Source: CAL_SOFT_TRIG

Input A:
Gain Full Scale INA: 40960 780.826 mVpp
Offset ADC A - nonDES: 2047 -0.007 mV
Offset ADC B: 2047 -0.007 mV
Offset ADC A - DES: 2047 -0.007 mV

Input B:
Gain Full Scale INB: 40960 780.826 mVpp
Offset ADC A - nonDES: 2047 -0.007 mV
Offset ADC B: 2047 -0.007 mV
Offset ADC A - DES: 2047 -0.007 mV

Digital Mux:
☐ PD_ACH
☐ PD_BCH
Digital Channel Binding A: ADC CH A -> Digital CH A
Digital Channel Binding B: ADC CH B -> Digital CH B

Over-range:
OVR Monitoring Period: 0 8 ADC Samples
Over-range Threshold T0: 242 -0.488 dBFS
Over-range Threshold T1: 171 -3.5 dBFS

Figure 3-3. Configuration GUI ADC Control

1. With the EVM GUI open on the PC, navigate to the *Control* tab.
2. To calibrate the ADC, click *Cal Triggered/Running* once, then click it again. This stops and re-starts the Calibration engine.
3. To enable background calibration, use the following steps:
    - Navigate to the *JESD204C* tab and click on *JESD Block Enable* to stop the JESD204C block.
    - Navigate back to the *Control* tab and click on *Enable Calibration Block* to disable calibration and allow setting changes.
    - Click on *Enable Background Cal*.If background offset calibration is desired also, click on *Enable Background Offset Cal*.
    - Click on *Enable Calibration Block* to re-enable the calibration subsystemNavigate to the *JESD204C* tab and click on *JESD Block Enable* to re-start the JESD204C block.
    - Navigate back to the *Control* tab and click the *Cal Triggered/Running* button once, then click it again. This restarts the Calibration engine.

4. To disable background calibration, use the following steps:
    - Navigate to the *JESD204C* tab and click on *JESD Block Enable* to stop the JESD204C block.
    - Navigate back to the *Control* tab and click on *Enable Calibration Block* to disable calibration and allow setting changes.
    - If background offset calibration was enabled, click on *Enable Background Offset Cal* to disable the feature.
    - Click on *Enable Background Cal* to disable the feature.
    - Click on *Enable Calibration Block* to re-enable the calibration subsystem.
    - Navigate to the *JESD204C* tab and click on *JESD Block Enable* to re-start the JESD204C block.
    - Navigate back to the *Control* tab and click the *Cal Triggered/Running* button once, then click it again. This restarts the Calibration engine.

Capture Data Using the HSDC Pro Software

Open the HSDC Software and Load the FPGA Image to the TSW14J57EVM

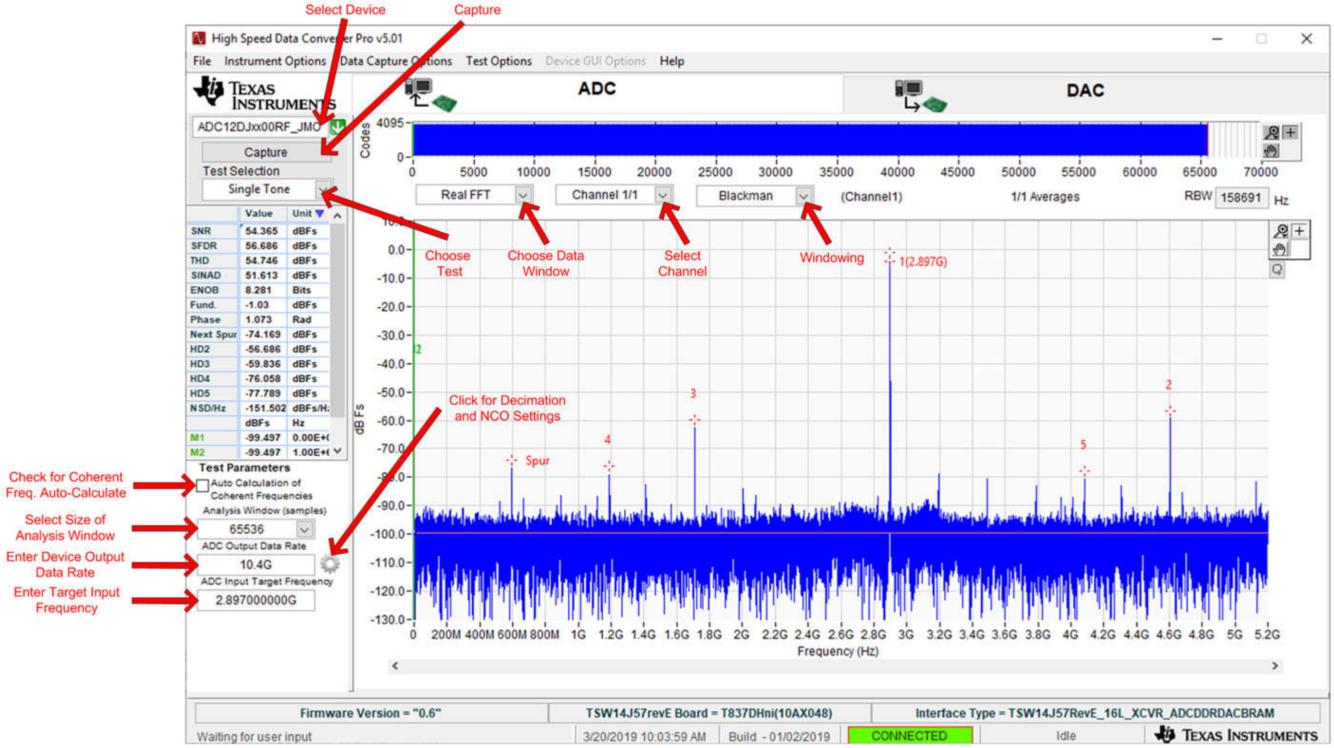
1. Open the HSDC Pro software.
2. Click *OK* to confirm the serial number of the TSW14J57EVM device. If multiple TSWxxxxx boards are connected, select the model and serial number for the one connected to the ADC12DJ5200RFEVM.
3. Select the ADC12DJxx00RF_JMODE1 device from the ADC select drop-down in the top left corner.
4. When prompted, click *Yes* to update the firmware.
5. Enter the ADC Output Data Rate ($f_{(SAMPLE)}$) as "10400M" or the desired output sample rate. This number must be equal to the actual sampling rate of the device and must be updated if the sampling rate changes.

The following steps show how to capture data using the HSDC Pro software:

1. Select the test to perform.
2. Select the data view.
3. Select the channel to view.
4. Click the capture button to capture new data.

Additional tips:

- Use the *Notch Frequency Bins* from the *Test Options* file menu to remove bins around DC (eliminate DC noise and offset) or the fundamental (eliminate phase noise from signal generators).
- Open the *Capture Option* dialog from the *Data Capture Options* file menu to change the capture depth or to enable Continuous Capture or FFT averaging.
- For analyzing only a portion of the spectrum, use the *Single Tone* test with the *Bandwidth Integration Markers* from the *Test Options* file menu. The *Channel Power* test is also useful.
- For analyzing only a subset of the captured data, set the *Analysis Window (samples)* setting to a value less than the number of total samples captured and move the green or red markers in the small transient data window at the top of the screen to select the data subset of interest.



ADC12DJxx00RF_JMO

Test Selection: Single Tone

Real FFT | Channel 1/1 | Blackman | (Channel1) | 1/1 Averages | RBW 158691 Hz

	Value	Unit
SNR	54.365	dBFs
SFDR	56.686	dBFs
THD	54.746	dBFs
SINAD	51.613	dBFs
ENOB	8.281	Bits
Fund.	-1.03	dBFs
Phase	1.073	Rad
Next Spur	-74.169	dBFs
HD2	-56.686	dBFs
HD3	-59.836	dBFs
HD4	-76.058	dBFs
HD5	-77.789	dBFs
NSD/Hz	-151.502	dBFs/H:
	dBFs	Hz
M1	-99.497	0.00E+(
M2	-99.497	1.00E+(

Test Parameters

☐ Auto Calculation of Coherent Frequencies

Analysis Window (samples): 65536

ADC Output Data Rate: 10.4G

ADC Input Target Frequency: 2.897000000G

Firmware Version = "0.6" | TSW14J57revE Board = T837DHni(10AX048) | Interface Type = TSW14J57RevE_16L_XCVR_ADCDDRDACBRAM

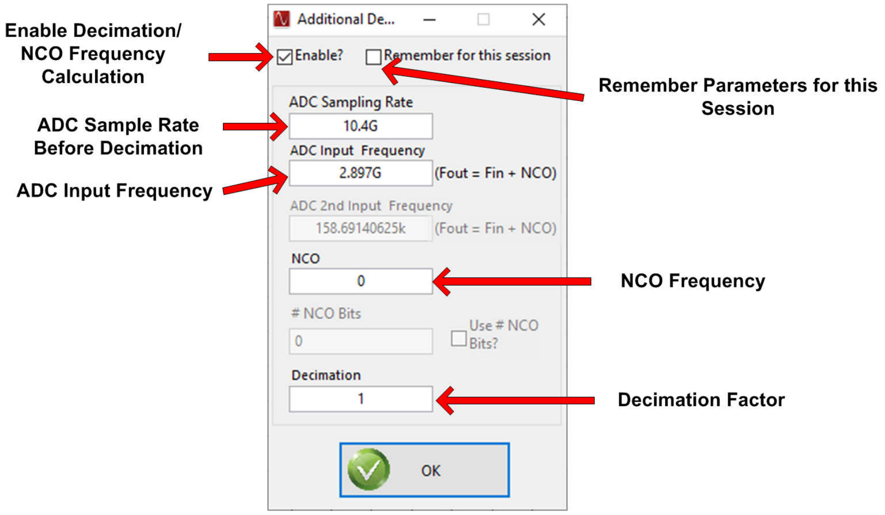
Waiting for user input | 3/20/2019 10:03:59 AM | Build - 01/02/2019 | CONNECTED | Idle

Figure 3-4. High Speed Data Converter Pro (HSDC) GUI

When using decimation and NCO features, click the gear symbol to access the *Additional Device Parameters* dialog box to enter the following details:

1. ADC Sampling Rate
2. ADC Input Signal Frequency
3. NCO Frequency
4. Decimation Factor

The HSDC Pro GUI calculates the *ADC Output Data Rate* based on these inputs. The *Fundamental and Harmonic* frequency locations are also calculated and identified in the FFT display.



☑ Enable? ☐ Remember for this session

ADC Sampling Rate: 10.4G

ADC Input Frequency: 2.897G (Fout = Fin + NCO)

ADC 2nd Input Frequency: 158.69140625k (Fout = Fin + NCO)

NCO: 0

NCO Bits: 0 ☐ Use # NCO Bits?

Decimation: 1

Figure 3-5. Additional Device Parameters Dialog Box

3.2.2 AFE Hardware Setup & Configuration

The TIDA-010133 reference design hardware has a few user selectable hardware configurations available to the user via jumpers headers. The jumpers primarily configure the programmability of the hardware. This includes the option to communicate with the hardware with either an onboard FTDI device or through SPI/I2C with a USB2ANY module. The following table shows the onboard devices and the communication interface used to communicate with each device.

Table 3-1. Device Interface

Device	Communication Interface
LMH6518	SPI
DAC80508	SPI
TPL0102	I2C

There are 7 jumper headers; 3 for the LMH6518, 2 for the DAC80508, 2 for the I2C TMUX121 interface.

The LMH6518 uses jumpers J18, J19, and J24 for it's configuration. J18 is used to select which channel device (1 or 2) to communicate with when using the USB2ANY. J19 is used to switch the interface between the FTDI and USB2ANY. J24 is used to enable or disable the mutiplexer used for the switching between FTDI and USB2ANY, the multiplexer enable pin is active low.

Table 3-2. LMH6518 Configuration

J18	J19	J24	Programming
x	0	0	FTDI
0	1	0	Channel 1 (USB2ANY)
1	1	0	Channel 2 (USB2ANY)
X	X	1	Disabled

The DAC80508 uses J25 and J27 for the configuration. J25 is to switch between the FTDI and USB2ANY communication interface. J27 is used to enable or disable the second multiplexer for the DAC.

Table 3-3. DAC80508 Configuration

J25	J27	Programming
0	0	FTDI
1	0	USB2ANY
X	1	Disabled

J31 is used to select I2C interface from FTDI or USB2ANY and J32 is to enable/disable the Multiplexer.

Table 3-4. I2C Source Selection

J31	J32	Programming
0	0	FTDI
1	0	USB2ANY
X	1	Disabled

J17 is used to provide the FTDI device a 3.3V input. The two available options are either from the onboard 3.3V power rail or from the USB V_{BUS}.

Table 3-5. FTDI 3P3V Supply Source

J17	VREGIN Source
1-2	+3P3VD Power Rail
2-3	V_{BUS} from connected USB

To power up the board, it requires a 12V, 500mA supply at J5 with ground connected at J30. The USB2ANY ribbon cable is connected on J16 header with pin 1 (red strip) facing bottom left. Once the power is provided the green LED will light up as shown in the figure below.

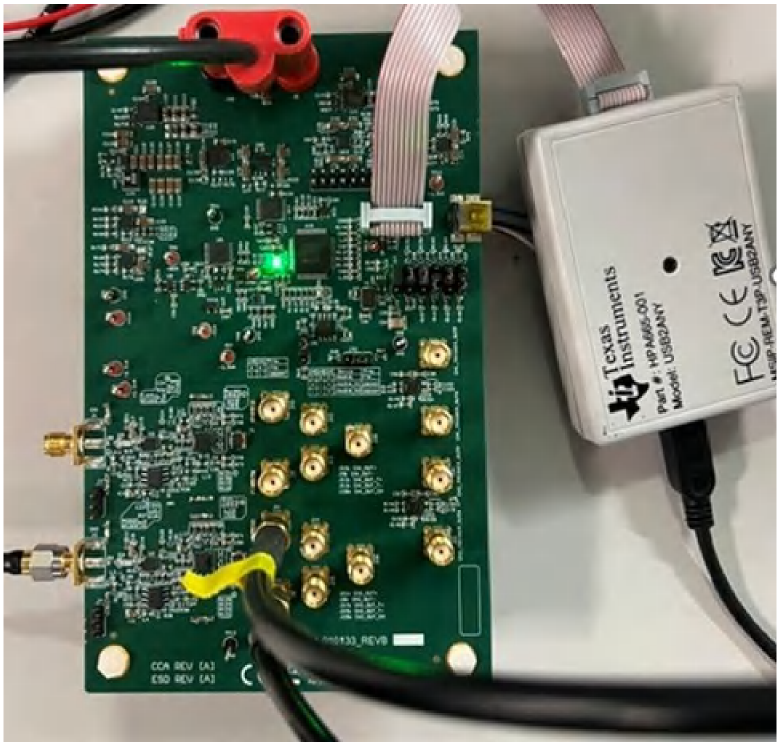


Figure 3-6. AFE Board Setup

3.2.2.1 Device Programming

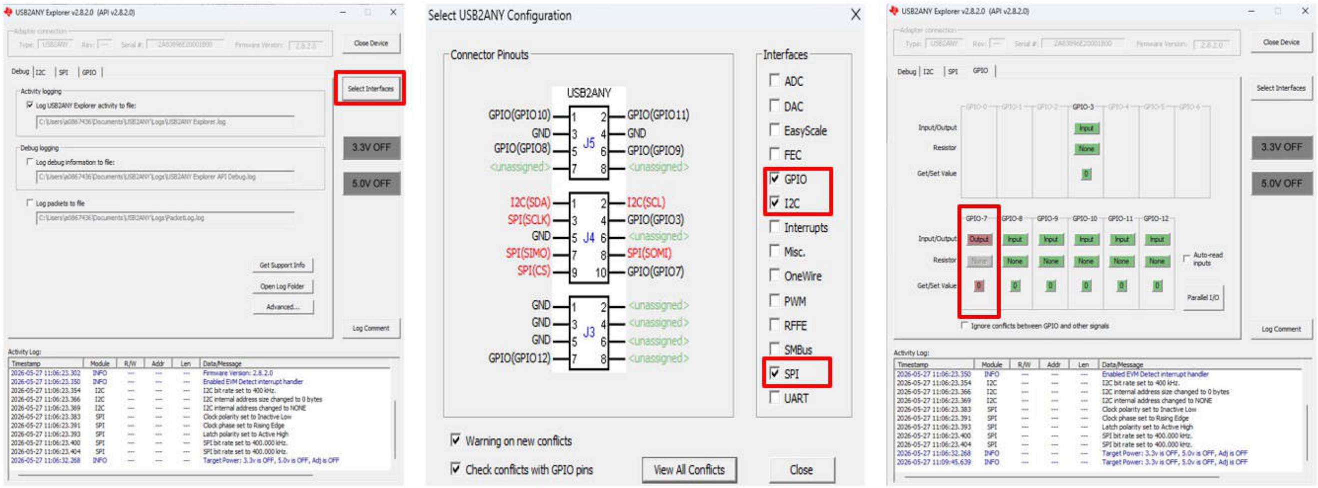
The USB2ANY module is the recommended method of programming the controllable devices on the board. There is a dedicated connector, J16, to connect the USB2ANY module. In addition, there is a FDTI IC, FT4232, that users can also use to program the board.

Figure 3-7. USB2ANY

The LMH6518 and DAC805058 both have an available GUI/Software package to allow for user programmability. The following steps provide the link from where each software can be downloaded from.

1. **Install the LMH6518 GUI**
   a. Download the most recent version of the LMH65618 GUI from https://www.ti.com/product/LMH6518.
   b. Follow the installation instructions to install the GUI.
   c. Read the Users Guide for more information on how to program the LMH6518 via the GUI.
2. **Install the DAC80505 GUI**
   a. Download the most recent version of the DAC80508 software package from https://www.ti.com/tool/DAC80508EVM.
   b. Follow the installation instructions to install the software.
3. **Install the USB2ANY**
   a. Download the most recent version of the USB2ANY Explorer software package from https://www.ti.com/tool/USB2ANY.
   b. Follow the installation instructions to install the software.
   c. Read the Users Guide for more information on using the USB2ANY module to program the devices.

Once the USB2ANY explorer is installed, open and configure the interface as follows:



Click "Select Interface"

Select GPIO, I2C and SPI

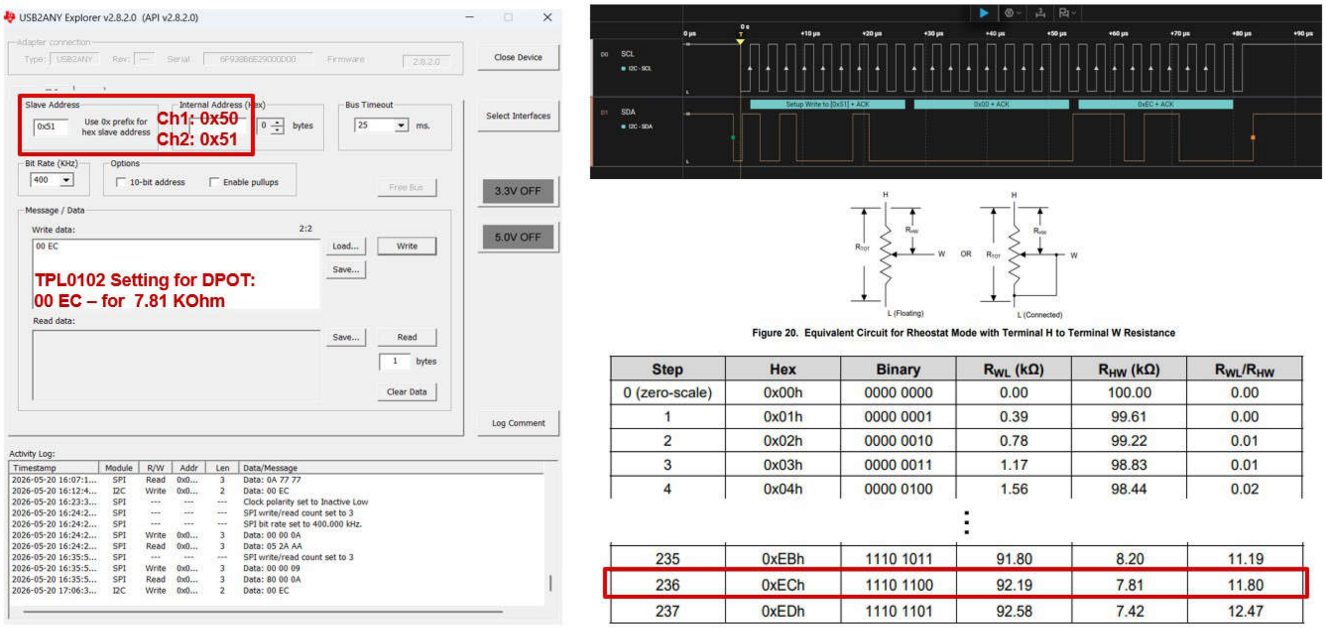
GPIO7 – U2A_SDIO_SEL Setting:

- Set to "0" for LMH6518 MOSI
- Set to "1" for LMH6518 MISO

Figure 3-8. USB2ANY Interface Setting

To configure the TPL0102 DPOT for Chx_ACDC_GAINADJ with I2C interface, the following is an example of an I2C transaction with the USB2ANY Explorer GUI.

As there are 2 different channels, enter the I2C address accordingly in the I2C Address entry. For channel 1, the address is 0x50 and for channel 2 the address is 0x51 as shown:



Slave Address: 0x51

Internal Address (Hex): 0 bytes

Bus Timeout: 25 ms.

Bit Rate (KHz): 400

Write data: 00 EC

Ch1: 0x50
Ch2: 0x51

TPL0102 Setting for DPOT:
00 EC – for 7.81 KOhm

Activity Log:

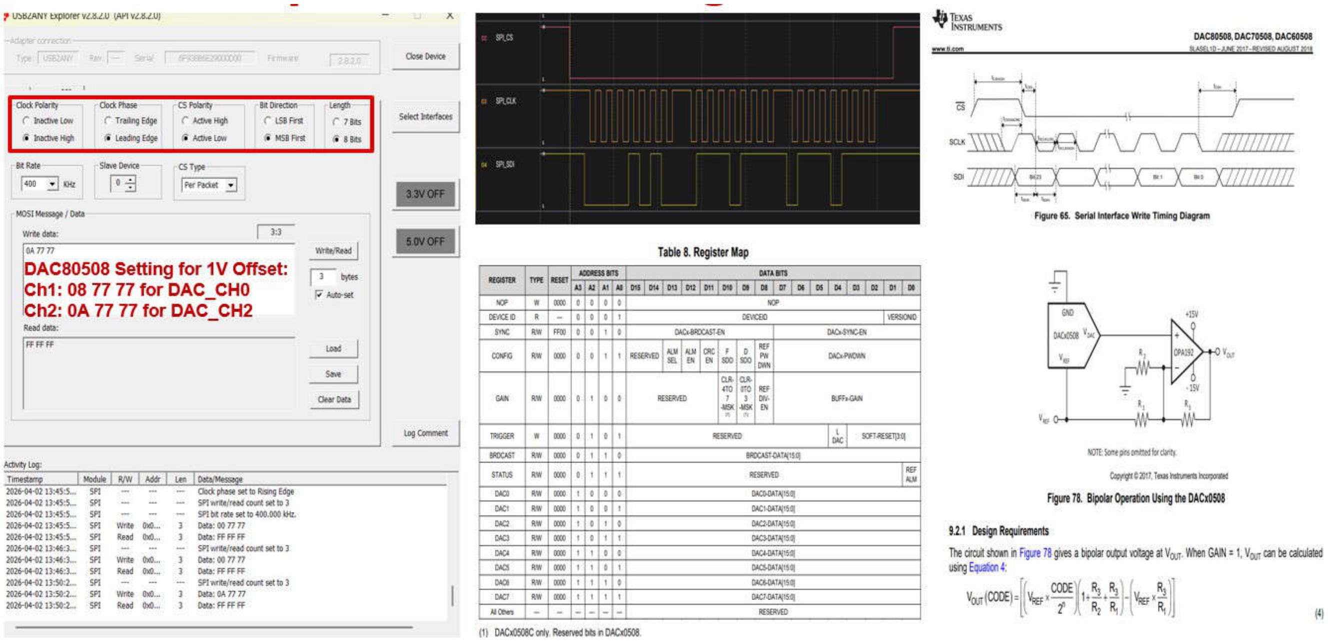
```
Timestamp              Module  R/W    Addr    Len  Data/Message
2026-05-20 16:07:1...  SPI     Read   0x0...  3    Data: 0A 77 77
2026-05-20 16:12:4...  I2C     Write  0x0...  2    Data: 00 EC
2026-05-20 16:23:3...  SPI     ---    ---     ---  Clock polarity set to Inactive Low
2026-05-20 16:24:2...  SPI     ---    ---     ---  SPI write/read count set to 3
2026-05-20 16:24:2...  SPI     ---    ---     ---  SPI bit rate set to 400.000 kHz.
2026-05-20 16:24:2...  SPI     Write  0x0...  3    Data: 00 00 0A
2026-05-20 16:24:2...  SPI     Read   0x0...  3    Data: 05 2A AA
2026-05-20 16:35:5...  SPI     ---    ---     ---  SPI write/read count set to 3
2026-05-20 16:35:5...  SPI     Write  0x0...  3    Data: 00 00 09
2026-05-20 16:35:5...  SPI     Read   0x0...  3    Data: 80 00 0A
2026-05-20 17:06:3...  I2C     Write  0x0...  2    Data: 00 EC
```

Figure 20. Equivalent Circuit for Rheostat Mode with Terminal H to Terminal W Resistance

Step	Hex	Binary	R_{WL} (kΩ)	R_{HW} (kΩ)	R_{WL}/R_{HW}
0 (zero-scale)	0x00h	0000 0000	0.00	100.00	0.00
1	0x01h	0000 0001	0.39	99.61	0.00
2	0x02h	0000 0010	0.78	99.22	0.01
3	0x03h	0000 0011	1.17	98.83	0.01
4	0x04h	0000 0100	1.56	98.44	0.02
⋮					
235	0xEBh	1110 1011	91.80	8.20	11.19
236	0xECh	1110 1100	92.19	7.81	11.80
237	0xEDh	1110 1101	92.58	7.42	12.47

Figure 3-9. TPL0102 I2C Transaction Example

For configuring CHx-OFFSET of DAC80508 through SPI interface, the following example shows the interface settings. As these offsets are provided by DAC channel 0 (DAC0-DATA) for channel 1 and DAC channel 2 (DAC2-DATA) for channel 2, the SPI address bit is set accordingly per the DAC80508 Table 8. Register Map of the data sheet. DAC1-DATA and DAC3-DATA are for the channel's calibration path. The code for the DAC conversion is given in the datasheet equation 4 also shown in the example below.



USB2ANY Explorer v2.8.2.0 (API v2.8.2.0)

Clock Polarity: ○ Inactive Low ● Inactive High
Clock Phase: ○ Trailing Edge ● Leading Edge
CS Polarity: ○ Active High ● Active Low
Bit Direction: ○ LSB First ● MSB First
Length: ○ 7 Bits ● 8 Bits
Bit Rate: 400 KHz
Slave Device: 0
CS Type: Per Packet

MOSI Message / Data
Write data: 0A 77 77 (3:3)

DAC80508 Setting for 1V Offset:
Ch1: 08 77 77 for DAC_CH0
Ch2: 0A 77 77 for DAC_CH2

Read data: FF FF FF
3 bytes ☑ Auto-set

Activity Log:

```
Timestamp            Module  R/W    Addr   Len  Data/Message
2026-04-02 13:45:5...  SPI    ---    ---    ---  Clock phase set to Rising Edge
2026-04-02 13:45:5...  SPI    ---    ---    ---  SPI write/read count set to 3
2026-04-02 13:45:5...  SPI    ---    ---    ---  SPI bit rate set to 400.000 kHz.
2026-04-02 13:45:5...  SPI    Write  0x0...  3   Data: 00 77 77
2026-04-02 13:45:5...  SPI    Read   0x0...  3   Data: FF FF FF
2026-04-02 13:46:3...  SPI    ---    ---    ---  SPI write/read count set to 3
2026-04-02 13:46:3...  SPI    Write  0x0...  3   Data: 00 77 77
2026-04-02 13:46:3...  SPI    Read   0x0...  3   Data: FF FF FF
2026-04-02 13:50:2...  SPI    ---    ---    ---  SPI write/read count set to 3
2026-04-02 13:50:2...  SPI    Write  0x0...  3   Data: 0A 77 77
2026-04-02 13:50:2...  SPI    Read   0x0...  3   Data: FF FF FF
```

Figure 65. Serial Interface Write Timing Diagram

Table 8. Register Map

REGISTER	TYPE	RESET	ADDRESS BITS				DATA BITS															
			A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NOP	W	0000	0	0	0	0	NOP															
DEVICE ID	R	—	0	0	0	1	DEVICEID														VERSIONID	
SYNC	R/W	FF00	0	0	1	0	DACx-BRDCAST-EN								DACx-SYNC-EN							
CONFIG	R/W	0000	0	0	1	1	RESERVED		ALM SEL	ALM EN	CRC EN	F SDO	D SDO	REF PWDWN	DACx-PWDWN							
GAIN	R/W	0000	0	1	0	0	RESERVED					CLR-4TO7-MSK (1)	CLR-0TO3-MSK (1)	REF-DIV-EN	BUFFx-GAIN							
TRIGGER	W	0000	0	1	0	1	RESERVED											LDAC	SOFT-RESET[3:0]			
BRDCAST	R/W	0000	0	1	1	0	BRDCAST-DATA[15:0]															
STATUS	R/W	0000	0	1	1	1	RESERVED															REF ALM
DAC0	R/W	0000	1	0	0	0	DAC0-DATA[15:0]															
DAC1	R/W	0000	1	0	0	1	DAC1-DATA[15:0]															
DAC2	R/W	0000	1	0	1	0	DAC2-DATA[15:0]															
DAC3	R/W	0000	1	0	1	1	DAC3-DATA[15:0]															
DAC4	R/W	0000	1	1	0	0	DAC4-DATA[15:0]															
DAC5	R/W	0000	1	1	0	1	DAC5-DATA[15:0]															
DAC6	R/W	0000	1	1	1	0	DAC6-DATA[15:0]															
DAC7	R/W	0000	1	1	1	1	DAC7-DATA[15:0]															
All Others	—	—	—	—	—	—	RESERVED															

(1) DACx0508C only. Reserved bits in DACx0508.

NOTE: Some pins omitted for clarity.

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Figure 78. Bipolar Operation Using the DACx0508

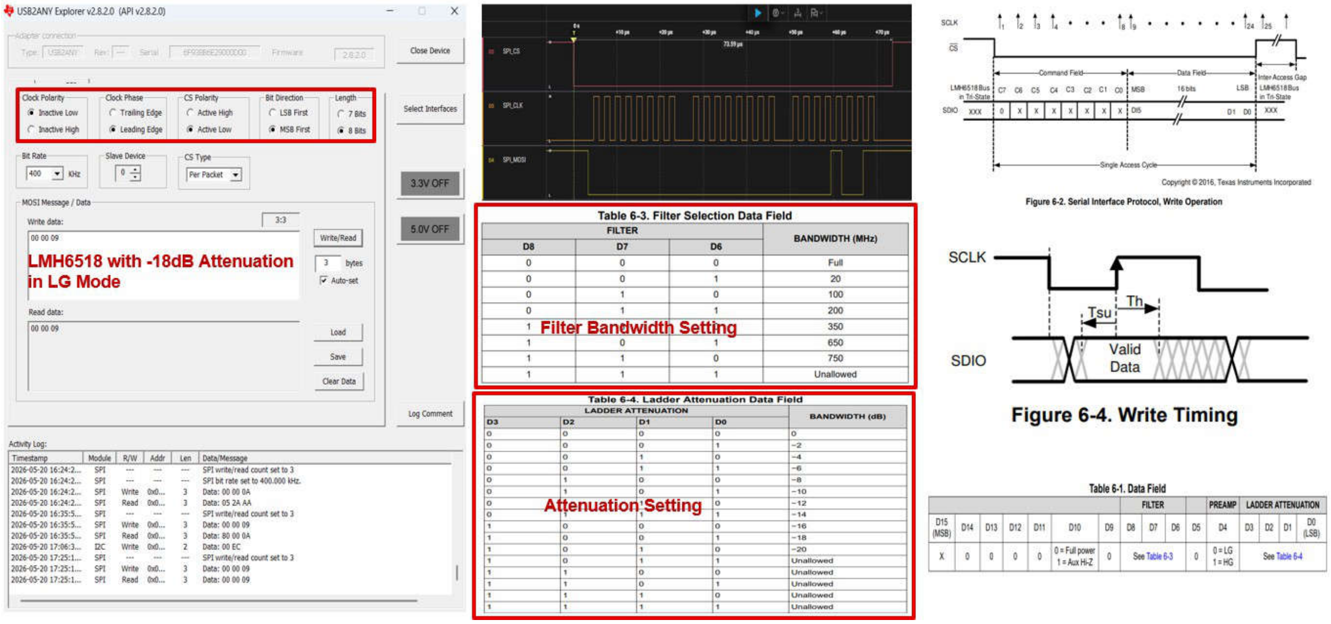
9.2.1 Design Requirements

The circuit shown in Figure 78 gives a bipolar output voltage at V_{OUT}. When GAIN = 1, V_{OUT} can be calculated using Equation 4:

$$V_{OUT}(CODE) = \left[\left(V_{REF} \times \frac{CODE}{2^n}\right)\left(1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}\right) - \left(V_{REF} \times \frac{R_3}{R_1}\right)\right] \quad (4)$$

Figure 3-10. DAC80508 SPI Interface Example

The LMH6518 VGA device is configurable through SPI interface and an example to set the gain is shown below. The field for the data is provided in Figure 3-11 in the datasheet.



USB2ANY Explorer v2.8.2.0 (API v2.8.2.0)

Clock Polarity: ● Inactive Low ○ Inactive High
Clock Phase: ○ Trailing Edge ● Leading Edge
CS Polarity: ○ Active High ● Active Low
Bit Direction: ○ LSB First ● MSB First
Length: ○ 7 Bits ● 8 Bits
Bit Rate: 400 KHz
Slave Device: 0
CS Type: Per Packet

MOSI Message / Data
Write data: 00 00 09 (3:3)

LMH6518 with -18dB Attenuation in LG Mode

Read data: 00 00 09
3 bytes ☑ Auto-set

Activity Log:

```
Timestamp            Module  R/W    Addr   Len  Data/Message
2026-05-20 16:24:2...  SPI    ---    ---    ---  SPI write/read count set to 3
2026-05-20 16:24:2...  SPI    ---    ---    ---  SPI bit rate set to 400.000 kHz.
2026-05-20 16:24:2...  SPI    Write  0x0...  3   Data: 00 00 0A
2026-05-20 16:24:2...  SPI    Read   0x0...  3   Data: 05 2A AA
2026-05-20 16:35:5...  SPI    ---    ---    ---  SPI write/read count set to 3
2026-05-20 16:35:5...  SPI    Write  0x0...  3   Data: 00 00 09
2026-05-20 16:35:5...  SPI    Read   0x0...  3   Data: 80 00 0A
2026-05-20 17:06:3...  I2C    Write  0x0...  2   Data: 00 EC
2026-05-20 17:25:1...  SPI    ---    ---    ---  SPI write/read count set to 3
2026-05-20 17:25:1...  SPI    Write  0x0...  3   Data: 00 00 09
2026-05-20 17:25:1...  SPI    Read   0x0...  3   Data: 00 00 09
```

Table 6-3. Filter Selection Data Field

FILTER			BANDWIDTH (MHz)
D8	D7	D6	
0	0	0	Full
0	0	1	20
0	1	0	100
0	1	1	200
1			350
1	0	1	650
1	1	0	750
1	1	1	Unallowed

Filter Bandwidth Setting

Table 6-4. Ladder Attenuation Data Field

LADDER ATTENUATION				BANDWIDTH (dB)
D3	D2	D1	D0	
0	0	0	0	0
0	0	0	1	−2
0	0	1	0	−4
0	0	1	1	−6
0	1	0	0	−8
0	1	0	1	−10
0		1	0	−12
0	1	1	1	−14
1	0	0	0	−16
1	0	0	1	−18
1	0	1	0	−20
1	0	1	1	Unallowed
1	1	0	0	Unallowed
1	1	0	1	Unallowed
1	1	1	0	Unallowed
1	1	1	1	Unallowed

Attenuation Setting

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Figure 6-2. Serial Interface Protocol, Write Operation

Figure 6-4. Write Timing

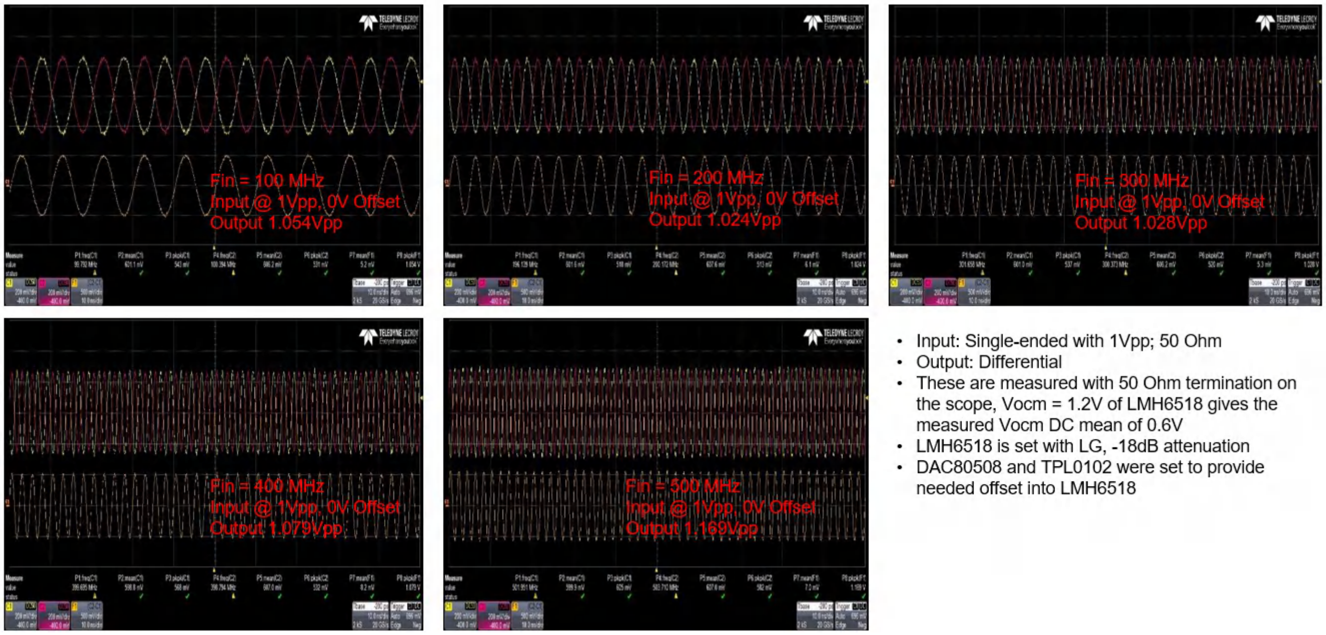
Table 6-1. Data Field

							FILTER				PREAMP	LADDER ATTENUATION			
D15 (MSB)	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
X	0	0	0	0	0 = Full power 1 = Aux Hi-Z	0	See Table 6-3			0	0 = LG 1 = HG	See Table 6-4			

Figure 3-11. LMH6518 SPI Interface Example

3.3 Test Results

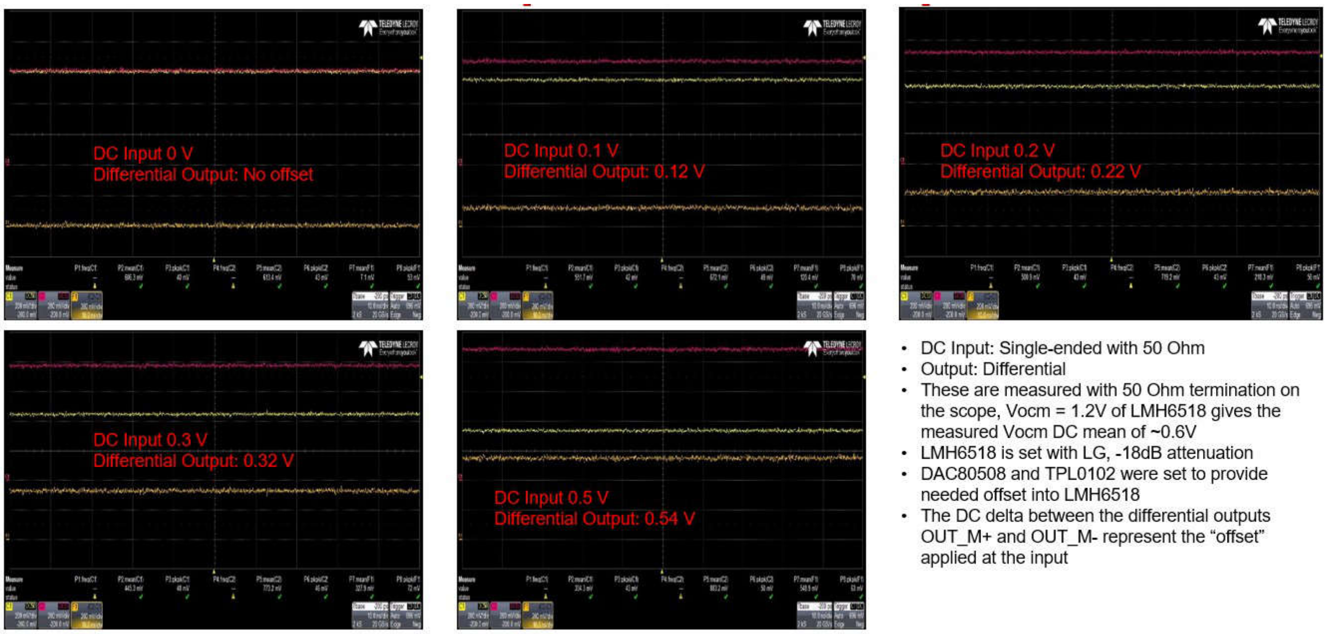
Test results taken with this reference design board are shown here. These are taken with the 50 Ohm input termination with AC and DC coupled.



- Input: Single-ended with 1Vpp; 50 Ohm
- Output: Differential
- These are measured with 50 Ohm termination on the scope, Vocm = 1.2V of LMH6518 gives the measured Vocm DC mean of 0.6V
- LMH6518 is set with LG, -18dB attenuation
- DAC80508 and TPL0102 were set to provide needed offset into LMH6518

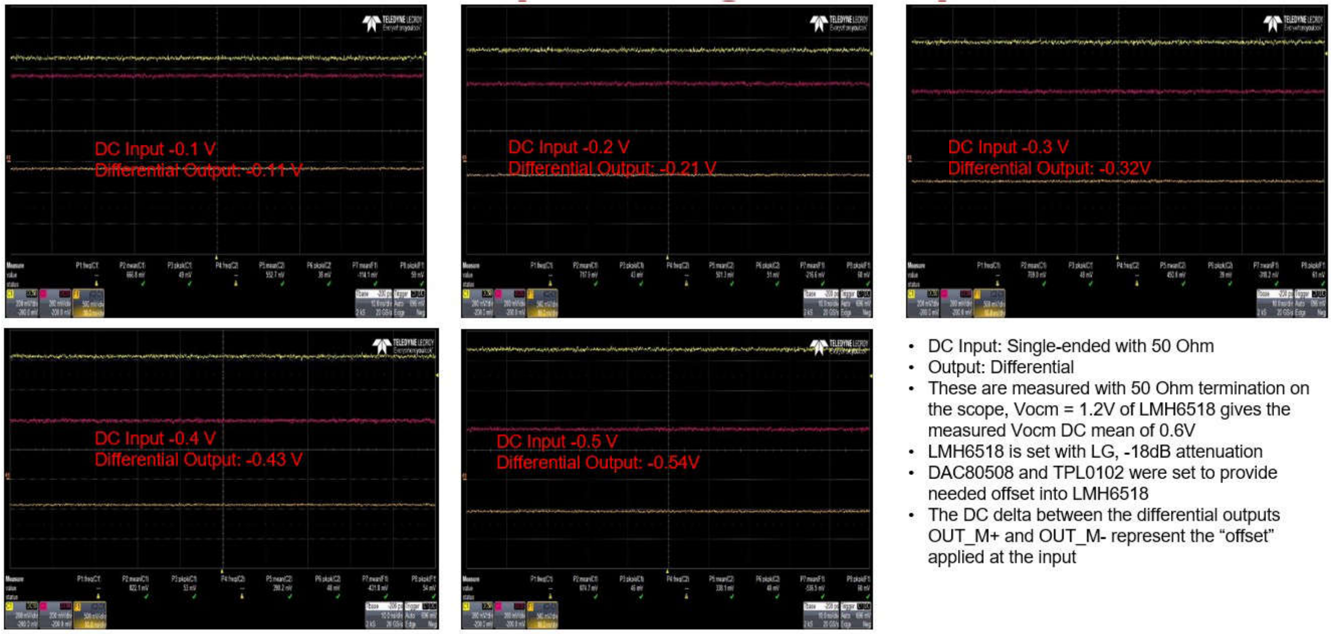
Figure 3-12. AC-Coupled at 1Vpp Input Across Frequency

On DC-Coupled, a DC input is provided at the input and the results of the differential output shows the respective DC output. A positive and negative DC inputs are tested and the polarity at the ouptut shows the respective input.



- DC Input: Single-ended with 50 Ohm
- Output: Differential
- These are measured with 50 Ohm termination on the scope, Vocm = 1.2V of LMH6518 gives the measured Vocm DC mean of ~0.6V
- LMH6518 is set with LG, -18dB attenuation
- DAC80508 and TPL0102 were set to provide needed offset into LMH6518
- The DC delta between the differential outputs OUT_M+ and OUT_M- represent the “offset” applied at the input

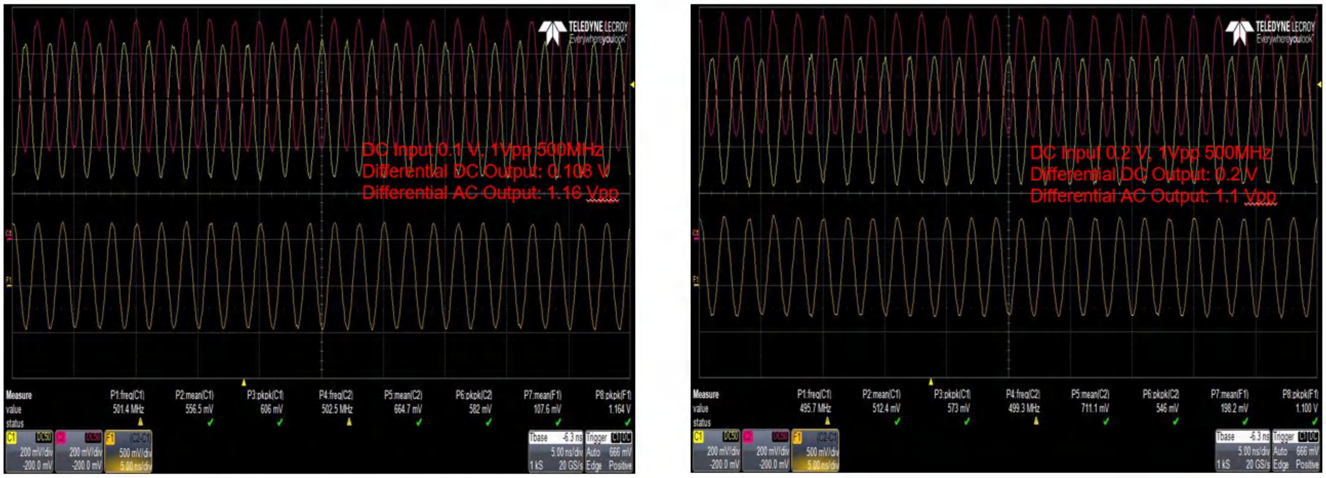
Figure 3-13. Positive DC-Coupled Input Case



- DC Input: Single-ended with 50 Ohm
- Output: Differential
- These are measured with 50 Ohm termination on the scope, Vocm = 1.2V of LMH6518 gives the measured Vocm DC mean of 0.6V
- LMH6518 is set with LG, -18dB attenuation
- DAC80508 and TPL0102 were set to provide needed offset into LMH6518
- The DC delta between the differential outputs OUT_M+ and OUT_M- represent the “offset” applied at the input

Figure 3-14. Negative DC-Coupled Input Case

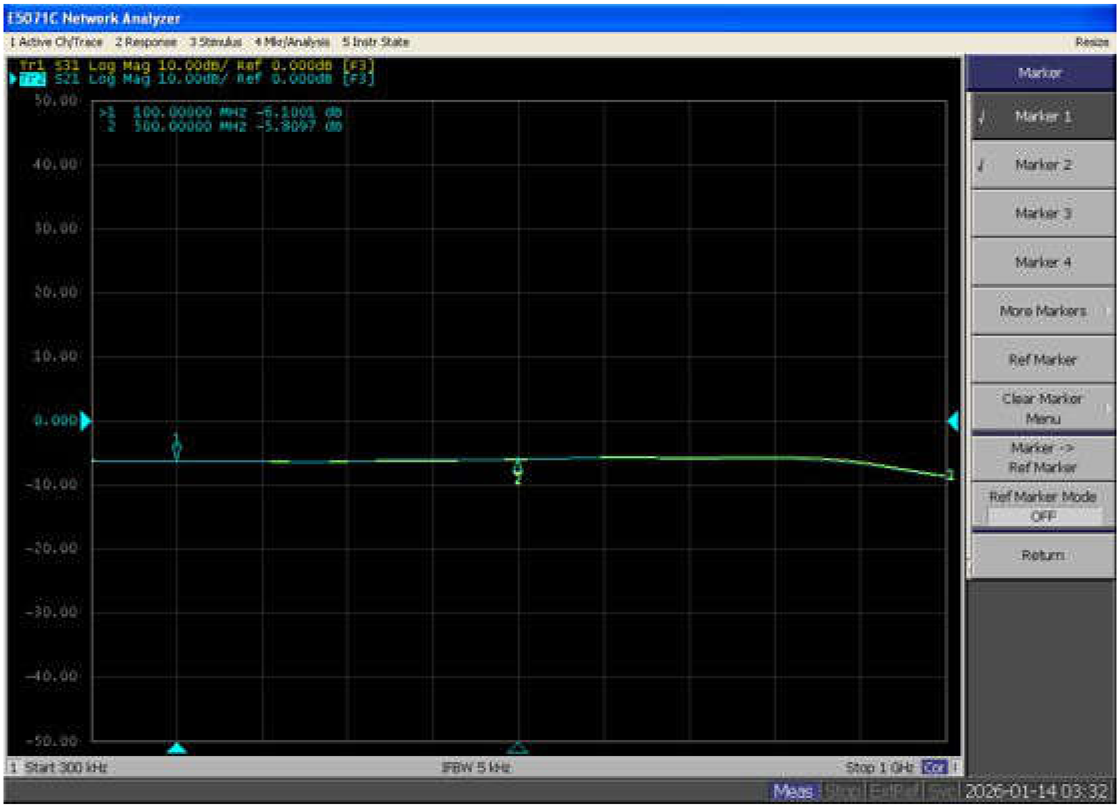
When DC input offset is injected with the AC signal, user needs to ensure the levels are within the LMH6518 output swing range. The input DC offset can be determine through the DAC80508 channel offset required to match the LMH6518 input common voltage. This level from the DAC80508 offset can be used in the post processing block to display the input offset. An example of an input of AC signal with DC offset is shown below.



- DC Input: Single-ended with 50 Ohm, 1Vpp 500MHz Signal
- Output: Differential
- These are measured with 50 Ohm termination on the scope, Vocm = 1.2V of LMH6518 gives the measured Vocm DC mean of ~0.6V
- LMH6518 is set with LG, -18dB attenuation
- DAC80508 and TPL0102 were set to provide needed offset into LMH6518
- The DC delta between the differential outputs OUT_M+ and OUT_M- represent the “offset” applied at the input

Figure 3-15. AC Signal with a DC Offset Input Case

A frequency sweep performance of this reference design is given below, which shows a flat response from DC to around 900MHz which is the bandwidth of the LMH6518. This is with 1Vpp single-ended input.



```
Tr1 S31 Log Mag 10.00dB/ Ref 0.000dB [F3]
Tr2 S21 Log Mag 10.00dB/ Ref 0.000dB [F3]
>1  100.00000 MHz -6.1001 dB
 2  500.00000 MHz -5.8097 dB
```

Figure 3-16. Frequency Sweep

The SNR measurements are taken with the 1Vpp level 500MHz signal and the noise power of the reference design when the input is terminated with 50Ω across the 500MHz span. The spectrum is shown below and the results is compared with the theoretical data.

Based on the Signal and Noise measurements below, the SNR is calculated below:

$$\mathrm{SE\ \ SNR} = -2.42\mathrm{dBm} - \left(-149.23\mathrm{dBm/Hz} + 10\mathrm{Log}_{10}\,5\mathrm{x}10^{8}\mathrm{Hz}\right) = 59.82\mathrm{dBm} \tag{5}$$

$$\mathrm{Diff\ \ SNR} = 59.82\mathrm{dBm} + 6\mathrm{dBm} = 65.82\mathrm{dBm} \tag{6}$$

The theoretical calculation based on signal of 0.5Vpp (0.177Vrms) and noise power from BUF802 (2.3nV/√Hz) and LMH6518 (1nV/√Hz) devices with filter correction factor of π/2, the SNR is calculated as follows:

$$\mathrm{N_{TOTAL}} = \sqrt{(2.3)^2 + (1)^2} * \sqrt{500\ \ \mathrm{MHz} * (\pi/2)} = 70\mu\mathrm{V} \tag{7}$$

$$\mathrm{SNR} = 20\mathrm{Log}_{10}(0.177\mathrm{V}/70\mu\mathrm{V}) = 68\mathrm{dB} \tag{8}$$

This shows a close matching with the measurement results.

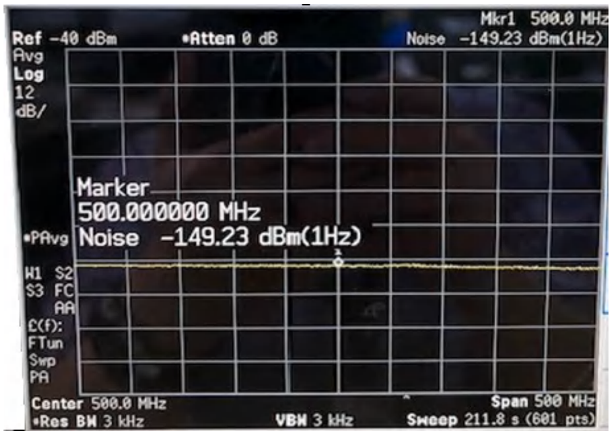


Figure 3-17. Signal and Noise Power Measurements (1)

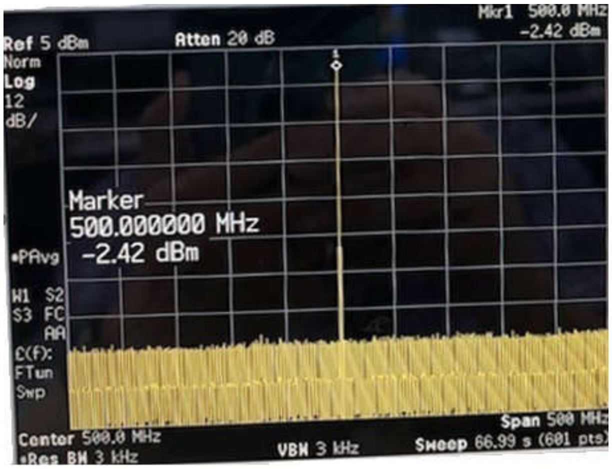


Figure 3-18. Signal and Noise Power Measurements (2)

The propagation delay of this reference design is measured with a fast rise time square wave input over two different levels and the results are shown below:

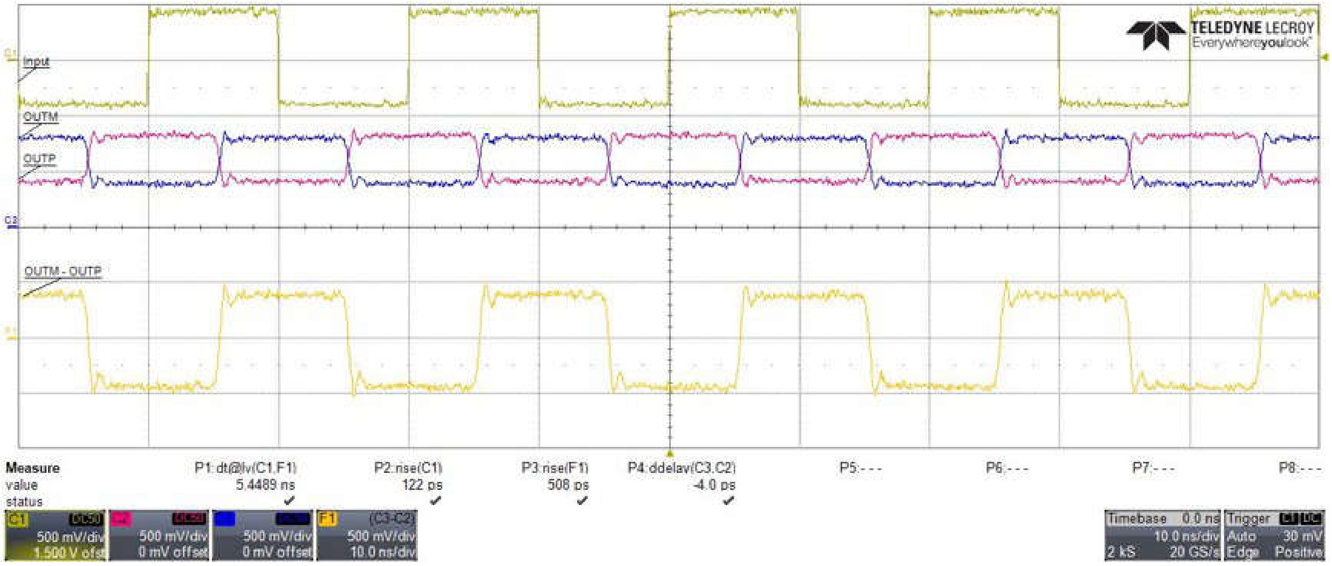
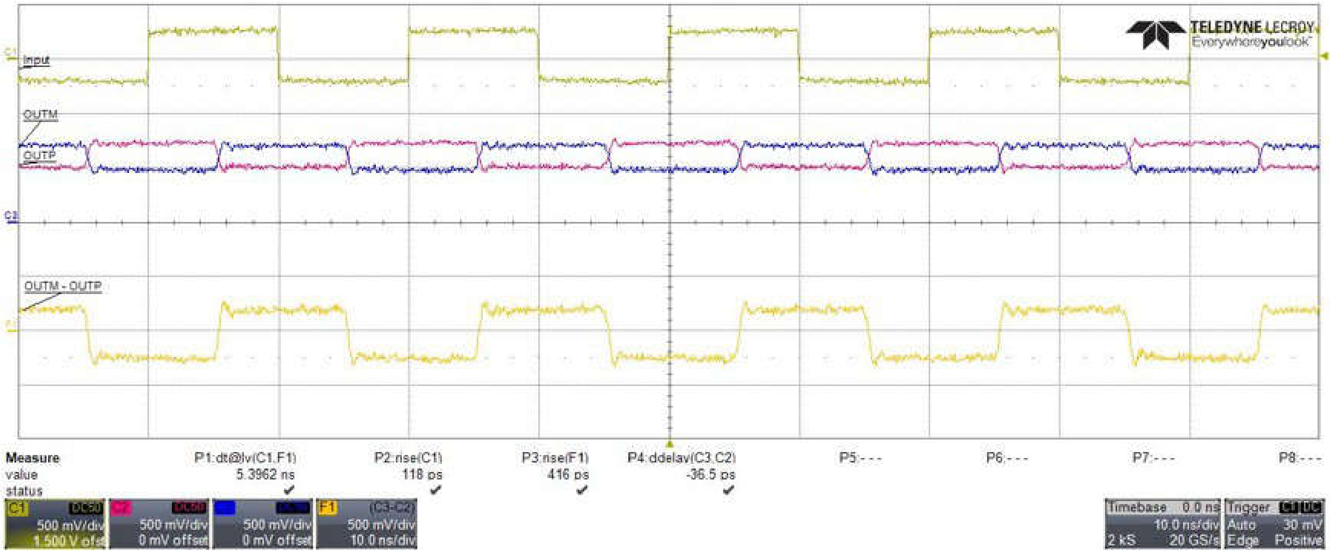


Figure 3-19. Delay Measurement with 0.9Vpp Input



Measure	P1:dt@lv(C1,F1)	P2:rise(C1)	P3:rise(F1)	P4:ddelay(C3,C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	5.3962 ns	118 ps	416 ps	-36.5 ps				
status	✓	✓	✓	✓				

C1 DC50	C2 DC50	C3 DC50	F1 (C3-C2)	Timebase 0.0 ns	Trigger C1 DC
500 mV/div	500 mV/div	500 mV/div	500 mV/div	10.0 ns/div	Auto 30 mV
1.500 V ofst	0 mV offset	0 mV offset	10.0 ns/div	2 kS 20 GS/s	Edge Positive

Figure 3-20. Delay Measurement with 0.5Vpp Input

The delays are measured to be around 5.4ns and based on the measured rise time, the bandwidth goes beyond 500MHz.

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010133.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010133.

4.2 Tools and Software

Tools

USB2ANY	USB2ANY Interface Adapter
ADC12DJ5200RFEVM	ADC EVM

Software

SLVC695	USB2ANY Explorer Software
ADC12DJ5200RFEVM	EVM GUI

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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