

**Test Data  
For PMP10750  
09/28/2015**



---

## Contents

1. Design Specifications .....	3
2. Circuit Description and PCB details.....	3
3. PMP10750 Board Photos .....	5
4. Thermal Data.....	6
5. Efficiency .....	8
6. Waveforms.....	9
6.1 Reverse Protection –Smart diode .....	9
6.2 Input Overvoltage Protection – PFET Fault switch .....	11
6.4 Output Voltage Ripple and Switch Node Voltage .....	14
6.5 Load Transient Response .....	16
7. Conducted Emissions .....	18

## 1. Design Specifications

Table 1: PMP10750 design specifications and recommended operating conditions

<b>Vin Minimum</b>	<b>4.8VDC</b>
<b>Vin Maximum</b>	<b>30 VDC(OVP at 20V)</b>
<b>Vout1</b>	<b>3.3 VDC_Slave</b>
<b>Iout 1</b>	<b>3A</b>
<b>Vout2</b>	<b>3.3VDC_Master</b>
<b>Iout 2</b>	<b>3A</b>
<b>Approximate Switching Frequency</b>	<b>2.1MHz Approx(all the DC/DC converters)</b>
<b>EMI</b>	<b>CISPR25 Class 5</b>
<b>Protection</b>	<b>Input Overvoltage, Reverse polarity , Short Circuit protections at Outputs, Load Dump protection</b>

## 2. Circuit Description and PCB details

PMP10750 is a System optimized (CISPR 25 Class 5) 20W design for upstream converter used in ADAS system with all the required automotive protection.

The design has various protections such as Load dump through TVS (ISO pulse testing), Reverse Voltage (Innovative Smart diode with very low Iq), Battery Disconnect Switch with OVP protection (PFET) and is EMI optimized to meet Conductive EMI limits of CISPR25 Class5.

Input voltage range is between 4.5V to 30V with OVP at 20V and hence will operate in wide input voltage conditions.

LM74610 is used for Battery reverse protection which utilizes a charge pump to drive an N-channel FET to provide a resistive path for the bypass current to flow. LM53603Q1 is used as front end DC/DC Buck converter which is 2.2MHz switching, Synchronous rectified Wide Vin Buck Converter which can take transient up to 42V.

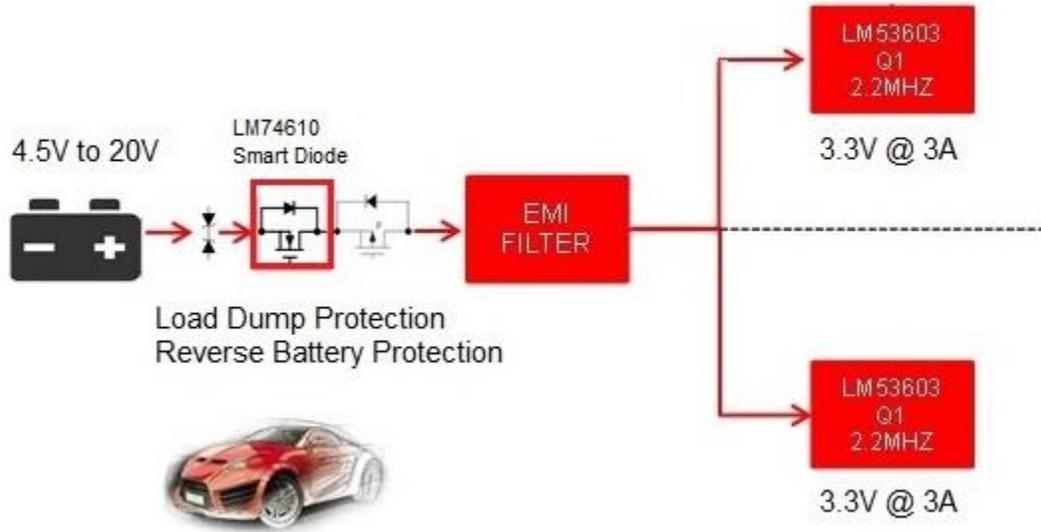


Figure 1: Application block diagram for PMP10750

The Board dimension of PMP10750 PCB is 3450mil \* 4950mil. Two layer PCB was used for the design.

### 3. PMP10750 Board Photos

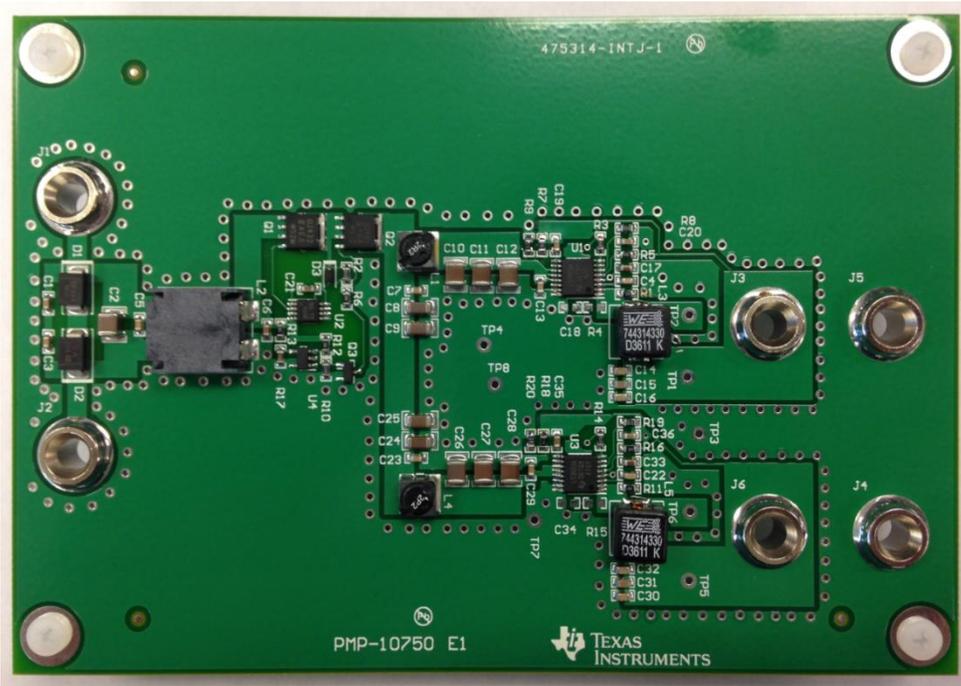


Figure 2: Top of board

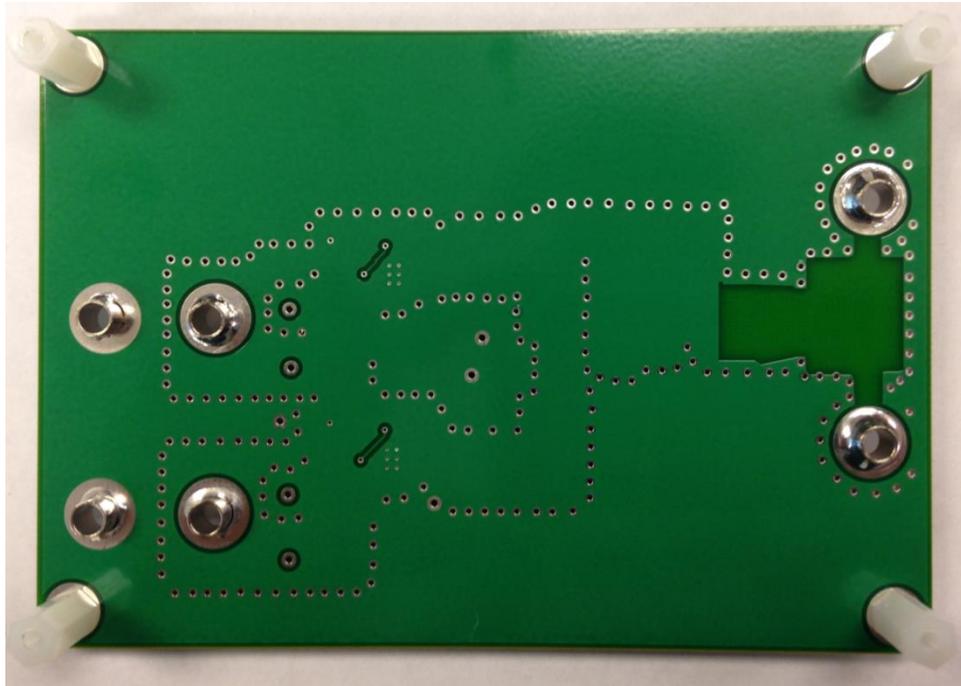


Figure 3: Bottom of board

#### 4. Thermal Data

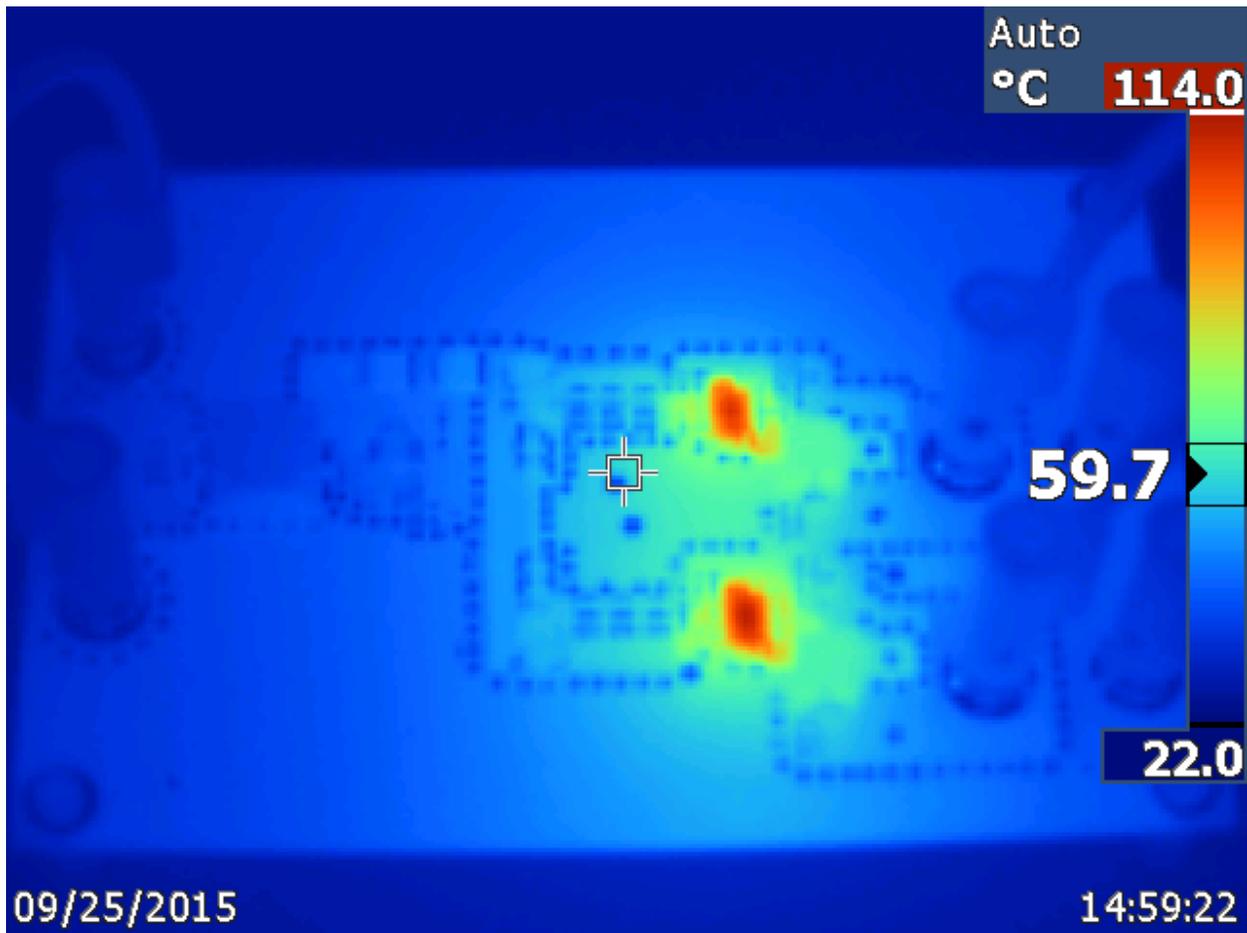


Figure 4: IR thermal image at steady state with 12Vin and both outputs fully loaded

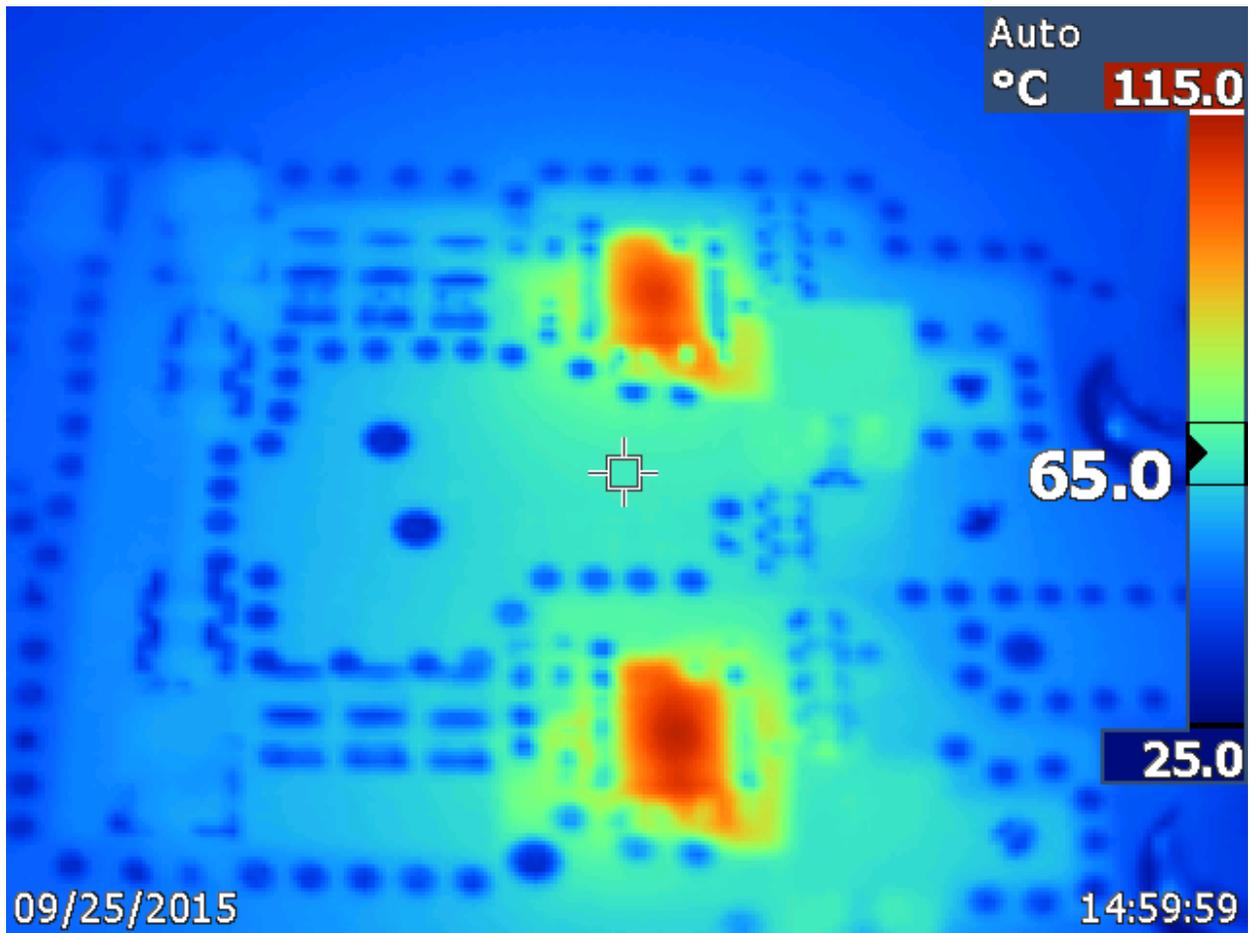


Figure 5: IR thermal image at steady state with 12Vin zoomed on LM53603

## 5. Efficiency

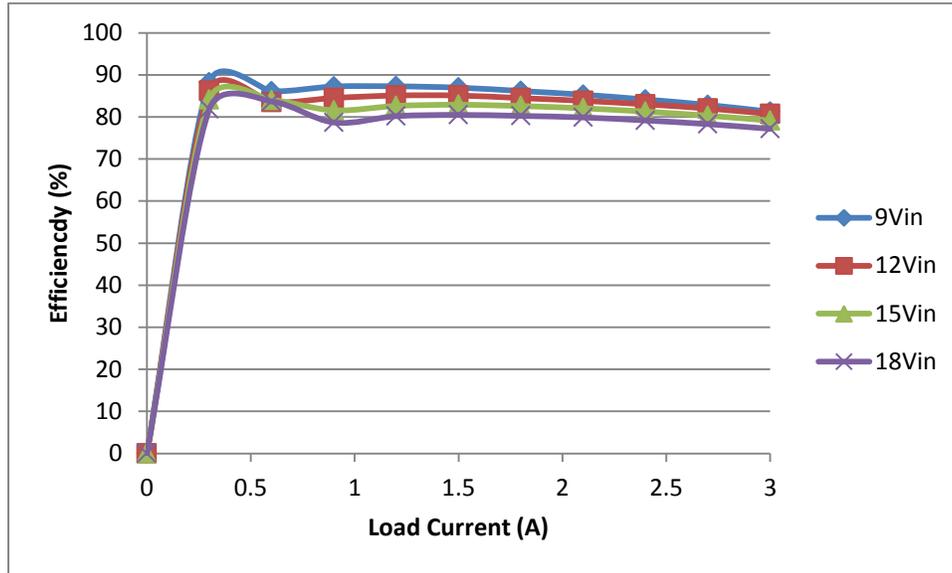


Figure 6: Load current vs efficiency with both outputs identically loaded for various input voltages

## 6. Waveforms

### 6.1 Reverse Protection –Smart diode

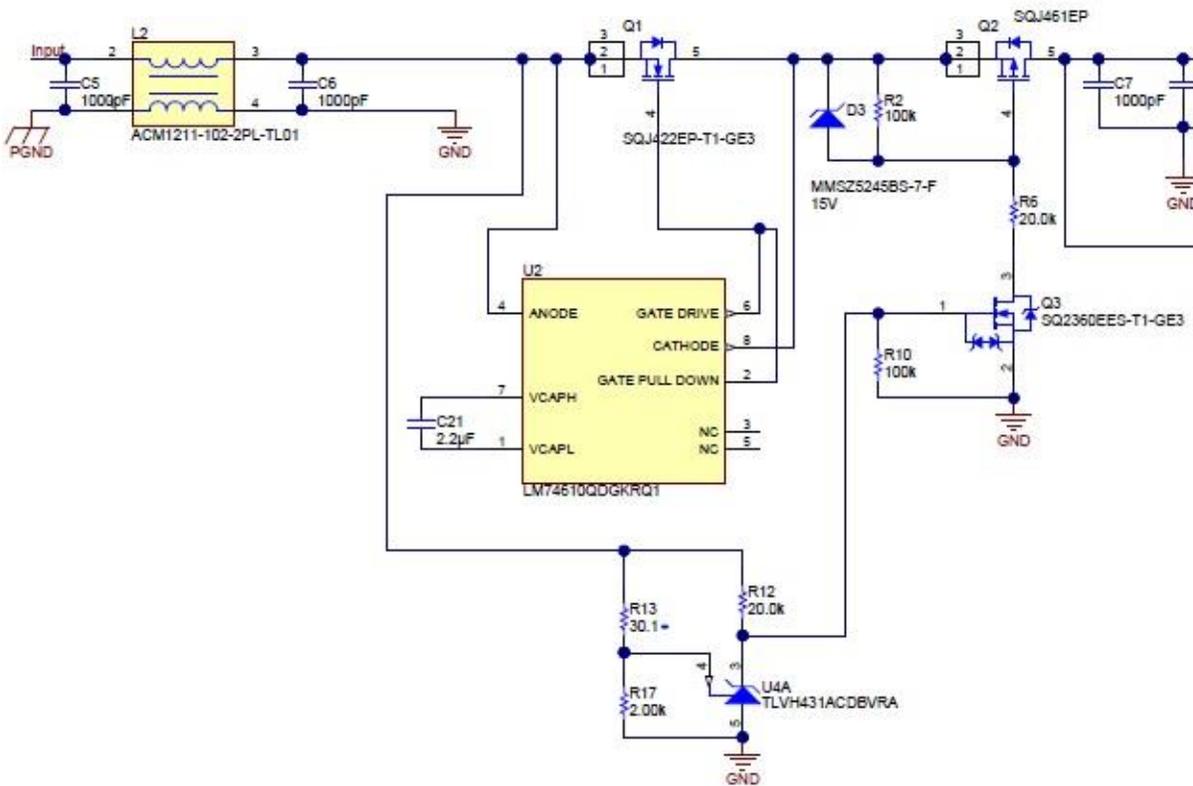


Figure 7: Reverse protection using smart diode circuit schematic

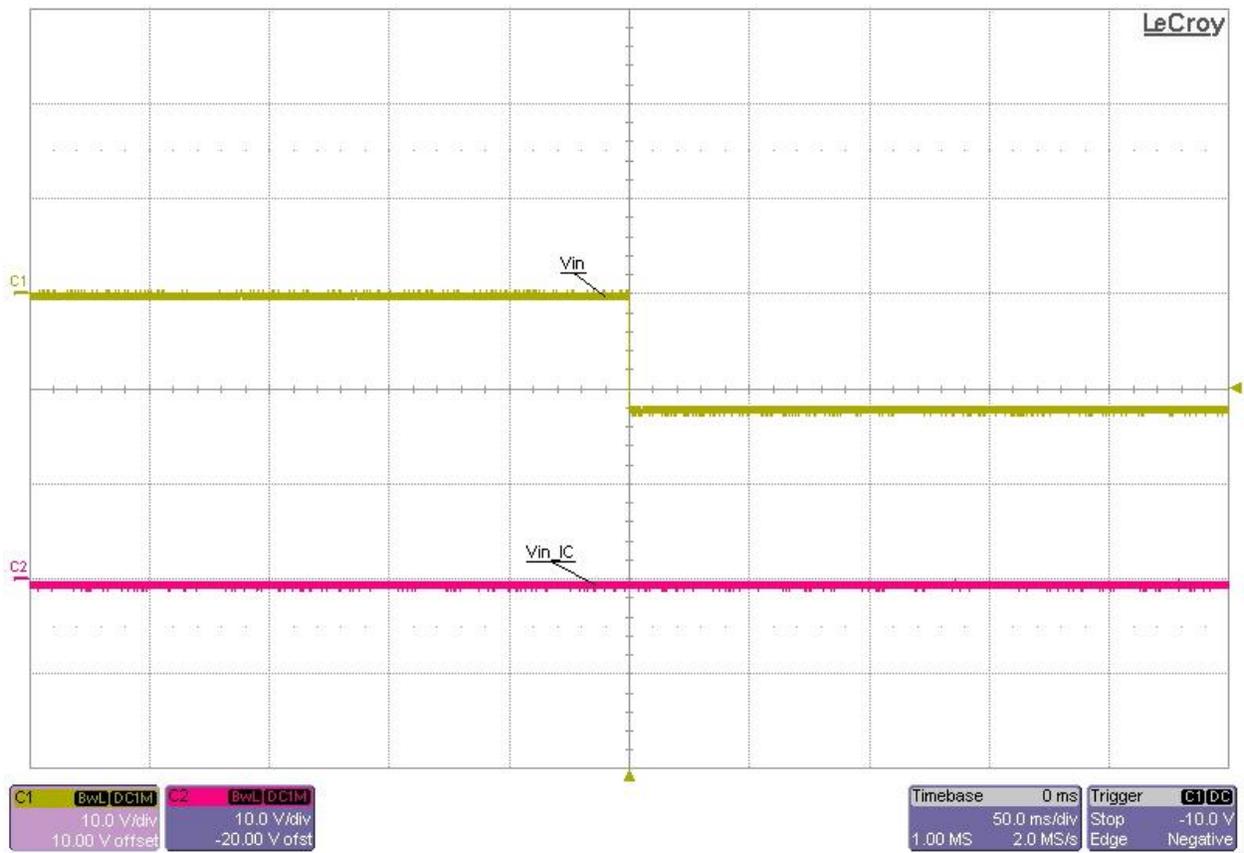


Figure 8: Reverse input voltage protection as  $V_{in}$  transitions to -12V while  $V_{in}$  to the IC remains unchanged

## 6.2 Input Overvoltage Protection – PFET Fault switch

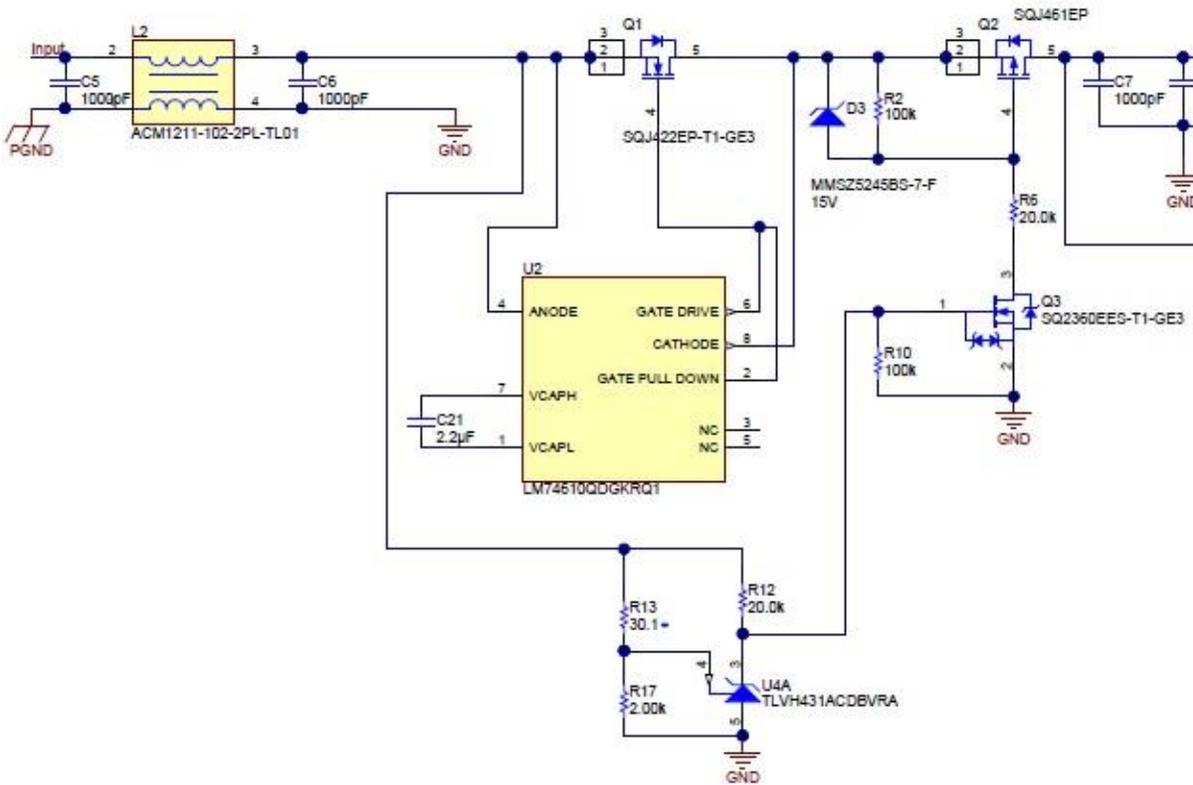


Figure 9: Input overvoltage protection using a PFET fault switch circuit schematic

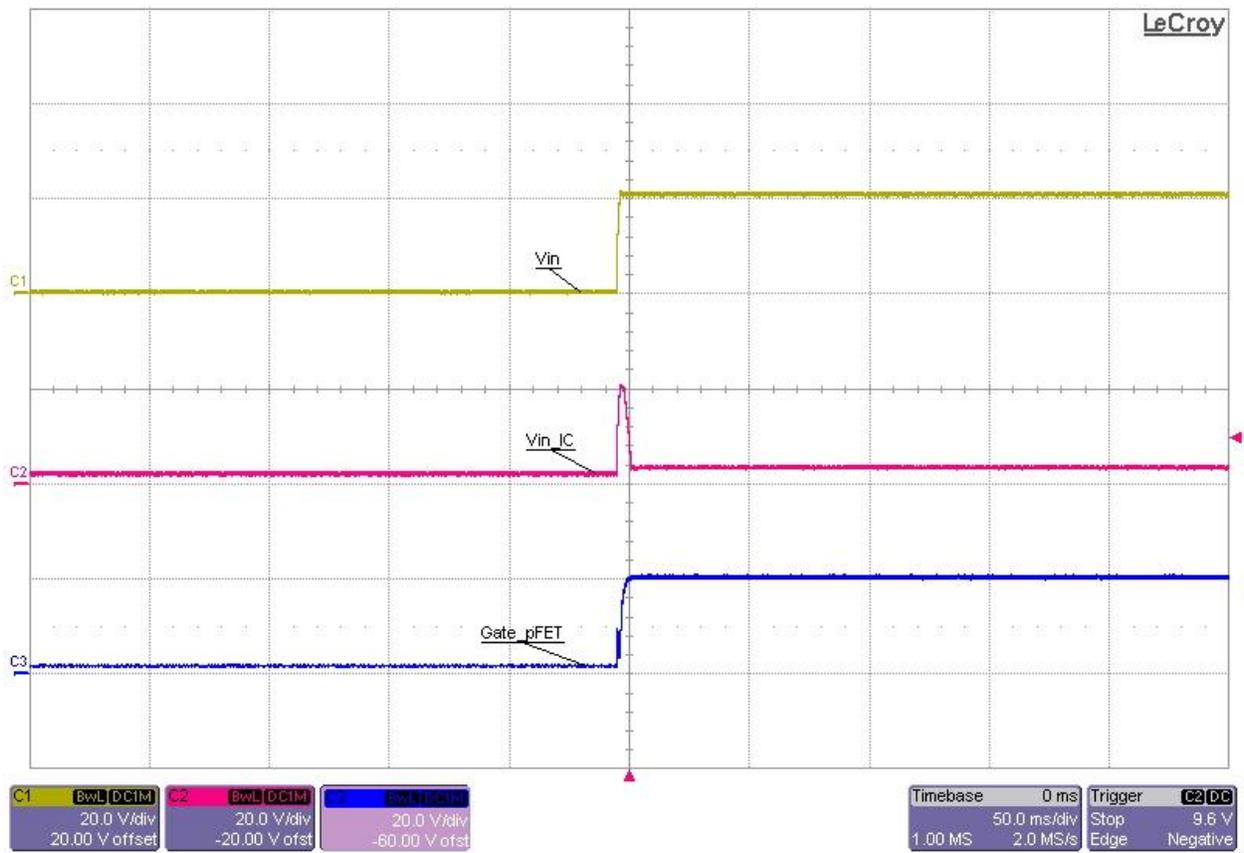


Figure 10: Transition to overvoltage condition shown on C1 forces the PFET gate shown on C3 high bringing the input voltage to the IC shown on C2 low

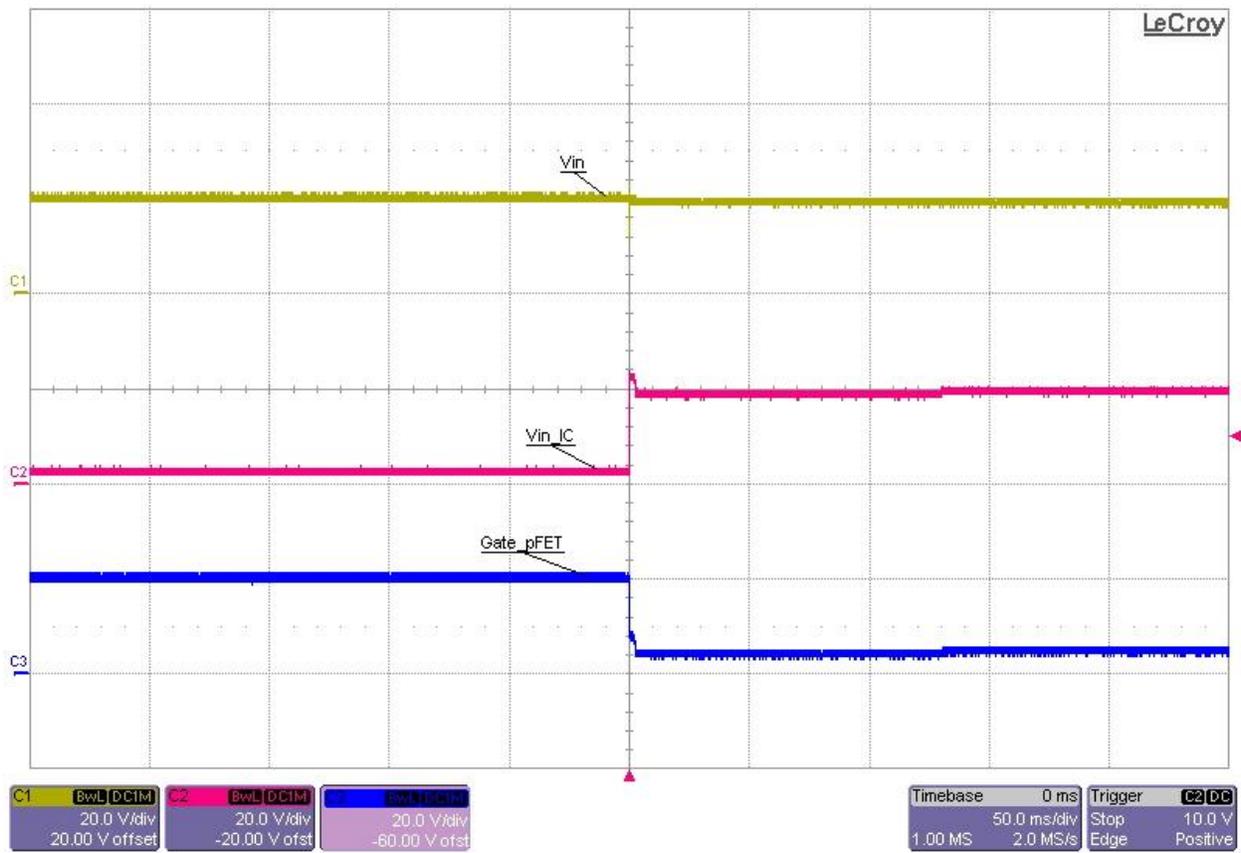


Figure 11: Transition to normal condition shown on C1 forces the PFET gate shown on C3 low allowing the input voltage to the IC shown on C2 to come up

### 6.4 Output Voltage Ripple and Switch Node Voltage

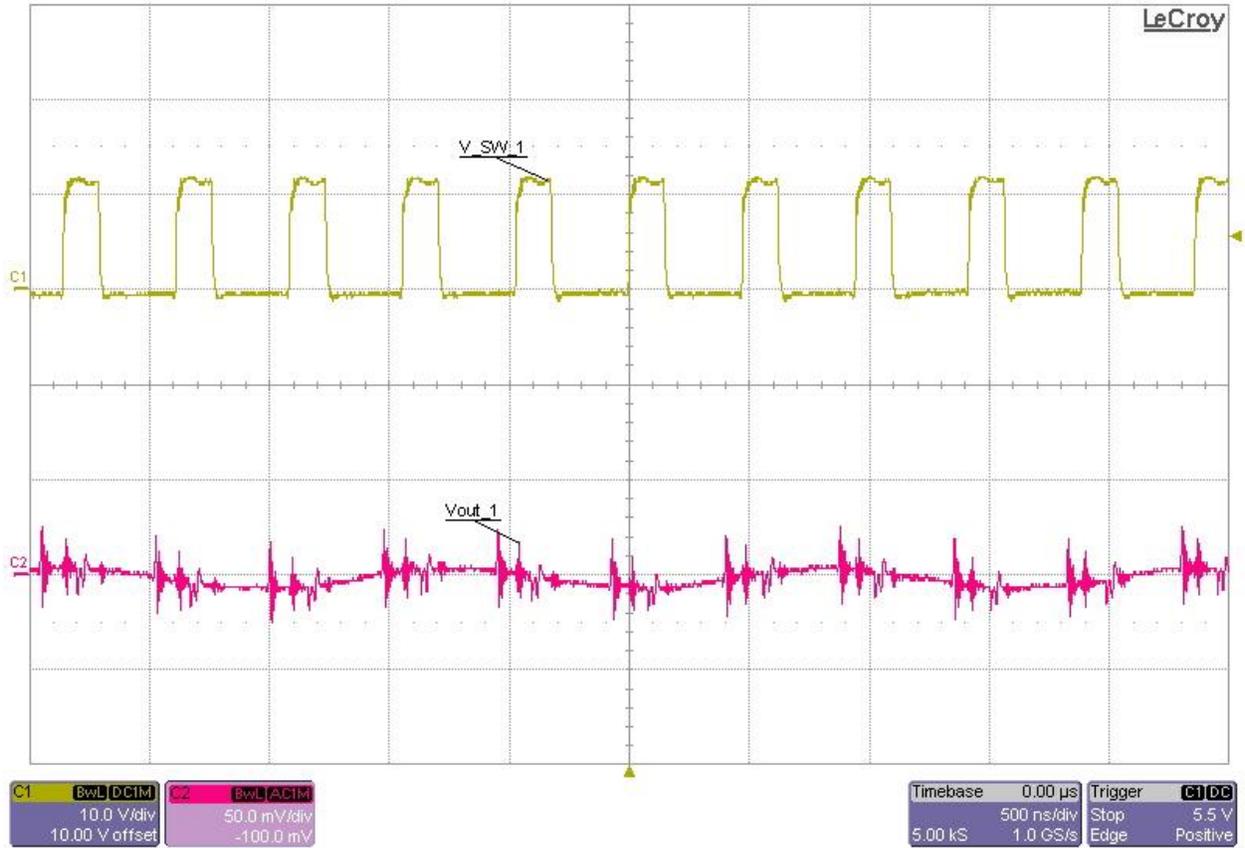


Figure 12: Switch node voltage and output voltage ripple for the 3.3V\_Slave channel of LM53603 with both outputs fully loaded

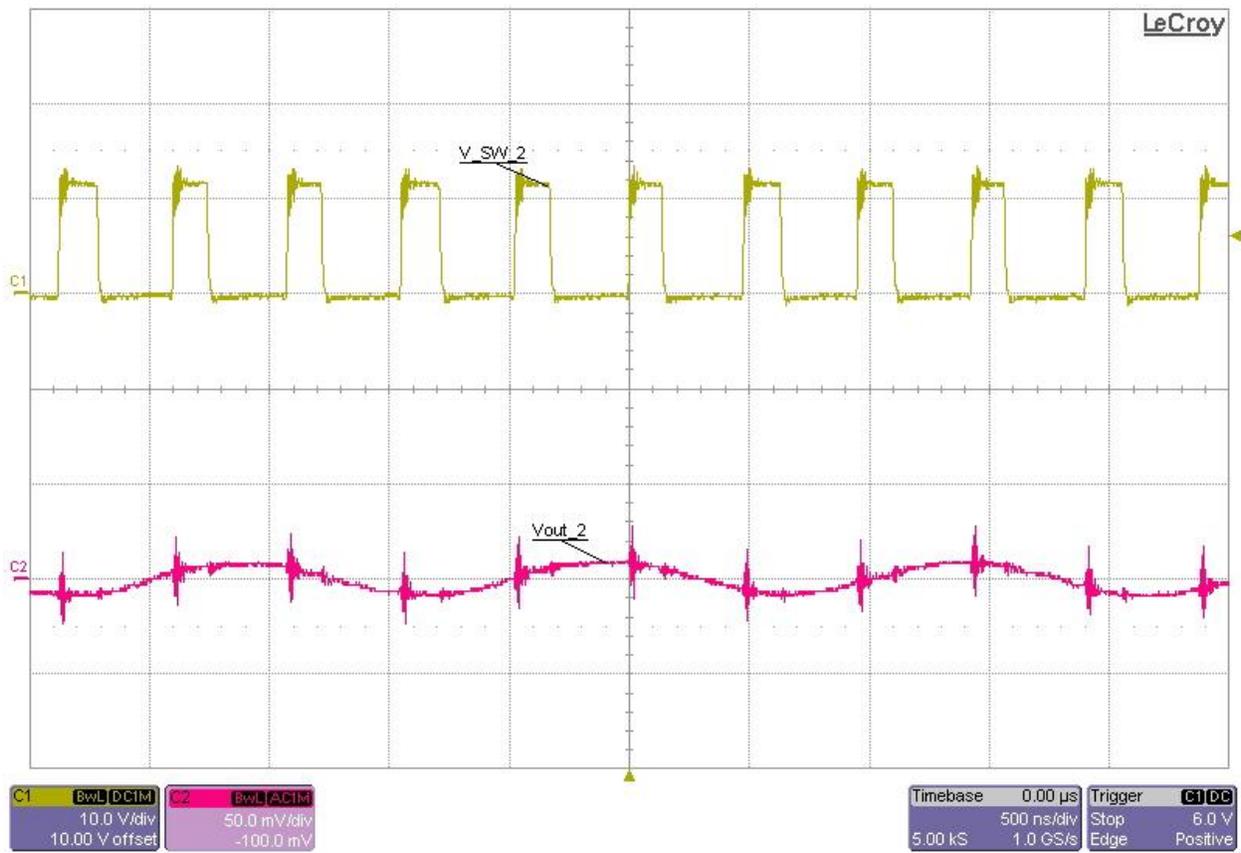


Figure 13: Switch node voltage and output voltage ripple for the 3.3V\_Master channel of LM53603 with both outputs fully loaded

## 6.5 Load Transient Response

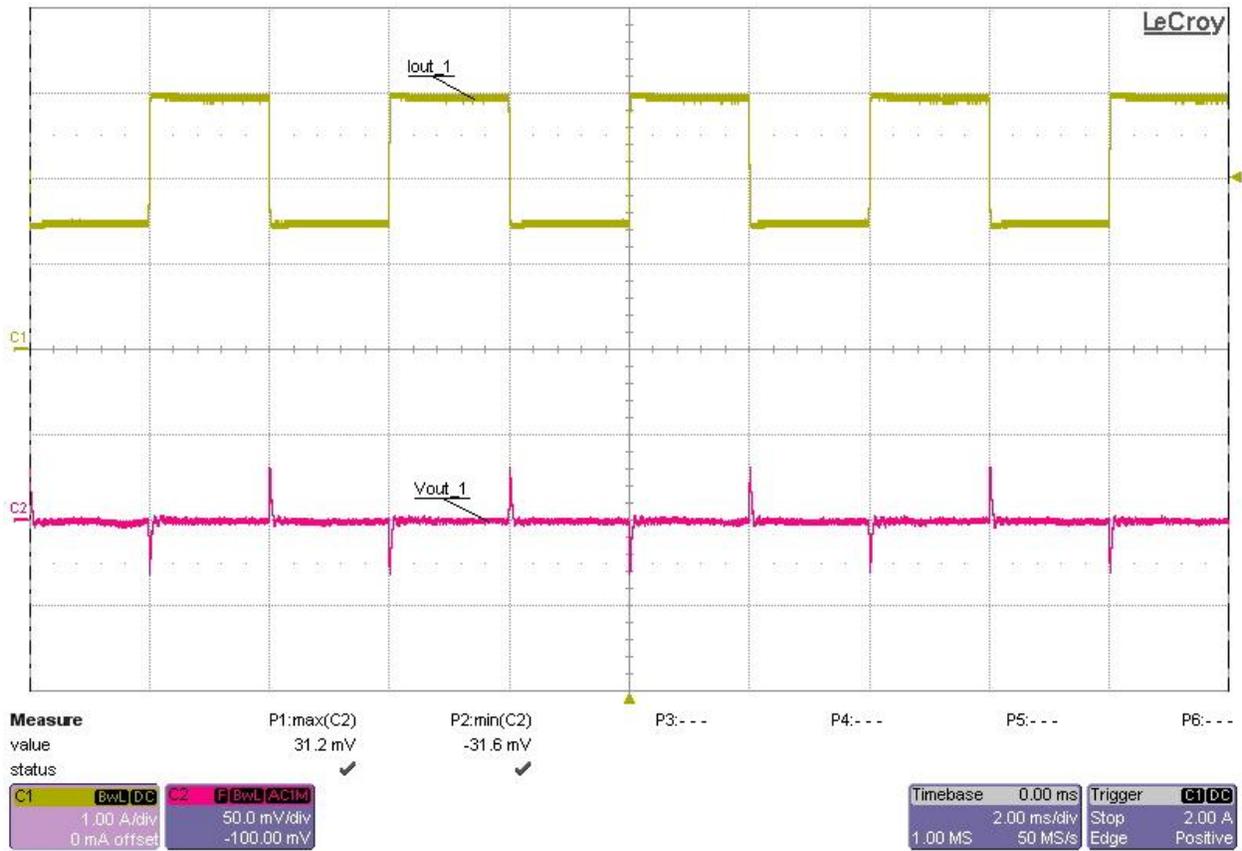


Figure 14: Load transient response shown on C2 for 3.3V\_Slave channel at 6V<sub>in</sub> with a 50%-to-100% load step shown on C1 while 3.3V\_Master channel is under full load

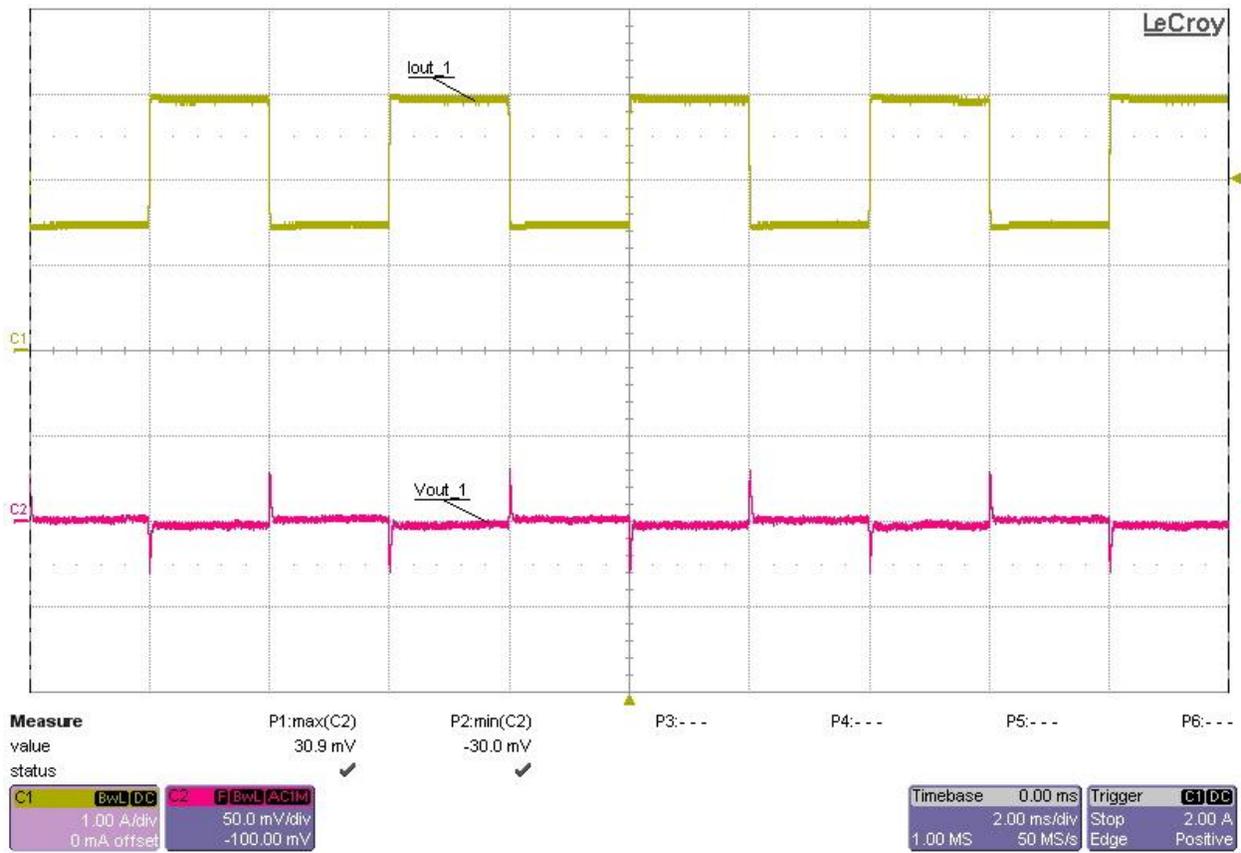


Figure 15: Load transient response shown on C2 for 3.3V\_Slave channel at 12Vin with a 50%-to-100% load step shown on C1 while 3.3V\_Master channel is under full load

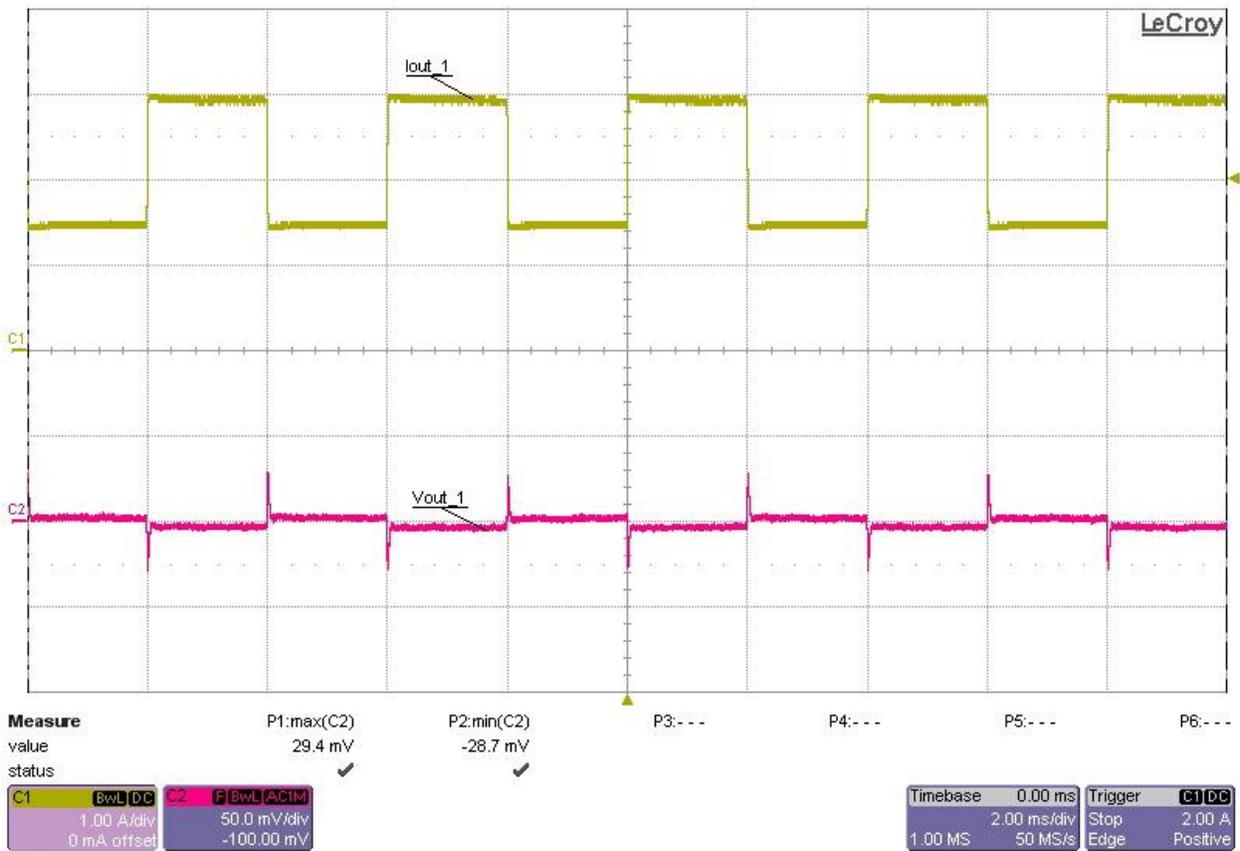


Figure 16: Load transient response shown on C2 for 3.3V\_Slave channel at 18Vin with a 50%-to-100% load step shown on C1 while 3.3V\_Master channel is under full load

The load transient response for the other channel (3.3V\_Master) is identical to that of the 3.3V\_Slave channel shown above.

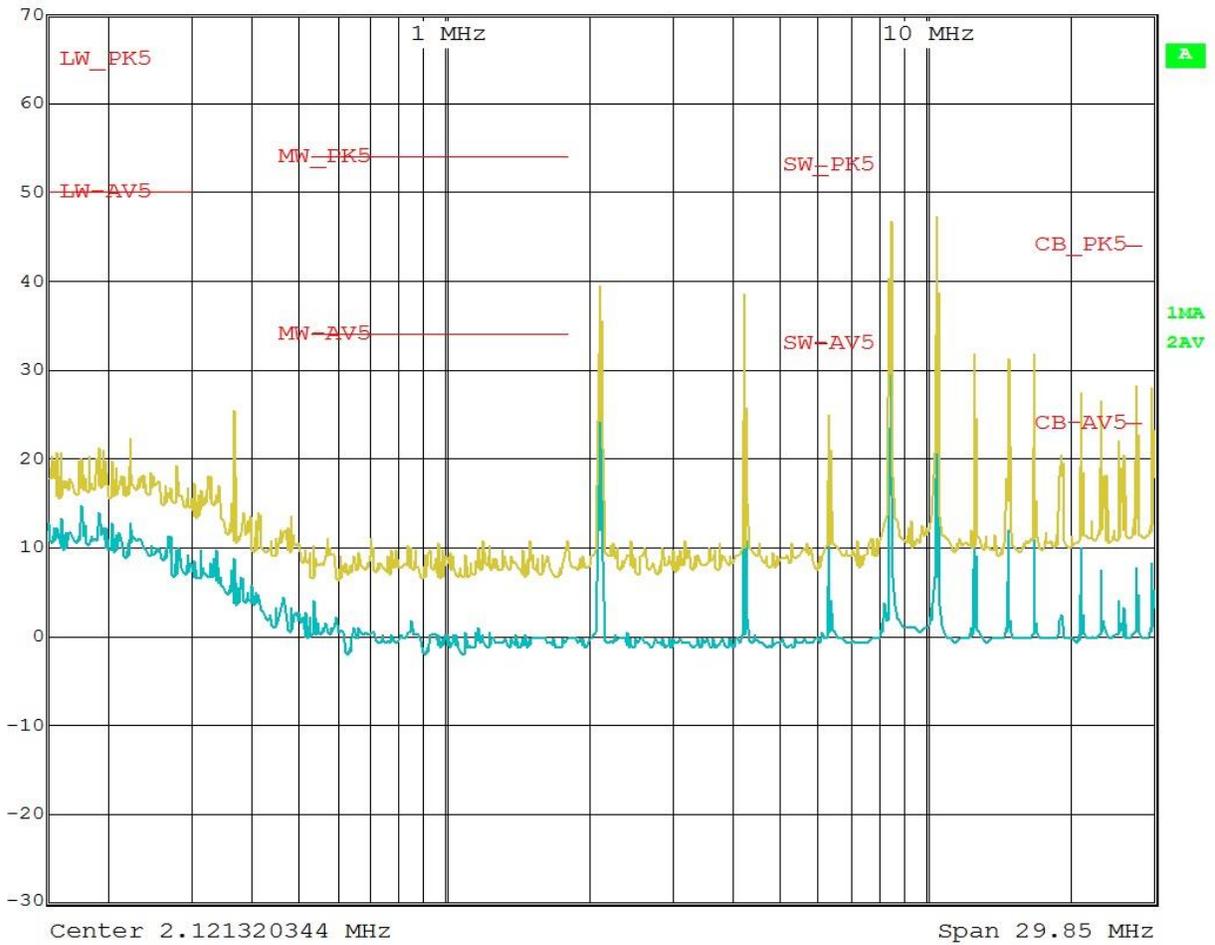
## 7. Conducted Emissions

The conducted emissions is tested followed the of CISPR 25 standards. The frequency band examined spans from 150 kHz to 108 MHz covering the AM, FM radio bands, VHF band, and TV band specified in the CISPR 25.

Figure 17 shows the test result using peak detection (yellow trace) and average detection (blue trace) measurements respectively up to 30MHz. Figure 18 shows the test result using peak detection (yellow trace) and average detection (blue trace) measurements respectively from 30MHz to 108MHz. The limit lines shown in red are the Class 5 limits(up 108MHz) for conducted disturbances specified in the CISPR 25. The results show the power supply operates quietly and the noise is below the Class 5 limits overall.

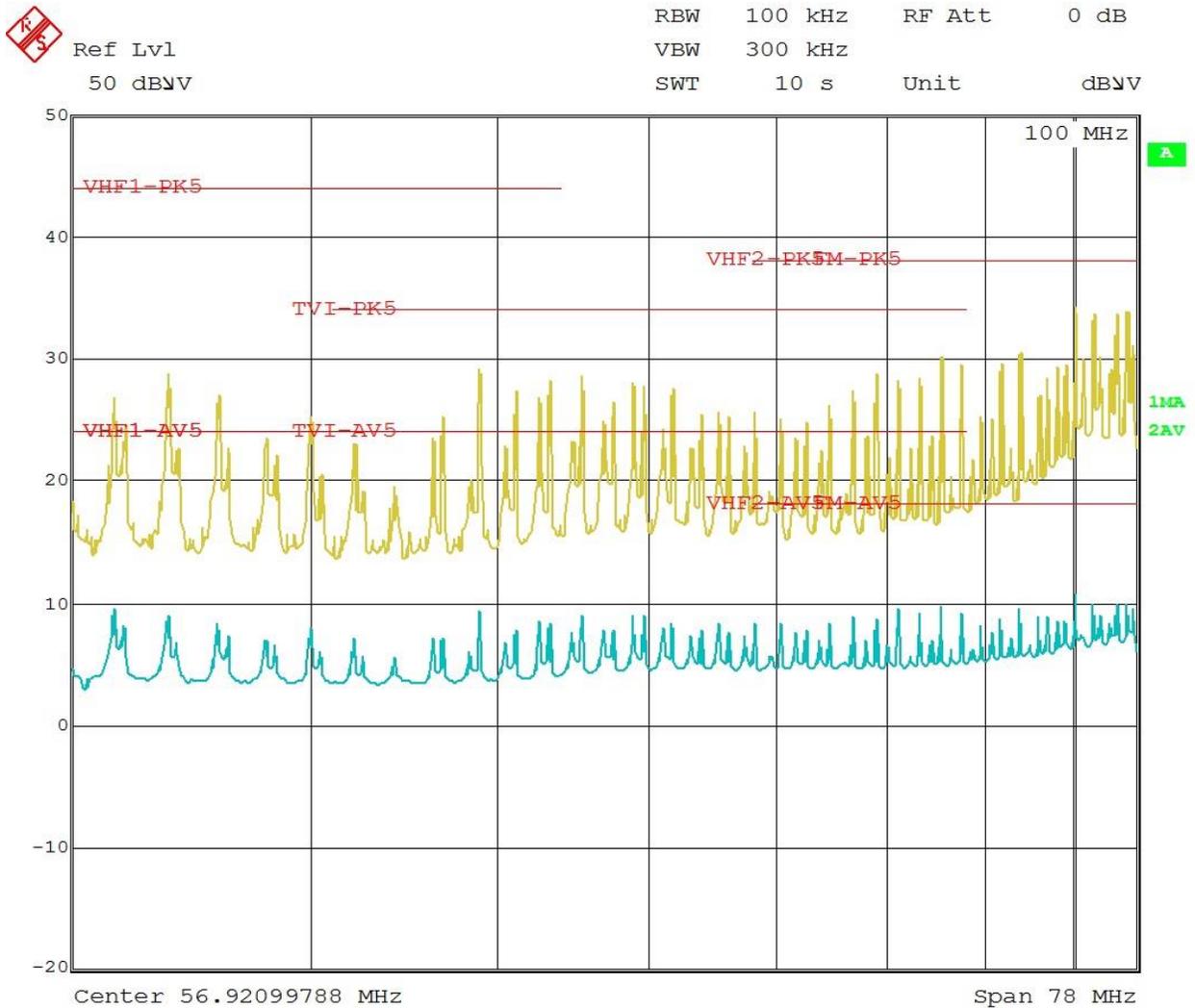

 Ref Lvl  
70 dBμV

RBW	10 kHz	RF Att	10 dB
VBW	30 kHz	Unit	dBμV
SWT	10 s		



Date: 25.SEP.2015 13:44:19

Figure 17: EMI testing for PMP10750 up to 30 MHz showing the peak detection (yellow), average detection (blue), and Class 5 peak and average limits (red)



Date: 25.SEP.2015 13:43:10

Figure 18: EMI testing for PMP10750 from 30 MHz to 108MHz showing the peak detection (yellow), average detection (blue), and Class 5 peak and average limits (red)

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated