

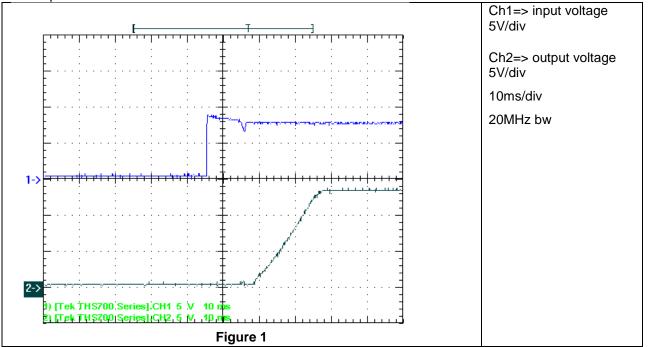
1	Startup2
2	Shutdown
3	Efficiency
4	Load Regulation
5	Line Regulation7
6	Output Ripple Voltage
7	Input Ripple Voltage
8	Load Transients9
9	Control Loop Frequency Response
10	Miscellaneous Waveforms16
11	Thermal Image

Topology: SEPIC Device: TPS40210

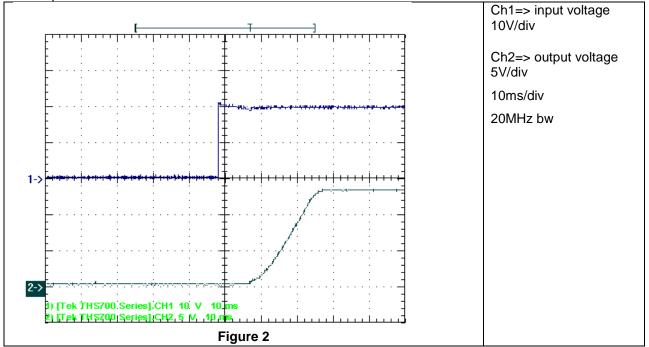


1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 8V, with 2A load at the output.

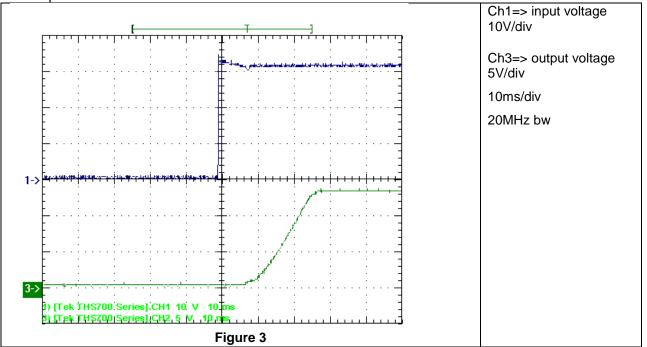


The startup waveform is shown in the Figure 2. The input voltage was set at 20V, with 2A load at the output.





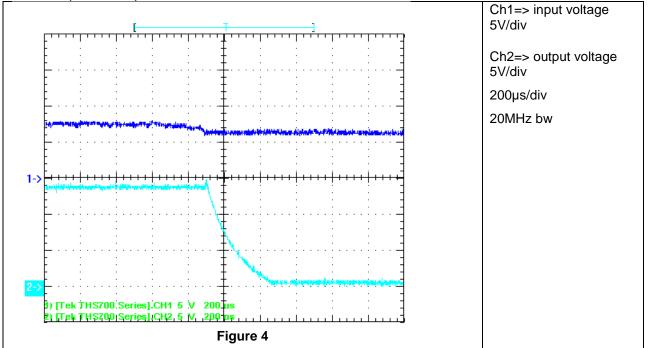
The startup waveform is shown in the Figure 3. The input voltage was set at 32V, with 2A load at the output.

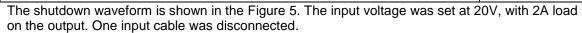


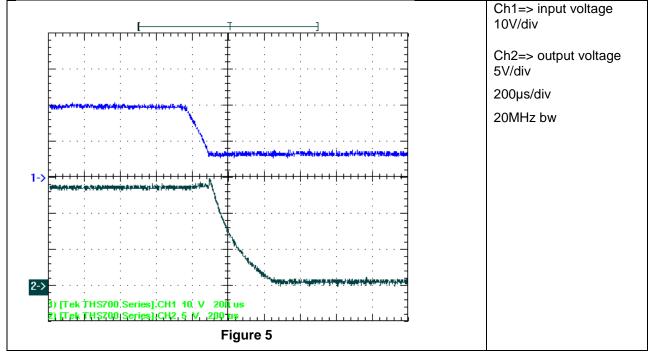


2 Shutdown

The shutdown waveform is shown in the Figure 4. The input voltage was set at 8V, with 2A load on the output. One input cable was disconnected.

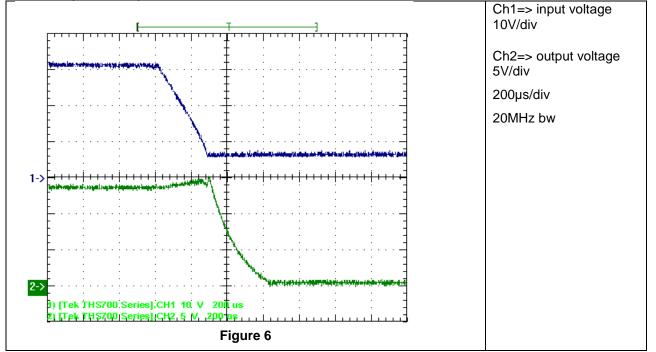








The shutdown waveform is shown in the Figure 6. The input voltage was set at 32V, with 2A load on the output. One input cable was disconnected.





3 Efficiency

The efficiency is shown in the Figure 7 below. The input voltage was set to 8V, 20V and 32V.

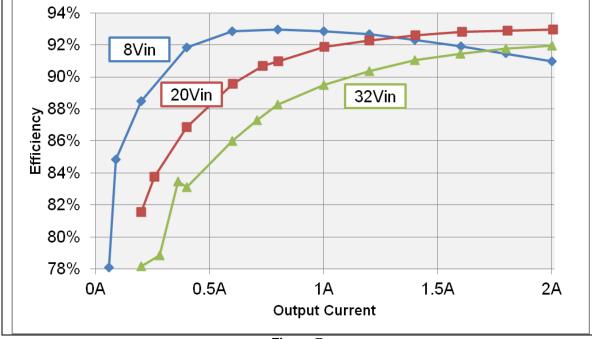


Figure 7

4 Load Regulation

The load regulation of the output is shown in the Figure 8 below. The input voltage was set to 8V, 20V and 32V.

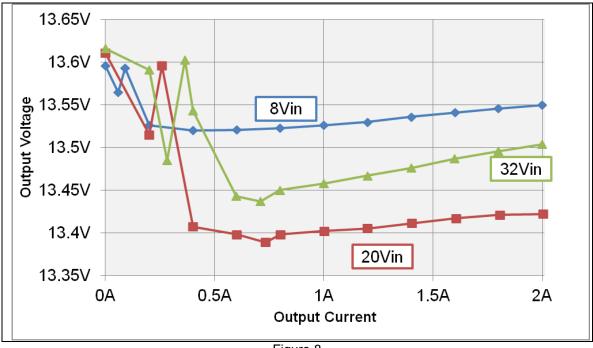


Figure 8	
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5 Line Regulation

The line regulation is shown in Figure 9. The output current was set about 2A.

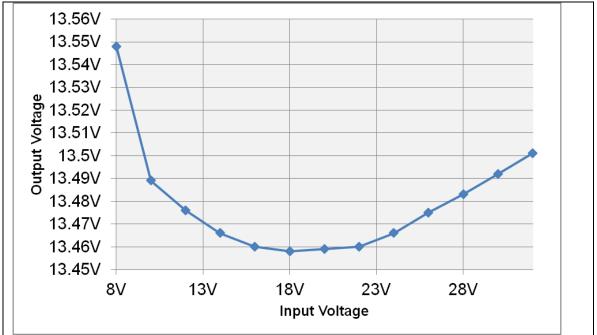
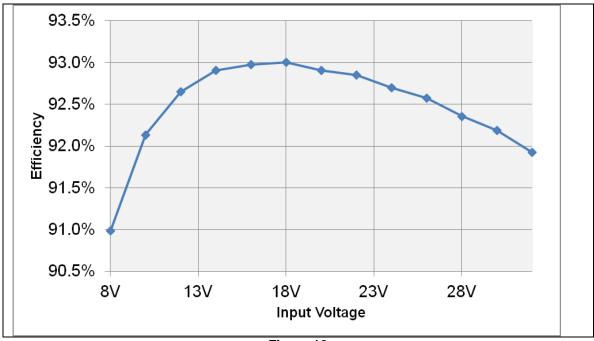


Figure 9

With the same setup the efficiencies are shown in Figure 10.

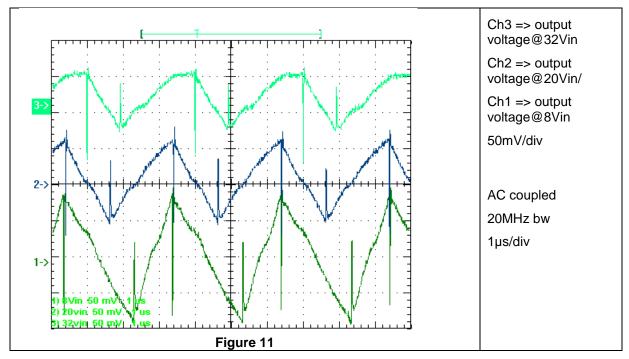






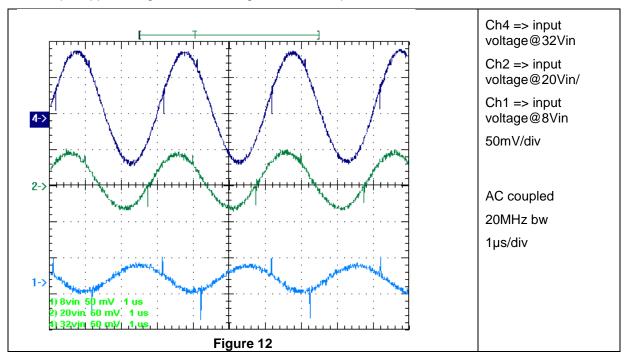
6 Output Ripple Voltage

The output ripple voltage is shown in Figure 11. The output current was set to 2A



7 Input Ripple Voltage

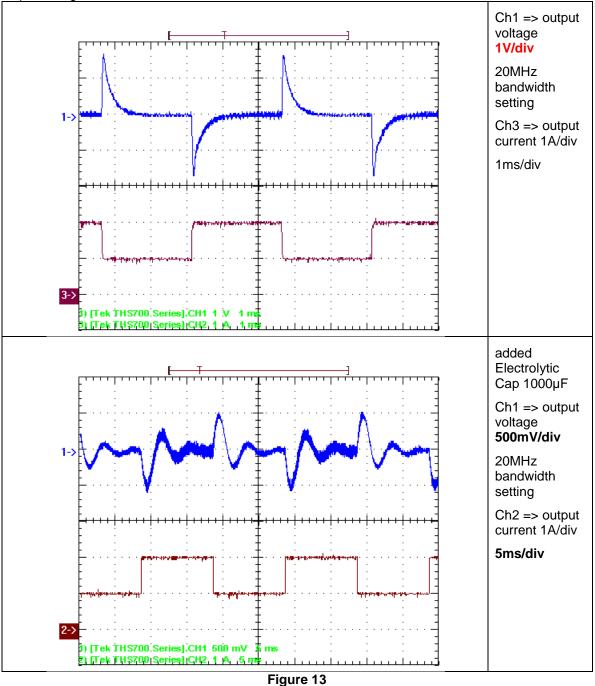
The output ripple voltage is shown in Figure 12 The output current was set to 2A





8 Load Transients

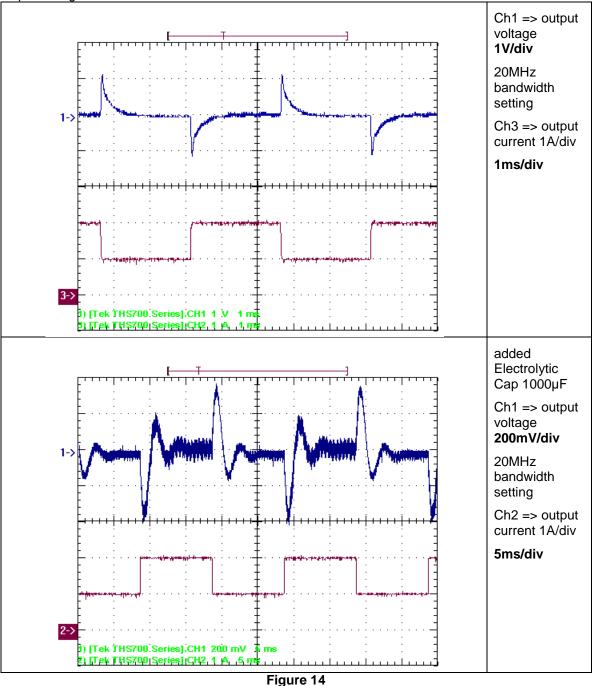
The Figure 13 shows the response to load transients. The load is switching from 1A to 2A. The input voltage was set to 8V



Upper pic shows transient response for ceramics only, lower pic w/ 1000uF added; For use of this design powering a capacitor bank for pulsed loads **gain needs to be adjusted**.



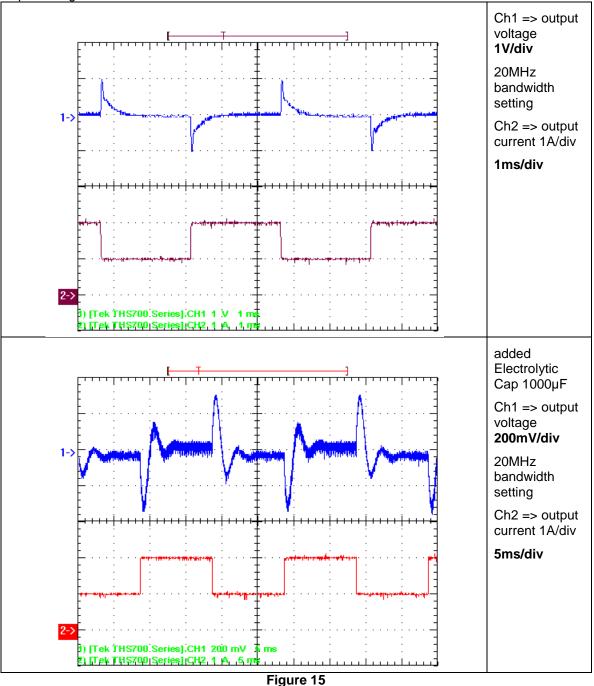
The Figure 14 shows the response to load transients. The load is switching from 1A to 2A. The input voltage was set to 20V



Upper pic shows transient response for ceramics only, lower pic w/ 1000uF added; For use of this design powering a capacitor bank for pulsed loads **gain needs to be adjusted**.



The Figure 15 shows the response to load transients. The load is switching from 1A to 2A. The input voltage was set to 32V



Upper pic shows transient response for ceramics only, lower pic w/ 1000uF added; For use of this design powering a capacitor bank for pulsed loads **gain needs to be adjusted**.



9 **Control Loop Frequency Response**

Figure 16 shows the loop response. 2A-load applied. The input voltage was set to 8V.

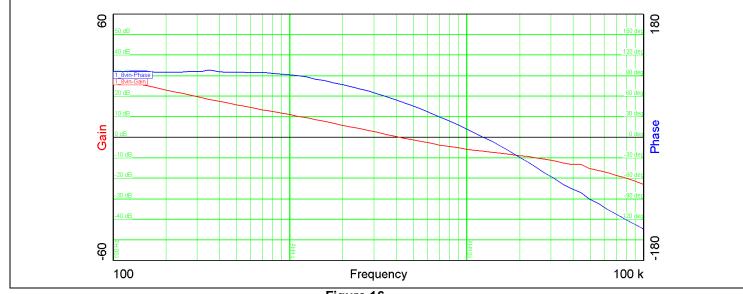
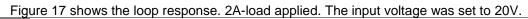


Figure 16



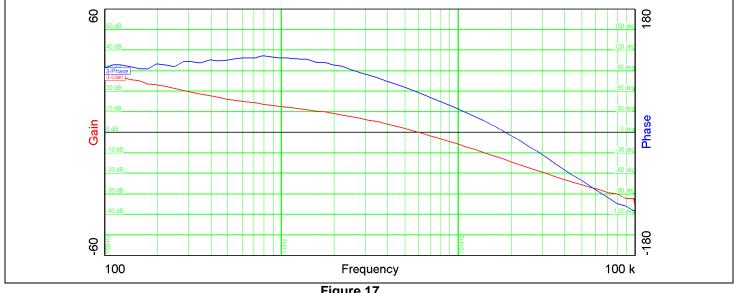


Figure 17

11/14/13 PMP8709RevC Test Results



Figure 18 shows the loop response. 2A-load applied. The input voltage was set to 32V.

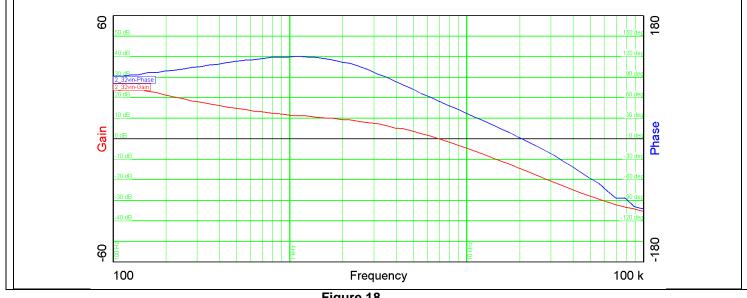


Figure 18

Table 1 summarizes the results from Figure 16 Figure 17 and Figure 18.

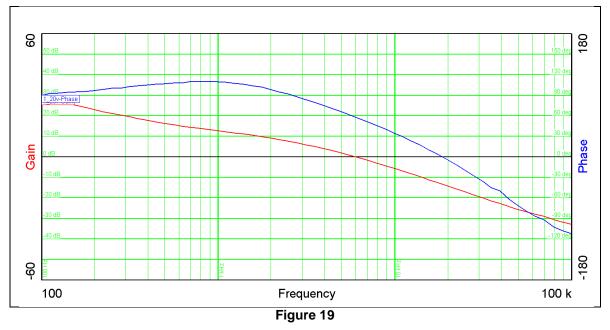
Vin	8V	20V	32V
Bandwidth (kHz)	4.23	5.95	6.94
Phase margin	52°	58	55
slope (20dB/decade)	-0.89	-1.23	-1.34
gain margin (dB)	-6.86	-13.4	-14.9
slope (20dB/decade)	-0.54	-1.52	-1.79
freq (kHz)	12.5	18.5	20.6

Table 1



Figure 19 and Figure 20 shows the influence of an additional output electrolytic cap $(1000\mu F/25V)$. The input voltage was set to 20V with 2A output current.

without cap



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Upper pic shows Bode plot for ceramics only, lower pic w/ 1000uF added; For use of this design powering a capacitor bank for pulsed loads **gain needs to be adjusted**. Here in example gain has to be increased **by 20dB** to achieve bw 2kHz. (reduce Zero to 200Hz, set Pole to 20kHz)

added 1000µF



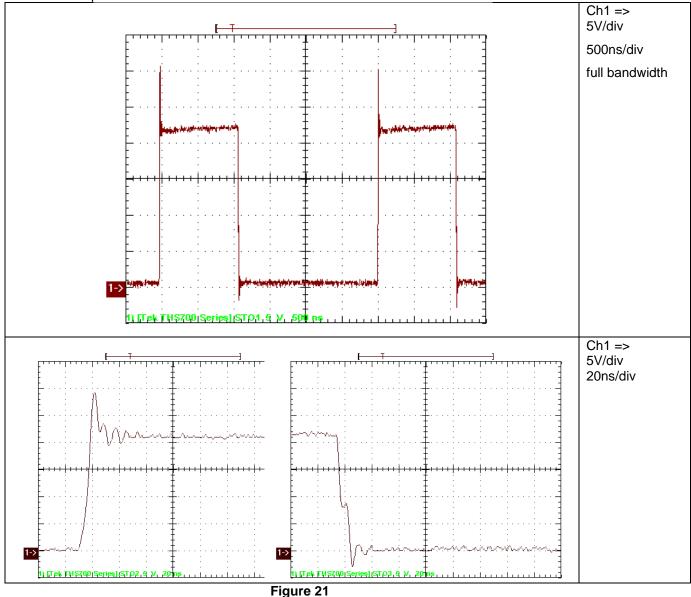
	no added Cap	1000µF
Bandwidth (kHz)	5.98	0.349
Phase margin	58°	34.3
slope (20dB/decade)	-1.19	-1.23
gain margin (dB)	-13.4	-34.9
slope (20dB/decade)	-1.45	-0.194
freq (kHz)	18.6	44.9

Table 2



10 Miscellaneous Waveforms

The waveform of the voltage on Q1 (Drain-Source) is shown in Figure 21. Input voltage was set to 8V and output current to 2A.





The waveform of the voltage on the gate to source is shown in Figure 22. Input voltage was set to 8V and output current to 2A.

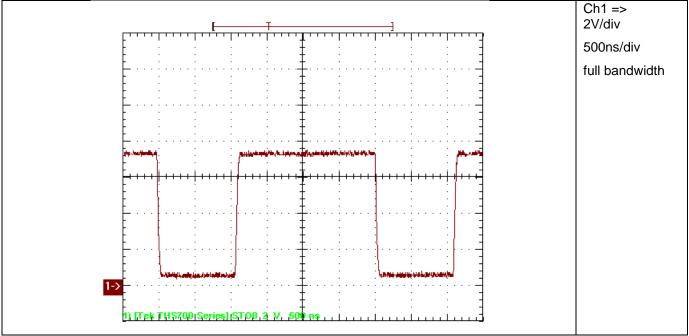
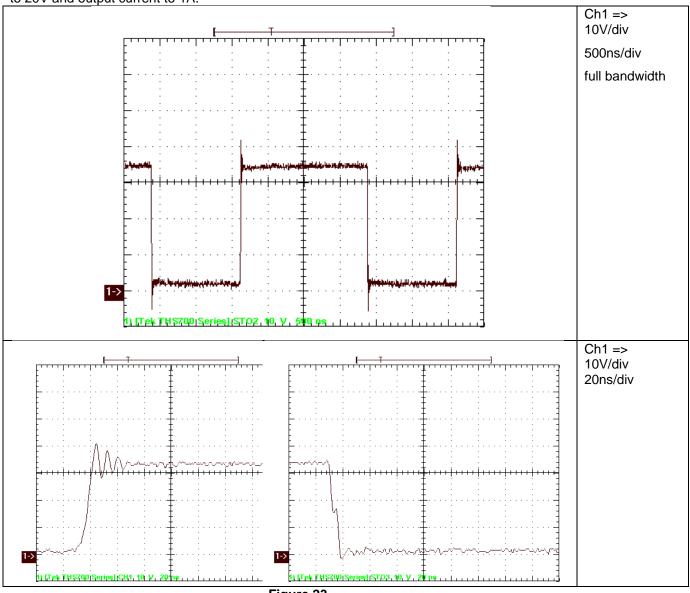


Figure 22



The waveform of the voltage on Q1 (Drain-Source) is shown in Figure 23. Input voltage was set to 20V and output current to 1A.







The waveform of the voltage on the gate to source is shown in Figure 24. Input voltage was set to 20V and output current to 2A.

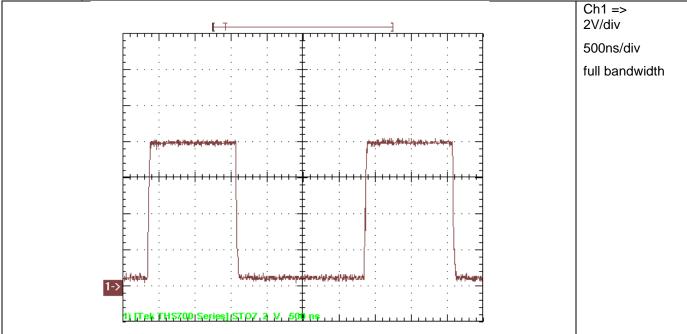
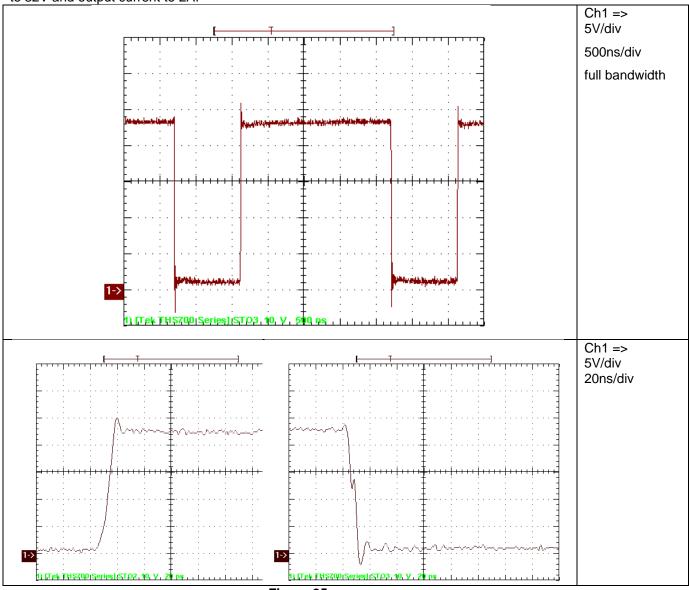


Figure 24



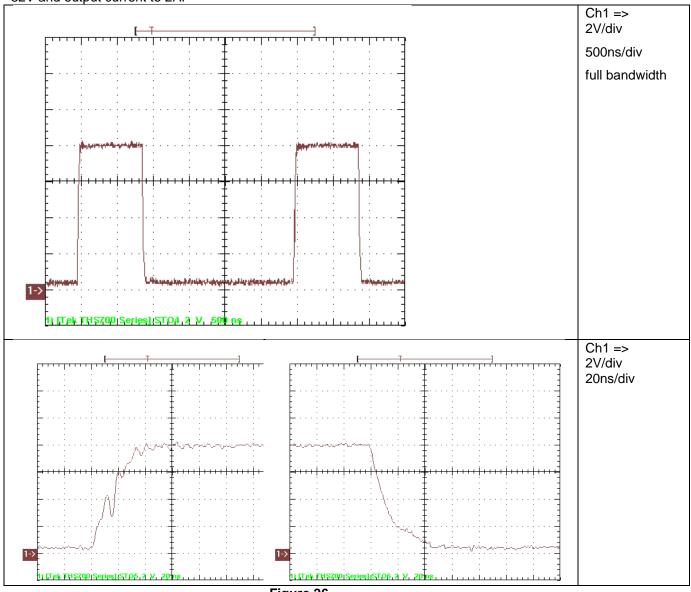
The waveform of the voltage on Q1 (Drain-Source) is shown in Figure 25. Input voltage was set to 32V and output current to 2A.







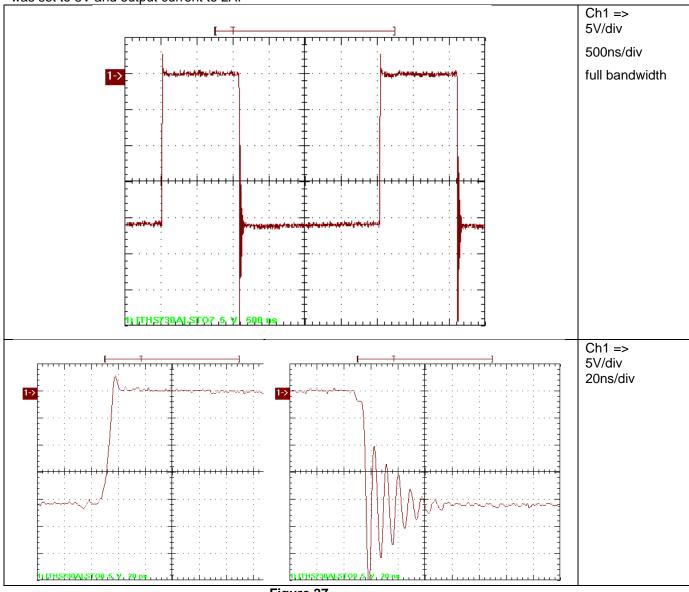
The waveform of the voltage on the gate to source is shown in Figure 26. Input voltage was set to 32V and output current to 2A.







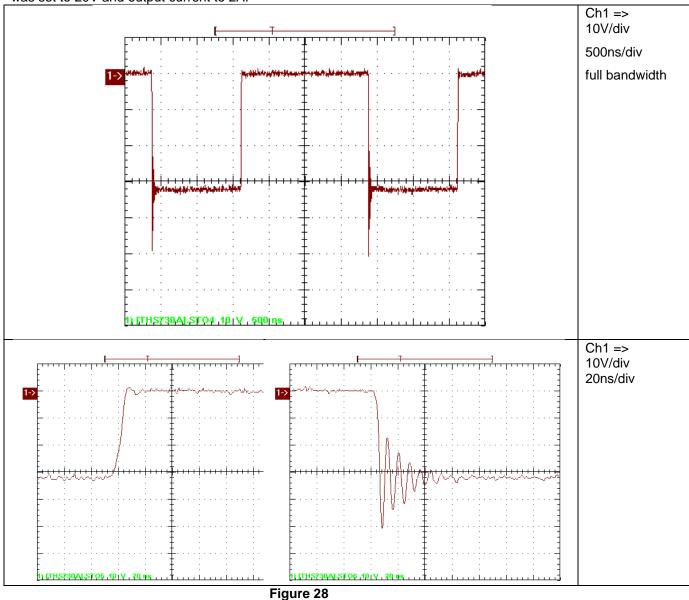
The waveform of the voltage on D1 (**referenced to VOUT**) is shown in Figure 27. Input voltage was set to 8V and output current to 2A.





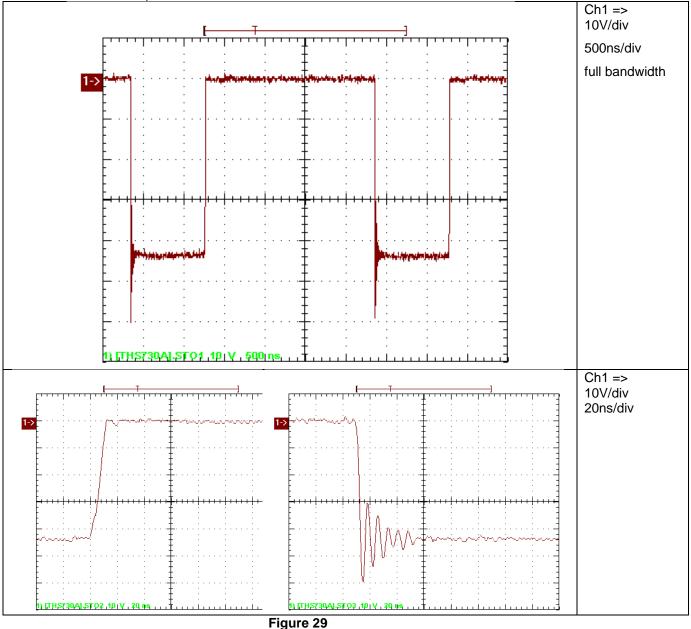


The waveform of the voltage on D1 (**referenced to VOUT**) is shown in Figure 27. Input voltage was set to 20V and output current to 2A.





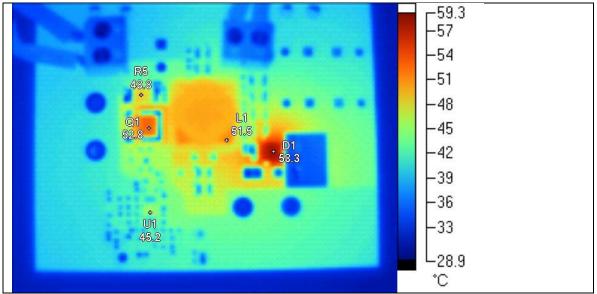
The waveform of the voltage on D1 (**referenced to VOUT**) is shown in Figure 29. Input voltage was set to 32V and output current to 2A.





11 Thermal Image

Figure 30 shows the thermal image at 20V input voltage and 2A output current.





Name	Temperature
D1	58.3°C
Q1	52.8°C
R5	48.8°C
U1	45.2°C
L1	51.5°C

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