TI Designs: TIDA-00790
Passive Equalization For RS-485

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SN65HVD78	Product Folder

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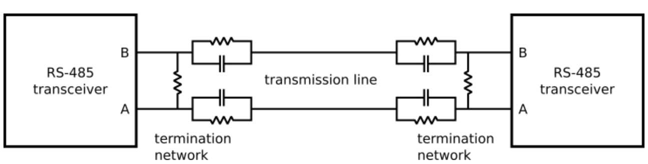
Design Features

- Evaluation of a passive equalization circuit on RS-485 connections
- Significant jitter reduction of RS-485 point to point connections
- Higher signal rates possible
- Low cost solution

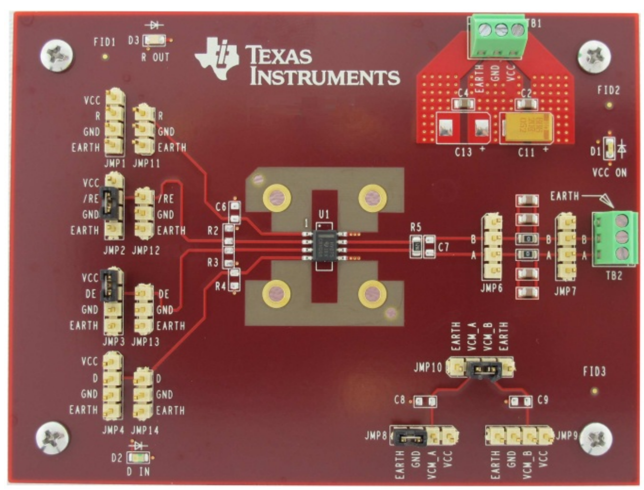
Featured Applications

- Elevators
- Industrial robots

Block Diagram



Board Image



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1 Design Overview

Many industrial communication networks are unidirectional or bidirectional point to point connections. For RS-485 connections usually 100Ω or 120Ω cables are used. To avoid reflections, they typically have two corresponding termination resistors on the end of the cables.

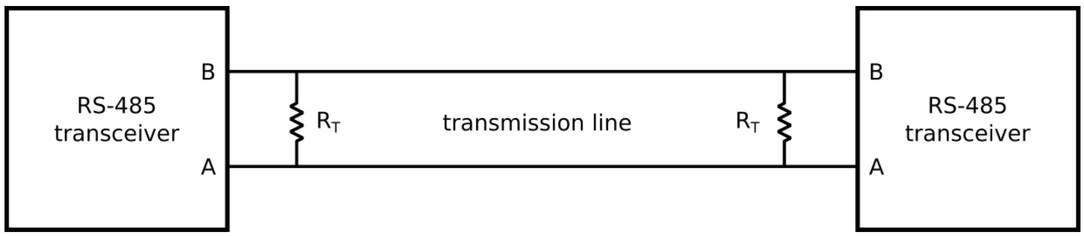

Figure 1. Typical point to point RS-485 connection

Figure 2 shows a single-ended input signal into a RS-485 transceiver. This signal will be changed to a differential signal by the transceiver and will be changed back to a single ended output signal by the receiving transceiver on the other side of the bus.

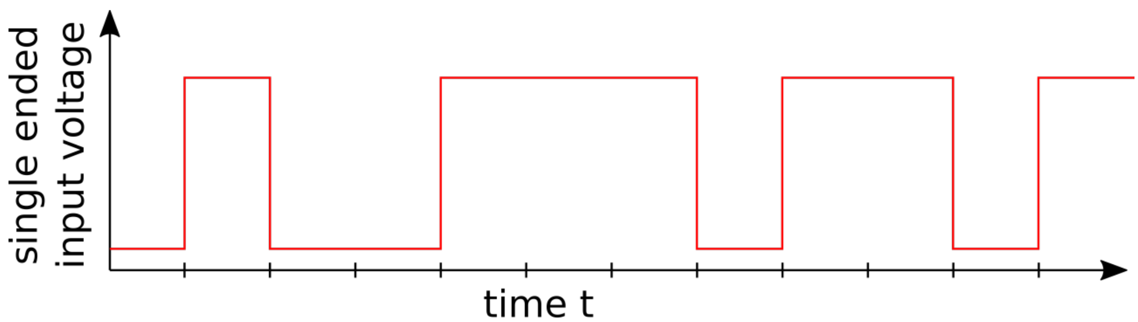

Figure 2. Single ended input signal from UART

A single-ended communication line consists of one signal trace and a ground trace. A differential communication line consists of two signal traces where the second signal trace transports the inverted signal of the first one. The cables used are mostly shielded or unshielded twisted pair cables. This configuration helps to improve noise immunity, as the noise couples on to both cable connections in the same way and the differential voltage stays the same. As a signal travels through a transmission line, the signal gets altered by the cable's parasitic effects and shows a typical low-pass filter characteristic.

Figure 3 shows two signals: the differential signal on top and the receiving single ended signal on the bottom. The gray trace on the top shows the theoretical differential output voltage. However, in reality the transmission line will change that signal to the red one, showing typical RC characteristics.

An ideal receiver compares the differential input voltages with zero volts. If the voltage on the A line is higher than the B line, the receiving pin R on the receiver will be high. If the voltage on the A line is lower than on the B line, the receiving pin R will be low. The transition takes place after the differential voltage signal changed its polarity, resulting in the time shifted single ended receiving output voltage, shown on the bottom in Figure 3.

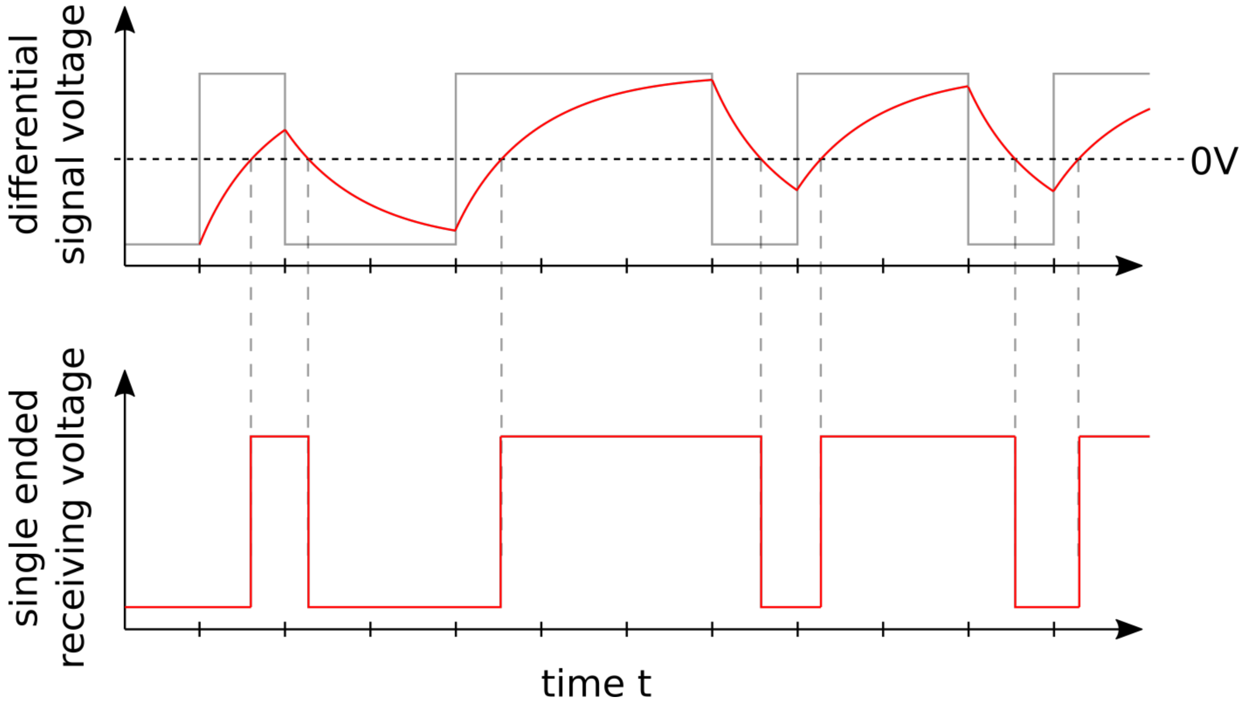

Figure 3. Top: Theoretical (gray) and real (red) differential signal

Bottom: Output signal

If the data rate on the bus is high, the differential voltage very often does not reach the full output swing, resulting in a time shift of edges on the output line. The time shift of the edges is related to the distance of the signal relative to the signal's full amplitude level. The closer the signal is to the full amplitude, the longer it will take to see the edge on the single ended receiving signal. This effect might be significant and can even destroy the signal by taking longer than a single bit period resulting in lost data.

Figure 4 shows a theoretical eye diagram of data signal received from a transmission line. The low-pass characteristic of the transmission line results in deviation of the edge positions in time. Since a signal may cross its logic threshold earlier or later depending on the data pattern. This effect is called data-dependent jitter.

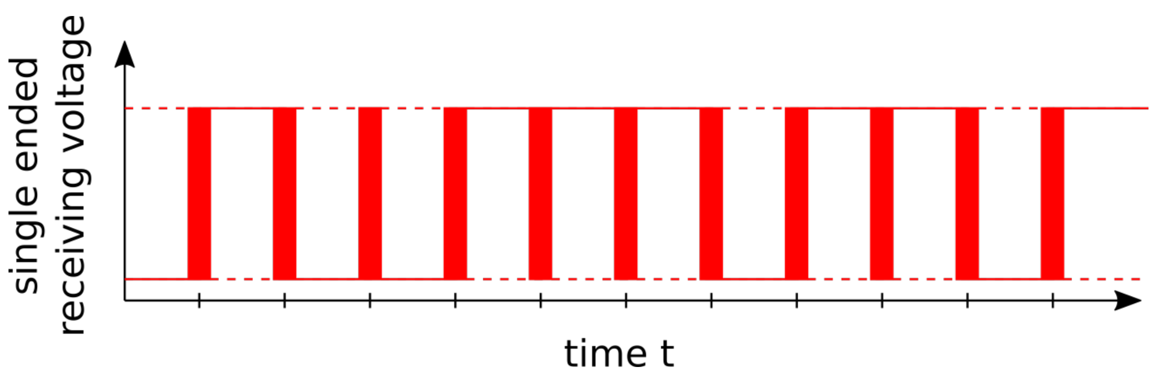

Figure 4. Theoretical eye diagram of the output signal

To lower the jitter, closer analysis on the cable should be done. Figure 5 shows three different Bode plots and represents the idea of a passive equalizer from a frequency perspective. The cable itself, shown here in green, shows a typical low-pass filter characteristic. In the diagram the cable shows a roll off of -20 dB/decade. For real cables this is not always the case, but for a simple approach the cable can be seen that way.

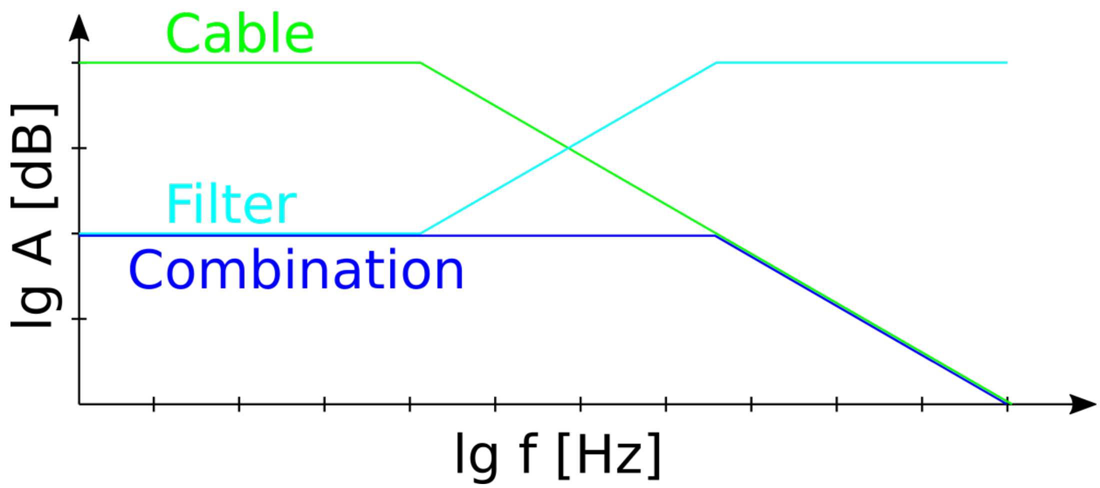

Figure 5. Bode plot cable (green), filter (cyan) and the resulting overall transfer function (blue)

Figure 6 shows the termination network of a passive RS-485 equalizer circuit. This mirrored, differential termination network has a filter function, represented by the cyan curve in the Bode plot in Figure 5. The cable and the filter work in series and therefore combine to the blue "Combination" curve in the Bode plot. Depending on the value of the resistors and capacitors used, the low frequency attenuation will be adjusted to a certain amplitude level. The lower corner frequency of the filter should be in the same region as the cable corner frequency to get a more stable attenuation line on the combination network at higher frequencies.

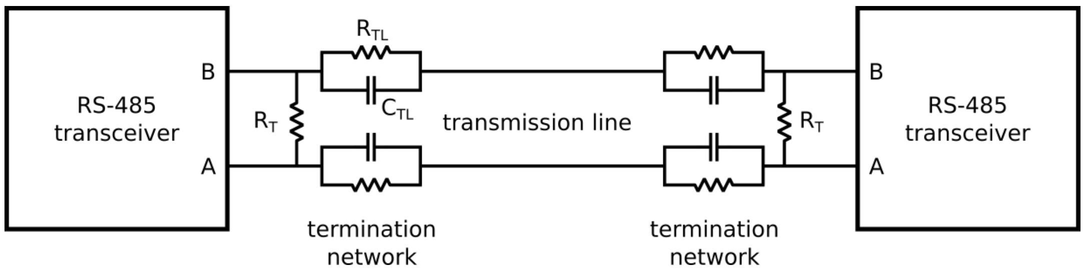

Figure 6. Passive RS-485 equalizer circuit

In practical terms a longer flat Bode curve means a more equal ratio between low and high frequencies, resulting in more stable, less data dependent edge transitions on the receiving side. But, at the same time, the differential signal amplitude will be reduced by the filter, taking away some noise margin, as illustrated in Figure 7.

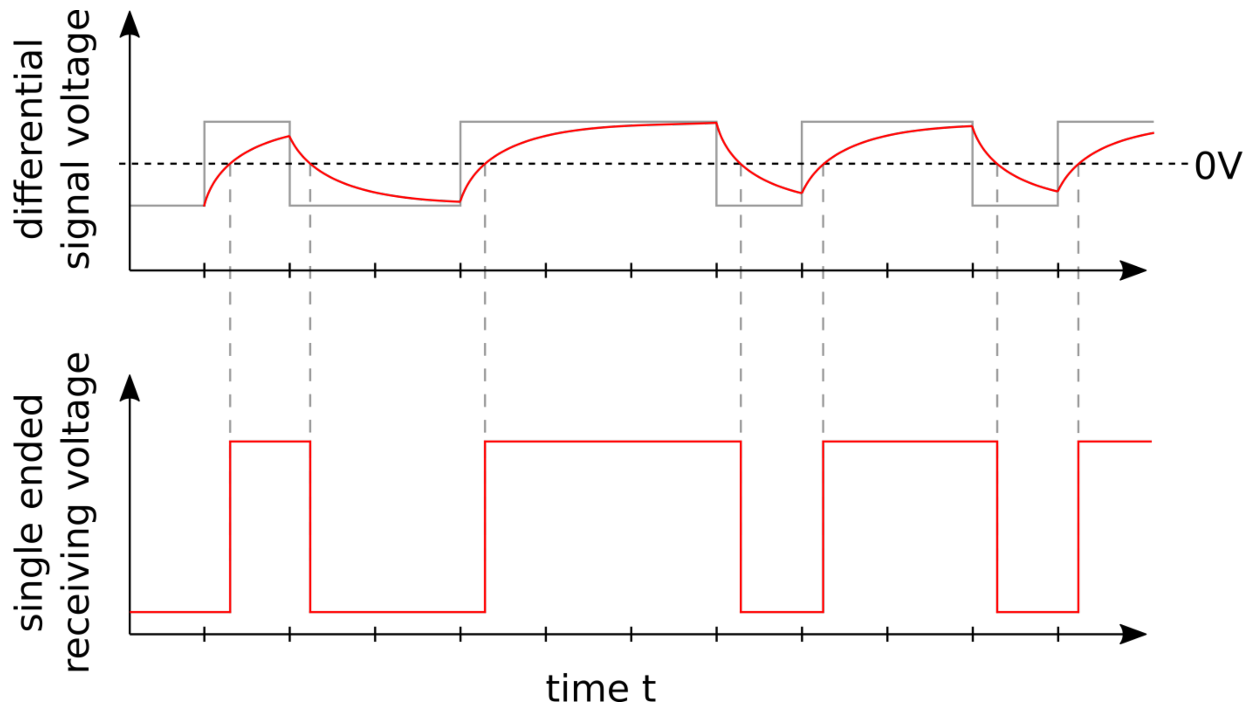

Figure 7. Top: Theoretical (gray) and real (red) differential signal with the passive RS-485 equalizer

Bottom: Output signal

Comparing Figure 7 to Figure 3 shows this effect: The rising and falling edges on the single ended receiving side are closer to the differential transition time, and are less dependent on the differential signal level at the beginning of a bit change. This decreases jitter on the far end of the cable, which allows faster bit rates to be applied.

The filter attenuation and corner frequencies are dependent on the resistor and capacitor combination. Since reflections are especially bad for high speed signals, and the capacitors are "conducting" at high frequencies, the termination resistors in parallel to the transceivers stay 100Ω to 120Ω depending on the used cable. Sometimes slightly smaller resistors can achieve better results, but this needs to be verified for each application or circuit.

The four resistors R_{TL} and R_T build a voltage divider for DC voltages, setting the attenuation at low frequencies of the filter. To achieve a good ratio between the high and low frequencies, R_{TL} should be as big as possible. But increasing R_{TL} reduces the signal amplitude and therefore also the noise margin and possible cable distance. A good tradeoff is using a R_{TL} to R_T ratio of ½.

This results in an attenuation of around -9.5dB for low frequencies, or an amplitude reduction of two thirds. It is important to understand that this reduction is necessary to achieve the desired performance, but it also reduces the noise immunity. Since the signal strength on the receiving side needs to be bigger than the +/-200 mV thresholds defined in the EIA-485 standard, and due to the cable characteristics, e.g. resistance of the cable, this can be a limitation.

The lower filter corner frequency must be adjusted to match the -3dB cable frequency by selecting the proper capacitor values. Unfortunately the capacitor values are highly dependent on the setup due to the parasitic inductances, capacitances, and resistances of the boards, connectors, and cables in the application and therefore no direct simple formula can be given. Each application will have to obtain this value through empirical measurement, or system-level simulation techniques. Some examples for the Belden 3105A cable shall be given in Table 1.

The transceiver used in the following example was a TI SN65HVD78 with a bit rate of 50Mbps across cables of 50, 100, and 150 meter lengths.

Table 1. Termination networks for different cable lengths

Cable length [m]	Termination resistor parallel [Ω]	Termination resistor series [Ω]	Termination capacitor series [pF]
50	120	60	340
100	120	60	340
150	120	60	390

2 Schematic

The schematic for the passive equalizer RS-485 reference design is shown below. The board identical to the RS-485 EVM, with the addition of capacitors C14-C17.

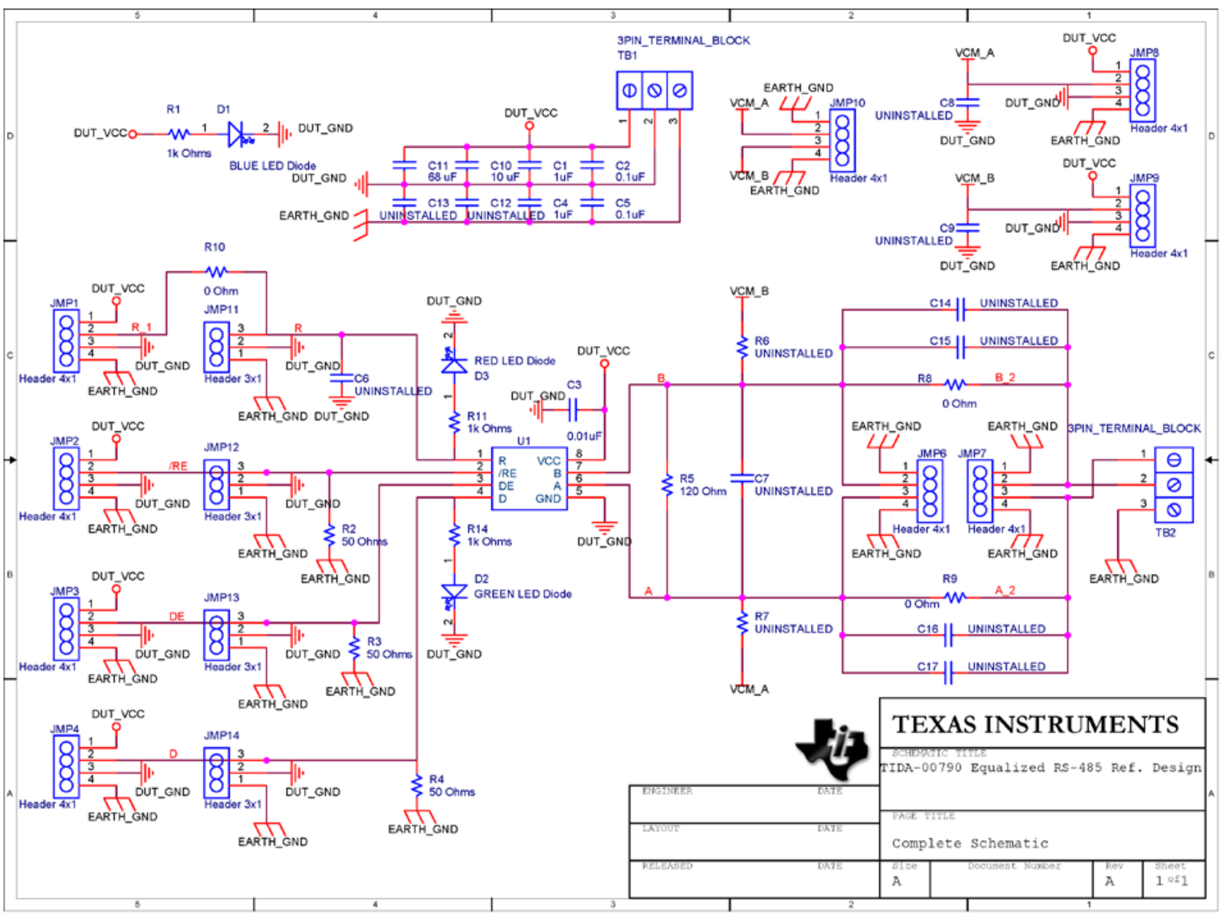

Figure 8. Schematic

3 Test Waveforms

The following waveforms were recorded using the SN65HVD78 3.3-V RS-485 transceiver and a DC power supply of 3.3 V. The function generator used a PRBS 2^16-1 data pattern in order to simulate a typical data stream.

Figure 9

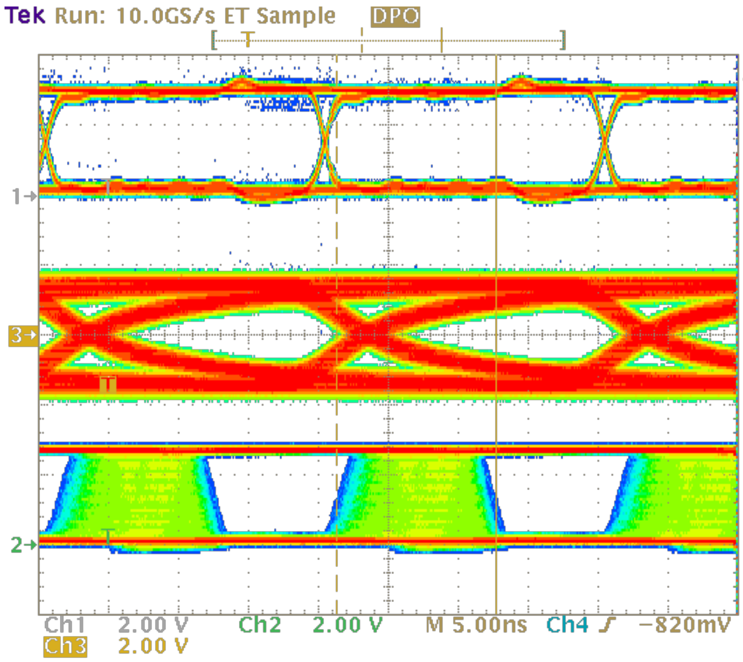

Figure 9. 120Ω reference termination resistor on a 100m cable at 50Mbps and 11.4ns jitter. Differential channel resolution is 2V/div.

For the measurement of the equalizer network, the differential channel 3 was changed to 1V/div.

Figure 10 shows a smaller jitter value than the value shown in Figure 9. This demonstrates the significant performance improvement that could be gained as a result of implementing the termination network.

The edges on the receiving channel 2 were also observed to not be 100% aligned; the rising edge is faster than the falling edge. This is because of the failsafe bias of the SN65HVD78 transceiver. The positive going threshold voltage is -70mV, and the negative going threshold voltage is -150mV, which results in the timing differences. This could be improved by selecting a receiver whose logic thresholds are symmetrical about 0 V or by adding a small negative differential offset in order to compensate for the effects of the failsafe biasing.Figure 9

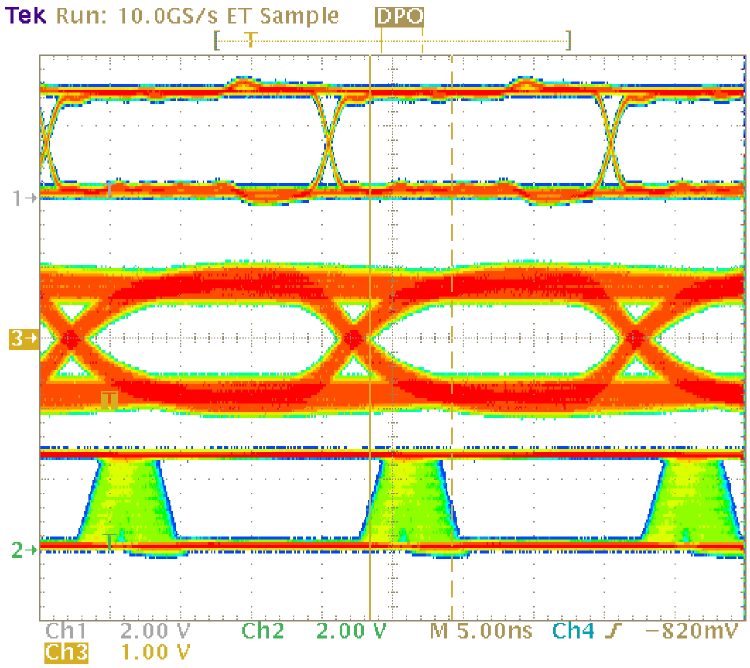

Figure 10. Passive equalizer eye diagrams on a 100m cable at 50Mbps and 5.8ns jitter. Parallel termination resistor 120Ω, series termination resistor 60Ω, series capacitor 680pF. Differential channel resolution is 1V/div.

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