# TI Designs Vision Analytics OMAPL-138-Based Hardware and Software Reference Platform

# Texas Instruments

# **Design Overview**

Vision analytics is a critical function for many industrial automated applications, including machine vision, inspection automation, surveillance, and image processing. This hardware and software design kit is optimized for vision analytic-based applications, and provides the all of hardware design elements, along with the C++ based foundational software, to get the reference design up and running quickly, letting you focus on adding differentiated application algorithms and features.

# **Design Resources**

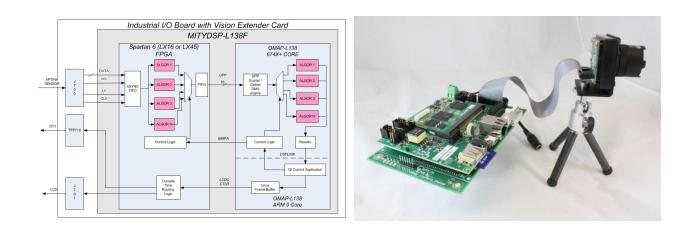
TI E2E<sup>f</sup>M Community

TIDEP0038	Design Folder
OMAP-L138	Product Folder
TMS320C64x Image Library	Software Folder
About CriticalLink	TI Design Network
MityDSP-L138F Overview	CriticalLink Website
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## **Design Features**

- Offers a Vision Development Kit (VDK) from CriticalLink, LLC that is a Complete Hardware and Software Framework Designed to Accelerate the Development of Vision Applications
- Includes Both a Xilinx Spartan<sup>®</sup> 6 FPGA and a TI OMAP-L138 Dual Core Processor
- Is Based on Critical Link's Production-ready MityDSP-L138F System on Module (SoM)
- Offers Source Design Files for the Base Industrial Input and Output Card and the Camera Expansion Cards
- Offers Easy Interface to OMAP-L138-based SOM.
- Offers Vision Algorithm Software Including Color Space Conversion, Edge Detection, Convolution, and Customer Processing Blocks with TI's Image Processing Library Software in Source Code
- Offers ARM-based GUI Software
- Supports Several Vision-Sensor Cameras in Monochrome or Color
- Offers a Wide Variety of Standard Peripherals Supported including ENET, USB, SATA, and LCD





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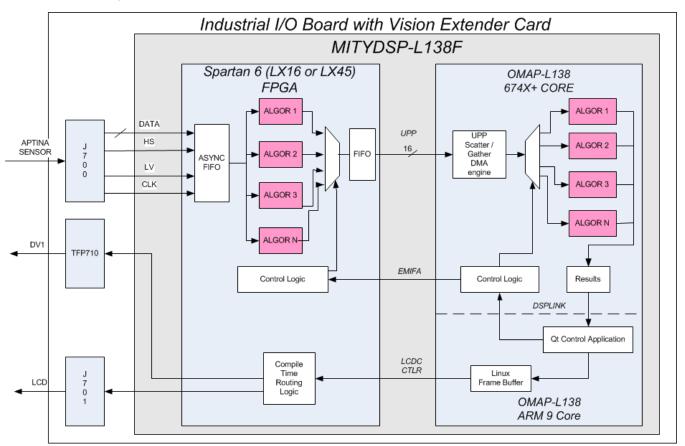
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#### **1** System Description

The system is designed to route raw video data from the CCD sensor board into the MityDSP-L138F. The FPGA captures the input data and performs optional user defined algorithms on the video data, then routes the data to the DSP core of the OMAP-L138 processor through the UPP interface.

The DSP then performs additional processing, and notifies the ARM core that the final processed video data (or results if no final video data is required) is available through a DSPLINK shared memory interface. The ARM accepts the data, and updates the local frame buffer with the needed results using a Qt drawing framework. Figure 1 shows a system block diagram for the Xilinx FPGA and DSP and ARM cores (TI OMAP-L138).





This document covers the following topics:

- Major system components: Sensor, FPGA, DSP, and ARM
- Hardware Design information
- · Key interfaces
- Development tools
- Getting started
- Examples

- Included components and ordering information
- About CriticalLink, LLC

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# 2 Design Features

# Features

- High Performance MityDSP-L138F CPU
  - TI OMAP-L138
  - Xilinx Spartan 6 FPGA
- Vision Sensor Boards Supported
  - 0.3 MP Monochrome
  - 0.3 MP Color
  - 1.0 MP Monochrome
  - 5.0 MP Monochrome
  - 5.0 MP Color
- Video Capture
- Image Analysis
- Linux<sup>®</sup> and HMI (Qt)

# Expansion

- UART Header (RS232 or RS485)
- WQVGA LCD Interface
- 4 Status LEDs
- 4-Pin GPIO Header

# **Featured Applications**

- Machine Vision
- Quality Control
- Semiconductor Inspection
- Image Processing (DSP and FPGA)

# **Digital Interfaces**

- DVI Video Output
- 10/100 Mbit Ethernet Interface
- Audio Output
- USB Host and OTG
- CAN Bus Interface
- SD/MMC Card Socket

# **Additional Hardware**

- AC to DC 12-V Adapter
- Tripod for Camera
- Pre-Loaded SD card
- Camera Lens
- Ethernet and Serial Cables

# 3 Block Diagram

Figure 2 shows the key components and interfaces for the VDK.

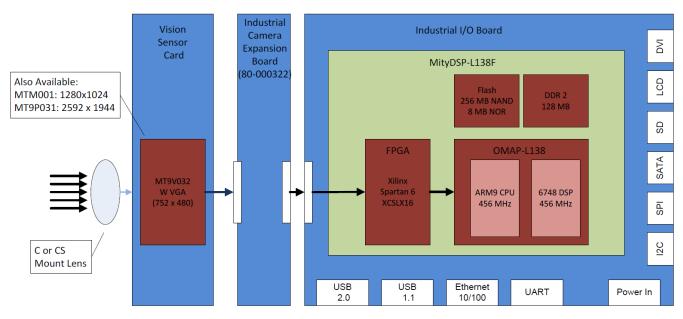


Figure 2. System Block Diagram for FPGA / DSP / ARM

# 4 Major System Components

#### 4.1 Sensor

The development kit comes standard with Aptina's monochrome Wide VGA sensor (MT9V032). This sensor supports a resolution of 752 × 480 pixels, and comes with a mount that accepts either a C or CS mount lens. A T0412 FICS-3 4-mm F1.2 Lens is included as the standard lens. In addition to the Wide VGA sensor, both the MTM001 (1280 × 1024 pixels) and MT9P031 (2592 × 1944) are also available. The MT9V032 and MT9P031 sensors are available in either monochrome or color format, and the MTM001 is monochrome only; refer to Section 11 for more details. Finally, custom sensor options are also available: contact Critical Link for additional details.

The sensor card connects directly to the Industrial Camera Expansion (80-000322) board through a 26-pin cable (included). This is an expansion board mounted beneath a Critical Link Industrial IO Development Kit through its three 50-pin expansion headers. Refer to Table 2 for datasheet information on both of these boards.

# 4.2 DSP

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Texas Instrument's C674x core (part of the OMAP-L138) provides the DSP processing function. The VDK framework in the OMAP receives the pixel data from the UPP port and makes it available to one or more processing elements (see Figure 2). A number of processing elements can be combined to make up the final desired processing. Once processing is completed, pixel data are presented to the DSPLink for transport to the ARM processor.

TI's C64x image processing library — provided in source form — includes numerous processing functions which are well-suited for image processing. Table 1 shows a summary of the available functions. The Vision Development contains instructions on adding your own additional algorithms to the DSP reference design provided. This information is provided in the VDK Algorithm Addition.pdf document included on the VDK DVD.

Boundary and Perimeter Detection	Median Filtering	
Dilation and Erosion	Pixel Expansion	
Edge Detection	Forward and Reverse DCT	
Thresholding	Motion Estimation	
Color Space Conversion	MPEG-2 Variable Length Encoding	
Convolution	Quantization	
Correlation	Wavelet Processing	
Error Diffusion	Background Subtraction	

Table 1. Summary of TI's C64x Image Processing Functions <sup>(1)</sup>
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(1) Additional information on TI TMS320C64x Image Processing library: http://focus.ti.com/docs/toolsw/folders/print/sprc094.html

# 4.3 ARM

The 456-MHz ARM9 runs Linux<sup>®</sup> (Open Embedded Angstrom distribution) and is responsible for all embedded computing type tasks, such as managing a GUI, communication stacks, and file system. A robust GUI is available through Qt, and both Ethernet and USB communication stacks are available in addition to all standard Linux facilities and tools.

The VDK contains instructions on modifying the provided QT GUI reference design. This information is provided in the VDK Algorithm Addition.pdf document included on the VDK DVD.

# 4.4 FPGA

A Xilinx Spartan 6 XCSLX16 FPGA is the first part of the processing chain. It receives sensor data and performs any time-critical functions best suited for the FPGA (vs. software). The FPGA is architected to receive sensor data and make it available for the algorithm processing blocks (see Figure 2). Once FPGA processing is completed, the pixel data is transmitted to the OMAP-L138 over the UPP port.

Examples of functions which may be performed in the FPGA include:

- Color space conversion
- Edge detection
- Convolution
- Custom processing blocks

The VDK contains instructions on adding your own custom algorithms to the base FPGA design provided. This information is provided in the VDK Algorithm Addition.pdf document included on the VDK DVD.



#### 5 Hardware Design Information

As shown in Figure 2, the Vision Development kit is comprised of four different printed circuit boards (PCBs). Each of these boards (MityDSP-L138F, Sensor, Industrial IO Board, and Industrial Camera Expansion (80-000322) Board) have their own datasheets. The Industrial IO and Industrial Camera Expansion Boards also have schematic, BOM, and gerber PDFs available. Copies of all of these files are available at the following locations, as shown in Table 2.

File Description	File Type	File Location	
MityDSP-L138F	Datasheet	http://www.criticallink.com/product/mitydsp -l138f-dev-kit/	
Sensor	Datasheet	Contact CriticalLink, LLC: info@criticallink.com	
Industrial IO	Design Guide	L138-1808-1810 Development Kit DVD and http://www.criticallink.com/wp- content/uploads/2014/01/MityDSP-L138F- Carrier-Board-Design-Guide.pdf	
Industrial IO	Schematic	L138-1808-1810 Development Kit DVD or http://www.ti.com/tool/TIDEP0038	
Industrial IO Bill of Materials		L138-1808-1810 Development Kit DVD or http://www.ti.com/TIDEP0038	
Industrial IO	Industrial IO Gerbers		
Industrial Camera Expansion Board (80- 000322)	Datasheet	Contact CriticalLink, LLC: info@criticallink.com	
Industrial Camera Expansion Board (80- 000322)	Schematic	Vision Development Kit DVD or http://www.ti.com/tool/TIDEP0038	
Industrial Camera Expansion Board (80- 000322)	Bill of Materials	Vision Development Kit DVD or http://www.ti.com/tool/TIDEP0038	
Industrial Camera Expansion Board (80- 000322)			

#### Table 2. Vision Development Kit Hardware Design File Locations

#### 6 Key Interfaces

One of the primary benefits of using Critical Link's Vision Development Kit is that the transport of pixel data from sensor through the FPGA, DSP, and ARM processors has been developed and optimized. This infrastructure is essential to deploying a complete system, but can take many months of effort to develop and perfect. All the key interfaces are provided with the framework and are summarized in Table 3.

From	То	Hardware Interface	Data Rate
Sensor	FPGA	Direct Sensor Interface	Up to 200 M Pixel/sec
FPGA	DSP	UPP Port	Up to 75 MHz (at 16 bits)
DSP	ARM	DSPLink <sup>(1)</sup> Share memory interface	
ARM	Host	USB, Ethernet (10,100)	Various data rates

#### Table 3. Vision DK Interface Summary

(1) DSPLink is a framework provided by TI for DSP / ARM communication. This framework includes facilities for transporting data between ARM and DSP, as well as code download and DSP reset. Critical Link has enhanced DSPLink by providing wrapper functions that allow both ARM and DSP applications easy access to data movement.



#### 7 Development Tools

This VDK leverages existing development tools from Xilinx and TI, and should fit seamlessly within the standard development environment. The development tools are available at <a href="https://support.criticallink.com/redmine/projects/indio/wiki/Vision\_framework\_kit">https://support.criticallink.com/redmine/projects/indio/wiki/Vision\_framework\_kit</a> and are summarized in .

Further information concerning many MityDSP-L138 topics can be found at http://support.criticallink.com/redmine/projects/arm9-platforms/wiki.

Table 4. Summary o	Development Tools
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Component	Development Tools	Version	Tool Location
FPGA	Xilinx ISE Webpack Version 13 or Higher	13 or higher	http://support.criticallink.com/redmine/projects/a rm9- platforms/wiki/FPGA Development Tools
	JTAG Programming Cable		http://support.criticallink.com/redmine/projects/a rm9- platforms/wiki/FPGA Development Tools
DSP	TI Code Composer (CCS)	5.2 or higher	http://processors.wiki.ti.com/index.php/Downloa d
	Spectrum Digital JTAG Emulator	XDS510 preferred	http://support.criticallink.com/redmine/projects/a rm9- platforms/wiki/DSP Development Tools
ARM	Eclipse IDE	Provided with CCS	http://support.criticallink.com/redmine/projects/a rm9- platforms/wiki
	GCC tool chain	Nov 2010	http://support.criticallink.com/redmine/projects/a rm9- platforms/wiki/GCC_Toolchain



#### Getting Started

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# Getting Started

Starting a project started using the Vision Development Kit from Critical Link is a straightforward process:

- 1. Identify the application and generate a vision algorithm.
- 2. Select a test or verification vehicle, which may be a Matlab or a general C++ programming environment.
- 3. Develop, debug, and verify algorithms on the selected platform. Once you have validated the algorithms, port them to the target hardware (Vision Development kit).
- 4. Set up a development environment for the MityDSP-L138F Vision Framework
  - VDK Environment Setup.pdf included on VDK DVD
    - Base L138-1808-1810 Linux Virtual Machine Development Environment
    - Update with supplemental Vision Development Kit specific files.
- 5. To facilitate quick addition of a new algorithm, a step-by-step document has been created to cover adding algorithms to either the FPGA or DSP and accessing them in the ARM Qt GUI application. Follow the Vision DK Algorithm Addition.pdf document included on the Vision Development Kit DVD.
  - Port algorithm to Vision DK
    - Convert to C++ (if using Matlab and the DSP)
    - Use a Vision DK algorithm block calling convention: Pointer to data-in, size, and pointer to data\_out.
    - Add algorithm to the ARM GUI.
- 6. Verify the algorithm on the target hardware.

# 9 Examples

The development kit is provided with the examples shown in Table 5, meant to illustrate basic functionality.

Mode	Description	
Raw Mode	Camera data is aligned to 16-bit integers and copied to frame buffer as 5-6-5 output	
Gray Scale (FPGA)	Camera data treated as monochrome data and is converted to gray scale color using 5-6-5 LCD color mapping (effective 32 levels of colors). Conversion done in FPGA	
Gray Scale (DSP)	Camera data treated as monochrome data and is converted to gray scale color using 5-6-5 LCD color mapping (effective 32 levels of colors). Gray scale conversion done in DSP	
Bayer Color Conversion (DSP)	Camera data is treated as color information formatted in standard Bayer pattern. The Bayer pattern is converted to standard 5-6-5 LCD color for display on LCD	
Sobel 3 × 3 Edge Detection	Camera data is treated as monochrome and 3 × 3 edge detection algorithm is run on the DSP, with result converted to gray scale (5-6-5) 32 levels color map display	

#### Table 5. Vision DK Examples

# 10 Included Components

Table 6 lists the components included with a Vision Development Kit. Refer to Table 7 for specific development kit ordering information.

Description	Qty. Included
Vision Development Kit Board Set	1
MityDSP-L138F Module	1
Selected Camera Sensor with Lens, Tripod and Cable	1
Null Modem Serial cable M/F and 10-pin adapter	1
12-V 1.2-A AC to DC Supply	1
Ethernet cable – 7 foot	1
DVD with L138-1808-1810 Development Environment	1
DVD with Vision Development Kit Supplemental Files	1

## Table 6. Included Items

# 11 Ordering Information

Table 7 lists the orderable module configurations. For shipping status, availability, and lead time of these or other configurations, contact your Critical Link representative.

Model	Sensor	Color/Monochrome	Resolution	SoM	FPGA
80-000492	MT9V032	Monochrome	WVGA (752 × 480 pixels)	L138-FG-225-RC	6SLX16
80-000493	MT9V032	Color	WVGA (752 × 480 pixels)	L138-FG-225-RC	6SLX16
80-000494	MT9M001	Monochrome	XGA (1280 × 1024 pixels)	L138-FG-225-RC	6SLX16
80-000495	MT9P031	Monochrome	5 M Pixel (2592 × 1944 pixels)	L138-FG-225-RC	6SLX16
80-000496	MT9P031	Color	5 M Pixel (2592 × 1944 pixels)	L138-FG-225-RC	6SLX16

#### **Table 7. Orderable Model Numbers**

Included Components



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# 12 About CriticalLink, LLC

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Critical Link is an embedded systems firm specializing in developing electronics for the scientific, industrial, communications, and transportation industries. The business is built around working with industry innovators bringing new products to market, and around leading-edge digital processing platforms. Critical Link's robust methodology, framework of designs, pre-engineered interface cores, device support, and tools help customers bring their applications to market more cost effectively, more rapidly, and with higher quality than if they build from the ground up.

#### Solutions

MitySOM/MityDSP provides an all-in-one solution for your instrumentation, data collection, and control needs. A product development and production system, MitySOM/MityDSP provides a production-ready core CPU platform that can be quickly and easily customized to meet your specific product requirements through configurable input and output interfaces. The MitySOM/MityDSP includes both hardware and software components that integrate seamlessly into your application, providing a fully customized embedded design that both reduces project technical risk and shortens development cycles and cost.

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