TI Designs

Reference Design for Interfacing Current Output Hall Sensors and CTs With Differential ADCs/MCUs

Design Overview

This design provides a reference solution for interfacing current output Hall sensors and current transformers (CTs) to differential ADCs (standalone and integrated into MCU). The differential signal conditioning circuit is designed to measure motor current with an accuracy of ±0.5% across the operating temperature range from −25°C to +75°C. The output common-mode voltage of the differential amplifier can be selected to either 1.25 V or 2.5 V.

Design Resources

TIDA-00368	Design Folder
TPS62150	Product Folder
TPS7A3001	Product Folder
TPS7A4901	Product Folder
OPA322	Product Folder
THS4531A	Product Folder
TLV1702	Product Folder
LP2992A-5.0	Product Folder
REF2025	Product Folder

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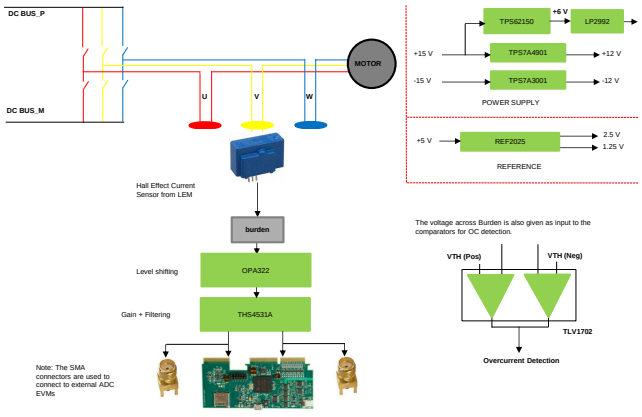
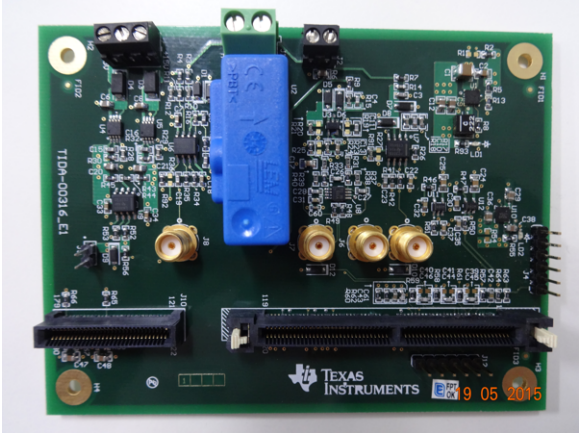
Design Features

- Onboard Current-Output Hall Sensor to Measure Nominal Current up to 25-A RMS
- Current Measurement Accuracy of 0.5%
- Common Reference Solution for Interfacing Both CT and Current Output Hall Sensor With Differential ADC or MCU
- Selectable Output Common-Mode Voltage for Differential Amplifier
- Designed to Evaluate With Delfino F2837x Control Card
- Designed to Evaluate With External ADC (ADS8354) for Interfacing With Motor Controller

Featured Applications

- AC Variable Speed Industrial Drives
- Servo Motor Drives
- UPS Systems
- Solar Inverters
- AC/DC and DC/DC Power Supplies





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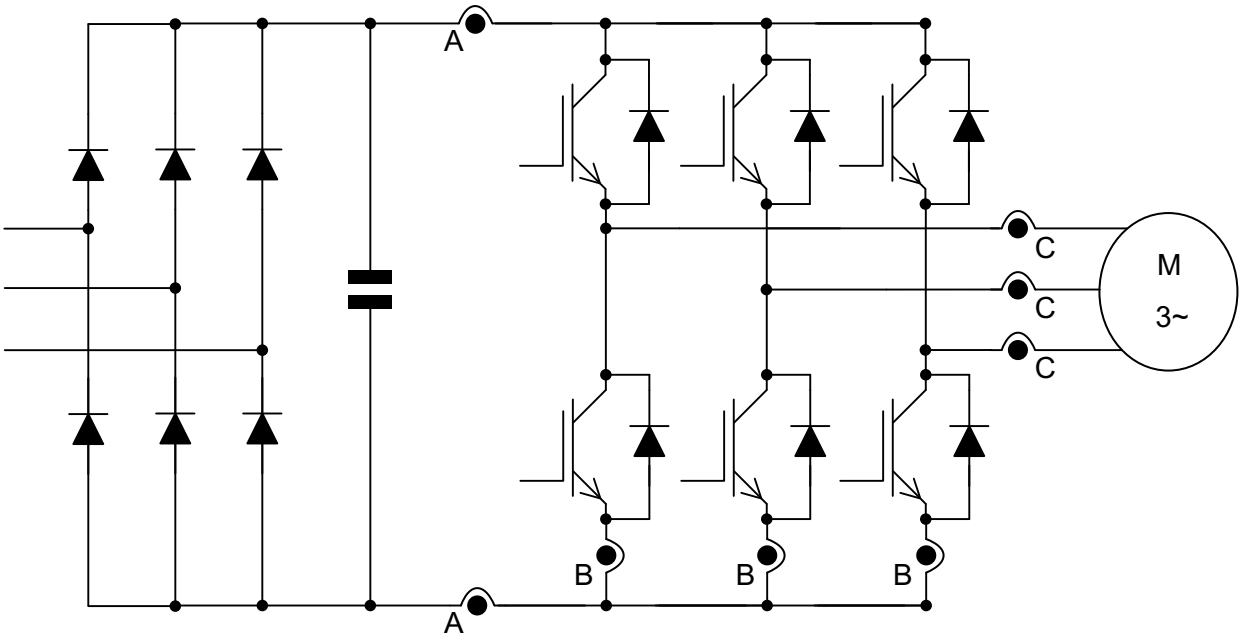
1 System Description

Current measurement is an inherent part of any inverter-driven application. One important reason for measuring the motor current is to perform a control algorithm. Vector control and direct torque control require current sensing for control purposes. Information regarding motor parameters is also important for several control schemes. The stator current measurement is used to estimate these parameters. The current measurement is also used for hardware overload and earth fault protection.

The inverter output rating must be derated while operating at higher temperatures. Higher temperatures can be to the result of increased ambient temperature, a faulty fan, or obstructions in cooling path. In these scenarios, the current measurement assists in derating the inverter current to keep the power devices within its permissible range of operating temperatures.

The motor current can be measured at different locations in the inverter. Figure 1 shows an overview of the usual measurement locations, considering a three-phase inverter for a motor control application:



A) Current measurement in the DC- and DC+ link
B) Current measurement in the bottom side emitter path of each half-bridge
C) Current measurement in the output phases

Figure 1. Typical Measuring Locations for Current Measurement in Motor Drives

The cheapest variant “A” of current measurement is often used for applications in the lower power range. Typically, the current measurement is done on the DC minus bus. Because this location may be used as the reference potential of the MCU, isolating the signal is not necessary. Variant “C” is another location for current measurement and is located primarily in the low-to-medium power range. In the case of this design, the current is measured at the emitter of the bottom insulated-gate bipolar transistor (IGBT) of each arm in a three-phase inverter. The third current measurement may not be necessary, as the user can derive this value from calculations based on the measured two current signals. The advantage of variant "B" is similar to that of variant "A", in that the negative section of the DC-bus can be taken as the common reference potential. However, a disadvantage of measuring variant "B" is the increased stray inductance. In high dynamic drives and high-power applications, current is usually measured in the output phases of the inverter (variant "C" in Figure 1). The third current sensor is not necessary in this case, either.

The TIDA-00368 design is intended for current measurement using current-output Hall-effect sensors in the AC and DC drives (variant C). The goal of this design is to provide a reference solution for a differential signal conditioning circuit to measure motor current using current-output Hall effect sensors and current transformers (CTs). Current output Hall effect sensors are typically available from companies like LEM Technologies www.lem.com and VACUUMSCHMELZE or VAC www.vacuumschmelze.com.

One very common method to measure current is to use single-ended ADCs integrated into the controller. Single-ended measurements are more prone to noise in a larger drive system, which can lead to inaccuracies in the measurement. Differential measurement helps to overcome the noise issues. The Texas Instruments Delfino™ series of microcontrollers (consisting of differential input ADCs), make it possible to measure the differential signals overcoming the noise interference.

The signal conditioning circuit for Hall-effect sensors is required for the following reasons:

- Current output Hall sensors are typically powered from ±12 V or ±15 V leading to a bipolar output swing. Interfacing this output swing to an ADC with a 3.3-V reference requires an amplifier and level shifting.
- With industrial motor drives, using the sensor until 200% to 250% of its rating is fairly common. Detecting the overload condition and protecting the drive is important.
- Higher input offset voltage, temperature drift, noise, and linearity leads to error in motor current measurements, which also affects control loop performance. The proper implementation of a signal conditioning circuit reduces the errors and noise from the sensors.
- If using a differential ADC inside a Texas Instruments Delfino™ MCU from the F2837x series, the common-mode voltage must be shifted from 2.5 V to 1.25 V.

2 Block Diagram

Figure 2 shows the system block diagram for the TIDA-00368 design. The design uses an onboard current-output Hall effect sensor to measure the motor current. A provision exists to connect an external CT to the signal conditioning circuit for the purposes of current measurement. The burden resistor is available on the board for both Hall effect sensors and CTs.

The voltage across the burden resistor is signal-conditioned using the OPA322 and THS4531A devices. The output of the signal conditioning circuit is connected to:

1. 180-pin connector to interface with the internal ADC of the Delfino™ F2837x series of MCUs
2. SMA connectors to evaluate the performance of the signal conditioning circuit with external ADCs like ADS8354

The Hall effect sensor is powered using a power supply of ±12 V, which is generated from ±15 V using TPS7A4901 and TPS7A3001 linear regulators. The signal conditioning circuit is powered using 5-V DC generated from the +15-V supply. The +5 V is used to power the OPA322 and THS4531A operational amplifiers (op-amps). For the THS4531A, the output common-mode voltage (VOCM) can be set at +2.5 V when used with external 5-V ADCs or +1.25 V when used with the internal ADC of a Delfino F2837x controller. The REF2025 reference is used to generate the reference voltage of +1.25 V and +2.5 V.

To provide protection against overcurrent fault conditions, feed the sensed current to two comparators, which are available in a single device, the TLV1702. One comparator is for the detection of overcurrent in a positive half-cycle and the other is for the detection of overcurrent in a negative half-cycle. Both protection circuits have a response time of less than 500 ns.

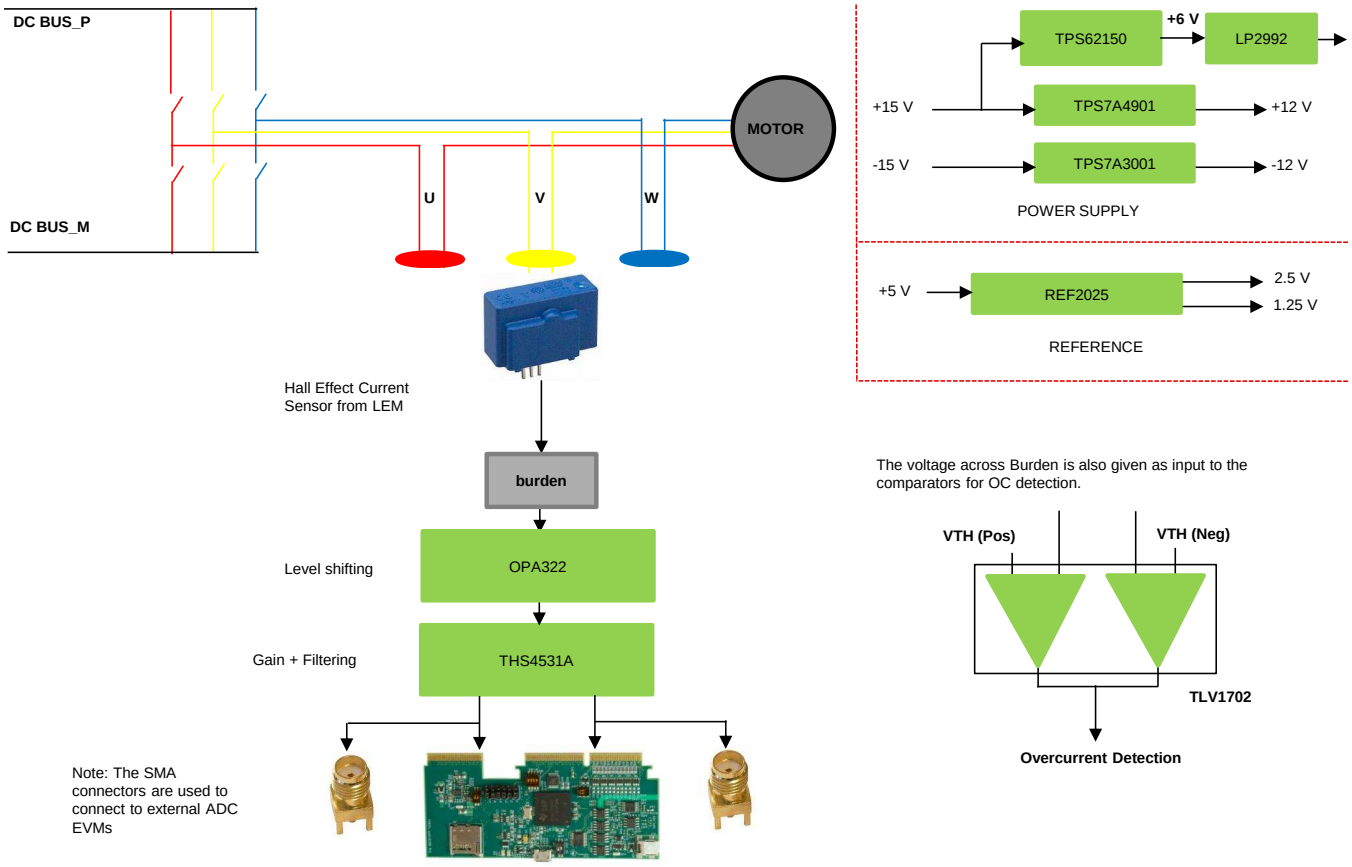


Figure 2. TIDA-00368 System Block Diagram

2.1 Highlighted Products

The TIDA-00368 reference design features the following devices from Texas Instruments:

- TPS62150 – A step-down (buck) regulator with a 3- to 17-V input, 0.9- to 6.0-V output, −40°C to 85°C, 16-pin QFN (RGT), and a green (RoHS and no Sb/Br) planned eco-friendly classification.
- TPS7A3001 – A single-output, high-power supply rejection ratio (PSRR) low-dropout regulator (LDO) with a 200-mA, adjustable −1.18- to −33-V output and −3- to −36-V input. The device features ultra-low noise, an 8-pin MSOP (DGN), –40 to 125°C operating temperature, and a green (RoHS and no Sb/Br) planned eco-friendly classification.
- TPS7A4901 – A single-output, High PSRR LDO with a 150-mA, adjustable 1.2- to 33-V output, 3- to 36-V input. The device features ultra-low noise, an 8-pin MSOP (DGN), −40°C to 125°C operating temperature, and a green (RoHS & no Sb/Br) planned eco-friendly classification.
- OPA322 – A 20-MHz, low-noise, rail-to-rail input and output (RRIO), CMOS operational amplifier with a 1.8- to 5.5-V range, −40°C to 125°C operating temperature, 8-pin SOIC (D0008A), and a green (RoHS and no Sb/Br) planned eco-friendly classification.
- THS4531A – An ultra-low power, rail-to-rail output (RRO), fully-differential amplifier.
- TLV1702 – A dual, 2.2- to 36-V micropower comparator.
- LP2992AILD-5.0/NOPB – A micro-powered, 250-mA, low-noise ultra-low-dropout regulator in a 6-pin LLP (Pb-free).
- REF2025 – A dual-output voltage reference DBV0005A with a 2.5-V load current.

For more information on each of these devices, see the respective product folders at www.TI.com or click on the links for the product folders on the first page of this reference design under Design Resources.

3 Hall Sensors

3.1 Closed-Loop Hall Effect Sensor

The conductor that carries a current IP (see Figure 3) generates a magnetic field, which is concentrated in a magnetic circuit. This field can be measured in an air gap by using a Hall element. The Hall element has the property of converting the magnetic flux into a voltage, when the element is supplied with a constant current IC. When applying the closed-loop principle, the Hall voltage is only used for balancing the primary and the secondary flux. The additional secondary coil (with 2,000 turns, for example), carries a current, IS (which equals 1/2000th of the primary current), to precisely compensate for the field of the primary conductor. The total flux then equals zero. Operating the Hall generator in a zero flux condition eliminates the drift of gain with temperature. When the magnetic flux is fully compensated (zero), the magnetic potential (ampere-turns) of the two coils is identical; so, Equation 1 can be calculated as:

$$N_P \times I_P = N_S \times I_S \text{ which can also be written as } I_S = I_P \times N_P / N_S \quad (1)$$

Consequently, the secondary current, I_S, is the exact image of the primary current, I_P, being measured. Inserting a “measurement resistor”, R_M, in series with the secondary coil creates an output voltage that is an exact image of the measured current. To give an order of magnitude, the typical number of secondary turns is N_S = 1000 to 5000 and the secondary current is usually between I_S = 25 mA to 300 mA, although it can be as high as 2 A.

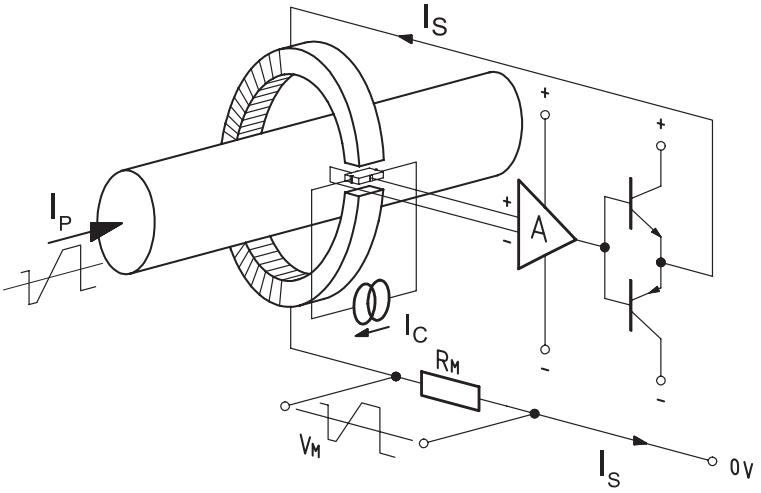


Figure 3. Operating Principle of Closed-Loop Hall Transducer

3.2 Advantages and Limitations

Closed-loop transducers are capable of measuring DC, AC, and complex current waveforms while ensuring galvanic isolation. The advantages of closed-loop sensors include very good accuracy and linearity, low gain drift, wide bandwidth, and fast response time. Another advantage is that the output current signal is easily scalable and well-suited to high noise environments; nevertheless, closed-loop transducers are available in voltage output configurations. Again, as with most magnetic-based measurement techniques, insertion losses are very low. The main limitations of the closed-loop technology are the high current consumption from the secondary supply (which must provide the compensation as well as bias current), the larger dimensions (more noticeable on high current transducers), a more expensive construction compared with the simpler open-loop designs, and a limited output voltage due to the internal voltage drops across the output stage and secondary coil resistance. Again, depending on the application requirements, the advantages often outweigh the limitations and the accuracy and response of a closed-loop solution is desirable over other alternatives.

3.3 Details of Hall Sensor "LAH 25-NP" from LEM Technologies

Selecting the right transducer is often a tradeoff between several parameters: operating current range, output signal type, accuracy, frequency response, dv/dt, temperature range, weight, size, costs, and so forth. The LAH 25-NP is a closed-loop (compensated), multi-range current transducer from LEM Technologies that uses the Hall effect. This transducer is typically used for the measurement of current (DC, AC, or pulsed) with galvanic separation between the primary and secondary circuit. Figure 4 shows the internal structure of the LAH 25-NP device.

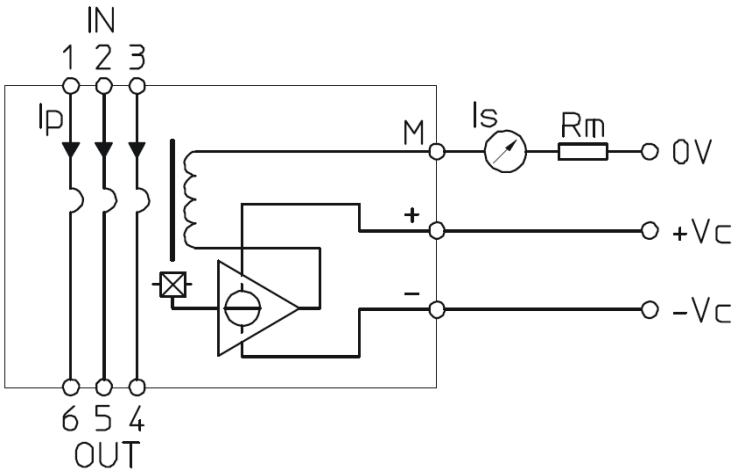


Figure 4. Internal Structure of LAH 25-NP

The LAH 25-NP transducer uses a dual power supply and provides the current output from pin "M". The output (or secondary) current is proportional to the primary current and turns ratio.

Closed-loop Hall sensors provide an excellent accuracy at 25°C (generally below 1% of the nominal range), and a reduced error over the specified temperature range (−40°C to +105°C). Table 1 shows the accuracy data for the LAH 25-NP transducer (taken from the datasheet).

Table 1. Accuracy—Dynamic Performance Data From LAH 25-NP

PARAMETER	SPECIFICATION	VALUE	UNIT
X	Accuracy at IPN, TA = 25°C	±0.3	%
ε_L	Linearity error	< 0.2	

4 Component Selection

4.1 Calculation of Burden Resistor for LAH 25-NP

The burden is calculated according to procedure given in the “Technical Manual” from LEM Technologies (4). The measuring voltage generated at the terminals of the burden resistor (V_M) depends on the amplitude of the primary current, I_P; the turns ratio of the transducer, K_N; and the measuring (or burden) resistor, R_M. The nominal current, I_{PN}, determines the type of transducer and its turns ratio, K_N. The voltage measured at a given primary peak current I_P is determined by the choice of the resistor R_M.

- Nominal current to be measured: 8 A
- Peak current → Overload condition: 225% of the nominal, that is 8 × 2.25 = 18 A
- Ambient temperature: 70 °C
- Transducer supply voltage: ±12 V
- Referring to the datasheet of LAH 25-NP, the PCB connection must be as Figure 5 shows in the third, encircled row. For this condition, the value of K_N is equal to 3:1000.

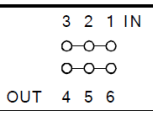
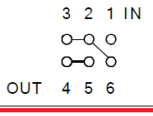
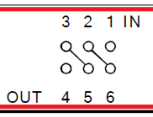
Number of primary turns	Primary current nominal I_{PN} [A]	Primary current maximum I_P [A]	Nominal output current I_{SN} [mA]	Turns ratio K_N	Primary resistance R_P [mΩ]	Primary insertion inductance L_P [µH]	Recommended PCB connections
1	25	55	25	1 : 1000	0.18	0.012	
2	12	27	24	2 : 1000	0.81	0.054	
3	8	18	24	3 : 1000	1.62	0.110	

Figure 5. Recommended PCB Connections and Corresponding Parameters

4.1.1 Calculation of R_M for 5-V ADC System

For a 5-V ADC, the mid-voltage value is 2.5 V. Keeping a margin of 0.25 V, the range of input voltages for a 5-V ADC is 0.25 V to 4.75 V. This range indicates that the voltage across the burden must be 2.25 V when the primary current is at its peak value.

For a positive peak current through the primary of the Hall sensor → 2.5 V + 2.25 V = 4.75 V
For a negative peak current through the primary of the Hall sensor → 2.5 V − 2.25 V = 0.25 V

The following Equation 2 shows the calculation of R_M for a 5-V system.

$$R_M = \frac{V_M}{I_P \times K_N} \tag{2}$$

Use Equation 2 for the following values:

- V_M = 2.25 V
- I_P = 18 A
- K_N = 3:1000
- R_M = 41.67 Ω

The selected value of R_M is 42.2 Ω for the purposes of testing.

4.1.2 Calculation of R_M for 3.3-V Differential ADC System

For a 3.3-V differential ADC, the V_{REF} = 2.5 V, so the mid-voltage value is 1.25 V. Keeping a margin of 0.25 V, the range of input voltages for the ADC is 0.25 V to 2.25 V. This range indicates that the voltage across the burden must be 1 V when the primary current is at its peak value.

For a positive peak current through the primary of the Hall sensor → 1.25 V + 1 V = 2.25 V
For a negative peak current through the primary of the Hall sensor → 1.25 V – 1 V = 0.25 V

Use Equation 2 for the following values:

- V_M = 1 V
- I_P = 18 A
- K_N = 3:1000
- R_M = 18.52 Ω

The selected value of R_M is 18.2 Ω for the purposes of testing.

4.2 Selection of Power Supply Components

The current sensor (LAH 25-NP) requires bipolar supply rails of ±12 V, so the board is designed to be powered from ±15 V (max).

From a ±15-V input, mainly two different voltages are derived:

1. ±15 V to ±12 V for a Hall sensor as well as comparator.
2. 15 V to 5 V for supplying a unipolar-supply op-amp, onboard voltage reference device, or Delfino controlCARD.

For applications requiring positive as well as negative high-performance rails (to power precision signal chain components), the TPS7A49XX and TPS7A30XX devices are most suitable.

With a 15- to 5-V generation, using a linear regulator is not a good option, as it consumes more power. A 5-V rail is used to power the op-amps, which are important elements of the signal conditioning process. The rail must be clean and free of noise. Due to the above reasons, this design allows the use one switching buck converter followed by a linear regulator.

The TIDA-00368 design uses the following components:

- 15- to 6-V conversion using a TPS62150 converter
- 6- to 5-V conversion using a LP2992 voltage regulator

4.3 Selection of Differential Amplifier

The fully-differential amplifier (FDA) is a critical piece of the analog signal chain and can often have a dramatic impact on the performance of the entire signal chain. The primary functions of an FDA used in this design are:

1. To provide amplification of the low-level input signals coming from the sensor
2. To provide the desired common-mode voltage at the output
3. To provide proper filtering for the signal connected to the ADC

Table 2 provides a comprehensive list of the factors that must be considered when selecting the operational amplifier.

Table 2. Selection Considerations for FDA

REQUIREMENT	BENEFITS
High input impedance	Minimizing this reduces input loading on sensor, minimizes input current offsets on input resistors
Input current noise	Minimizing this reduces the amount of current noise that converts to voltage noise on input resistors
Voltage noise	Minimizing this improves the overall signal-to-noise ratio (SNR)
CMRR versus frequency	Maximizing this reduces the amount of input offset changes due to 50- or 60-Hz common noise coupling common noise coupling on the inputs
Resistive gain matching	Maximizing this improves the total unadjusted system error
Voltage offset drift	Minimizing this reduces the amount that the total unadjusted error changes at the output of the amplifier
Single supply operation	Designing a single supply amplifier simplifies the system supply requirements; this usually correlates with a lower power architecture
Low power	Enables use in power-sensitive or battery monitoring applications
Input type	Using differential input structure can improve common-mode noise rejection
Output type	Using differential output structure can improve common-mode noise rejection at the ADC inputs as well as potentially reduce or relax the signal conditioning circuitry

This reference design uses the THS4531A device as a front end amplifier for the ADC. The THS4531A is a fully differential op-amp and can be used to amplify differential input signals to differential output signals. Figure 6 shows a basic block diagram of the circuit (VOCM and PD inputs are not shown). The gain of the circuit is set by RF divided by RG.

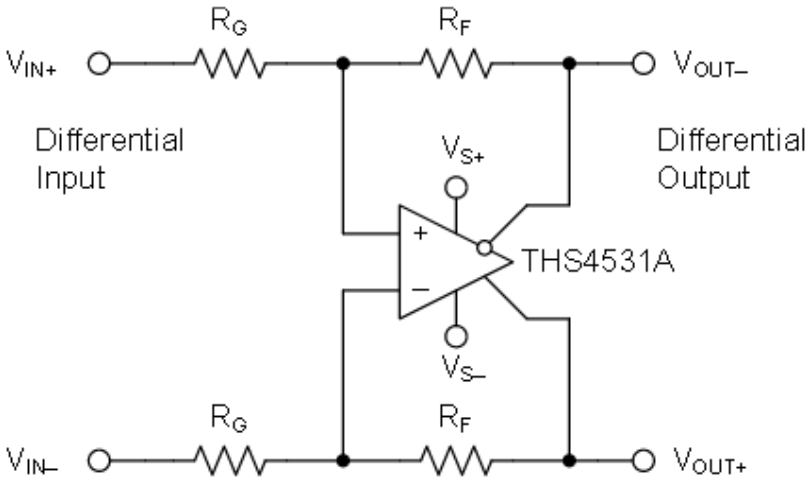


Figure 6. Differential Input Differential Output Amplifier

The output common-model voltage for the THS4531A device is set by the voltage at the VOCM pin and the internal circuit works to maintain the output common-mode voltage as close as possible to this voltage. If left unconnected, the output common-mode is set to mid-supply by internal circuitry, which may be overdriven from an external reference source.

4.4 Selection of Voltage Reference

When external ADCs (which are powered using a 5-V single supply) are used for capturing the data, the reference voltage must be set to 2.5 V. When internal ADCs (of a Delfino controller) are used in differential mode, the reference pin must be powered from a 2.5-V reference (Delfino converts 2.5 V into a 1.25-V reference, internally). Two reference voltages are required to fulfill all these conditions (2.5 V and 1.25 V).

The REF20xx series provides a reference voltage (V_{REF}) and a second highly-accurate voltage (V_{BIAS}) that can be used to bias the input bipolar signals. The V_{REF} and V_{BIAS} outputs track each other with a precision of 6 ppm/°C (max) across the entire temperature range. The REF20xx family is specified to deliver a current load of ±20 mA per output. Both the V_{REF} and V_{BIAS} outputs of the device are protected from short circuits by limiting the output short-circuit current to 50 mA.

4.5 Selection of Comparator

Present-day state-of-the-art inverters are equipped with full IGBT protection, including overcurrent and ground-fault protection. An overcurrent condition is one of the fatal drive faults that can destroy IGBT devices in a motor-drive system. IGBT overcurrent conditions basically fall into three categories: line-to-line short, ground fault, and shoot through.

Table 3 lists overcurrent conditions and their potential causes. When considering an IGBT overcurrent protection scheme, two important factors must be evaluated. The first factor is what type of overcurrent protection the system should provide and how the system can be shut down. The second factor is the control architecture. Control architecture significantly influences the method and implementation of the overcurrent protection. Protection of IGBT devices is normally implemented in the hardware circuit. However, the circuit implementation and the type of overcurrent-sensing device vary depending on which overcurrent condition is being addressed.

Table 3. Overcurrent Conditions and Possible Causes

OVERCURRENT CONDITION	POTENTIAL CAUSE
Ground fault	Motor insulation breakdown to ground
Line-to-line short	Miswiring, motor leads short, motor phase-to-phase insulation breakdown
Shoot through	False IGBT turn-on

The overcurrent protection can be implemented using two comparators. The two thresholds are required, one for positive cycle and one for negative cycle. These thresholds must be derived based on the voltage across the burden resistor. The total propagation delay of the shutdown is also important. The current sensor itself has some delay, which includes delay for the sensing mechanism and its own response time. Therefore, no matter how the protection circuit is implemented, this delay time must be added to the circuit delay to meet the IGBT short-circuit duration time.

The following list lays out the four basic criteria for choosing the comparator:

1. Propagation delay: Typically, industrial motor drives require an overcurrent protection shutdown to be triggered within 1 µs, which means that the comparator must have a propagation delay of 500 ns or less.
2. Supply voltage: The current output Hall effect sensor LAH 25-NP operates on the dual supply, which means the output voltage (across the burden resistor) also varies in positive as well as negative range. The supply voltage requires a comparator with the same dual supply as the sensor, or ±12 V.
3. Output type: The output of the comparator is a digital signal that indicates the overcurrent protection. The output is typically connected to a general purpose input/output (GPIO) pin or the ADC of a microcontroller. Therefore, the maximum output voltage can go up to 3.3 V. If the comparator output is an open-drain or open-collector type, then it can be connected to a 3.3-V supply using pullup resistor.
4. Size and cost: Having a single package with two comparators is ideal. The cost of the comparator should be as low as possible.

Based on the different requirements, this design uses the TLV1702 as a comparator for the overcurrent protection mechanism. The TLV1702 is a dual supply (±1.1- to ±18-V) comparator with two channels. The open collector output offers the advantage of allowing the output to be pulled to any voltage rail up to 36 V regardless of the supply voltage. The propagation delay for the TLV1702 device is 560 ns and it is available in a VSSOP-8 package. The TLV1702 is specified for operation across the expanded industrial range of −40°C to +125°C.

5 System Design

5.1 Sensor Circuit Design

The LAH 25-NP sensor can be configured to measure a nominal primary current of 8 A, 12 A, and 25 A using the datasheet. Figure 7 (taken from the datasheet) shows the different PCB connections when using the sensor for different current ratings.

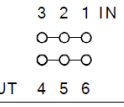
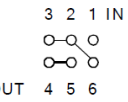
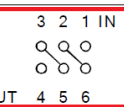
Number of primary turns	Primary current nominal I_{PN} [A]	Primary current maximum I_P [A]	Nominal output current I_{SN} [mA]	Turns ratio K_N	Primary resistance R_P [mΩ]	Primary insertion inductance L_P [µH]	Recommended PCB connections
1	25	55	25	1 : 1000	0.18	0.012	
2	12	27	24	2 : 1000	0.81	0.054	
3	8	18	24	3 : 1000	1.62	0.110	

Figure 7. Recommended PCB Connection for LAH 25-NP

Figure 8 shows the schematic connections for the LAH 25-NP, based on Figure 7.

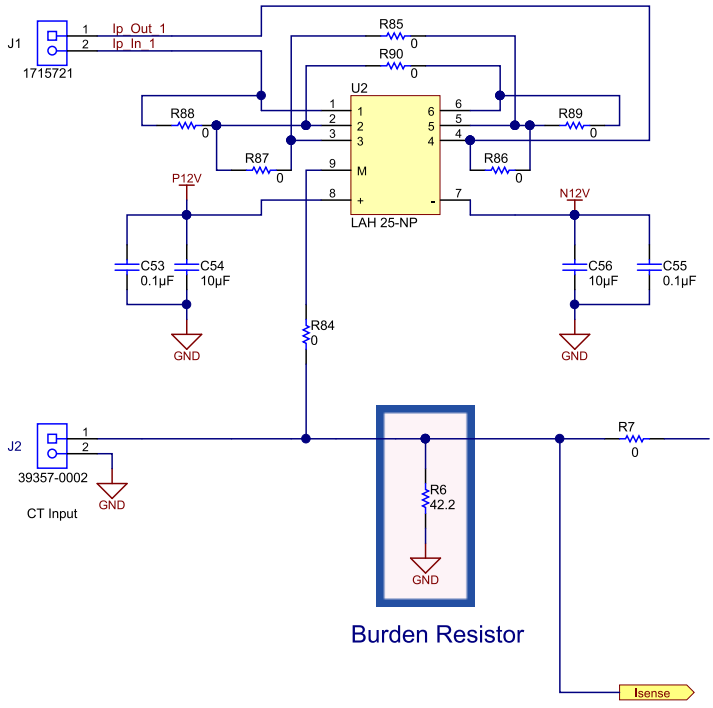


Figure 8. Schematic Section Showing Connections for LAH 25-NP

Table 4 shows the details regarding which resistors to mount to achieve a particular nominal input current setting.

Table 4. Resistor Straps on Board

NOMINAL PRIMARY CURRENT (IN A)	POPULATE THESE RESISTORS ONLY
8	R85, R90
12	R86, R90
25	R86, R87, R88, R89

5.2 Generation of ±12 V to Power LAH 25-NP and TLV1702

For applications that require positive and negative high-performance rails, TI recommends to use the TPS7A40xx and TPS7A30xx families of linear regulators. Figure 9 shows the generation of ±12 V from a ±15-V input supply.

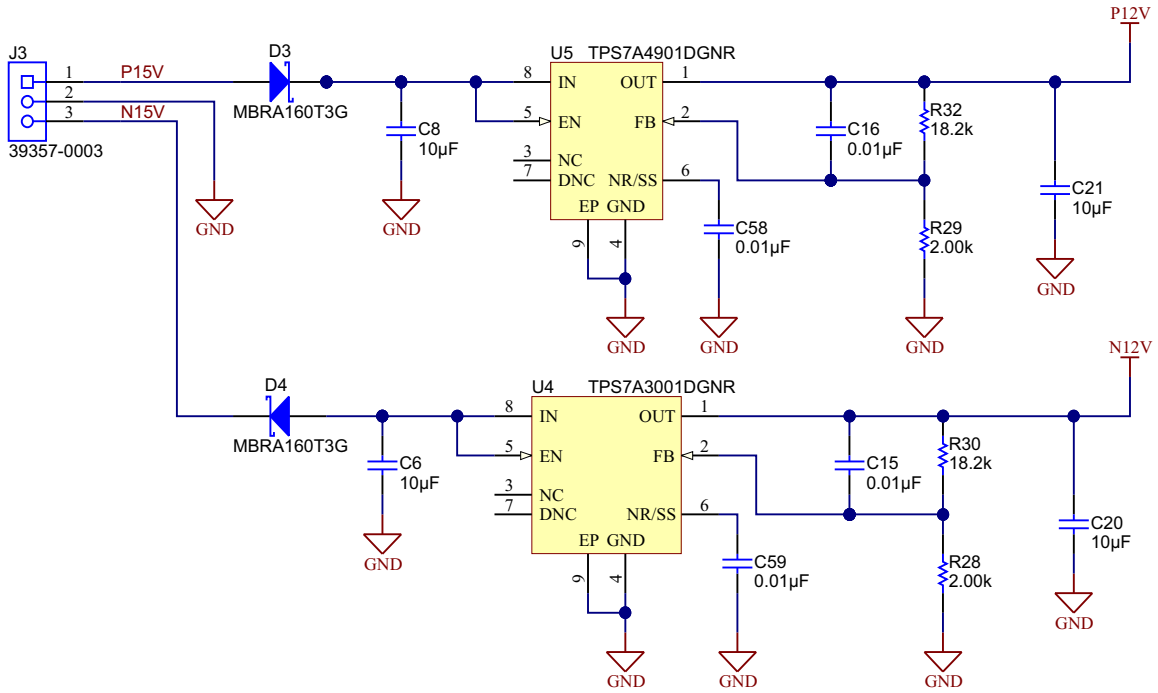


Figure 9. Schematic Generation of ±12 V From ±15 V

The TPS7A4901 is a high-voltage, positive, high-accuracy linear regulator designed to power operational amplifiers and other high-performance analog circuitry. In this design, the TPS7A4901 device is used to generate 12 V from a 15-V rail. Two 10-µF caps are connected: C8 on the input and C21 on the output of the TPS7A4901. The TPS7A4901 regulator requires a capacitor ≥ 2.2 µF from the output pin connected to ground to ensure stability. The TPS7A3001 is a high-voltage, positive, high-accuracy linear regulator designed to power operational amplifiers and other high-performance analog circuitry. In this design, the TPS7A3001 is used to generate −12 V from a −15-V rail. Two 10-µF caps are connected: C6 on the input and C20 on the output of the TPS7A3001 device. The TPS7A3001 regulator requires a capacitor ≥ 2.2 µF from the output pin connected to ground to ensure stability.

For both the TPS7A4901 and TPS7A3001 devices, the NR/SS pin bypasses noise generated by the internal bandgap. Capacitors C58 and C59 (connected to the NR/SS pin) allow the RMS noise to be reduced to very low levels and also control the soft-start function. The soft-start time is calculated as given in Equation 3:

$$t_{ss}(ms) = 1.4 \times C_{NR/SS}(nF) \quad (3)$$

So for both devices, with a capacitor value of 0.01 µF, the soft-start time is 14 ns.

The outputs for the TPS7A4901 and TPS7A3001 devices are set to 12 V and −12 V respectively using Equation 4.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB(nom)}} - 1 \right), \text{ where } \frac{V_{FB(nom)}}{R_2} > 5\ \mu A \tag{4}$$

For a 12-V output, the feedback resistors are R32 = 18.2 kΩ and R29 = 2 kΩ. For a −12-V output, the feedback resistors are R30 = 18.2 kΩ and R28 = 2 kΩ.

5.3 Generation of PVMID

The TPS62150 is a synchronous step-down DC-DC converter. A high-switching frequency of 2.5 MHz (typically) allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by utilizing the DCS-Control™ topology. If efficiency is the key parameter, more so than solution size, set the switching frequency to half (1.25 MHz typically) by pulling f_{sw} to high. It is mandatory to start with f_{sw} = low to limit the inrush current, which can be done by connecting to V_{OUT} or PG. To obtain low ripple and full output current at the lower switching frequency, TI recommends using an inductor of at least 2.2 µH. The switching frequency can be changed during operation, if required. A pulldown resistor of about 400 kΩ is internally connected to the pin.

The output voltage of the TPS62150 device is adjustable. It can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from V_{OUT} to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 5. TI recommends choosing resistor values that allow a current of at least 2 uA, meaning that the value of R2 must not exceed 400 kΩ. Lower resistor values are recommended to obtain the highest level of accuracy and the most robust design.

$$R_{13} = R_5 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{5}$$

where

- V_{OUT} = 6 V
- V_{REF} = 800 mV
- R13 = 1 MΩ
- R5 = 154 kΩ (see Figure 10)

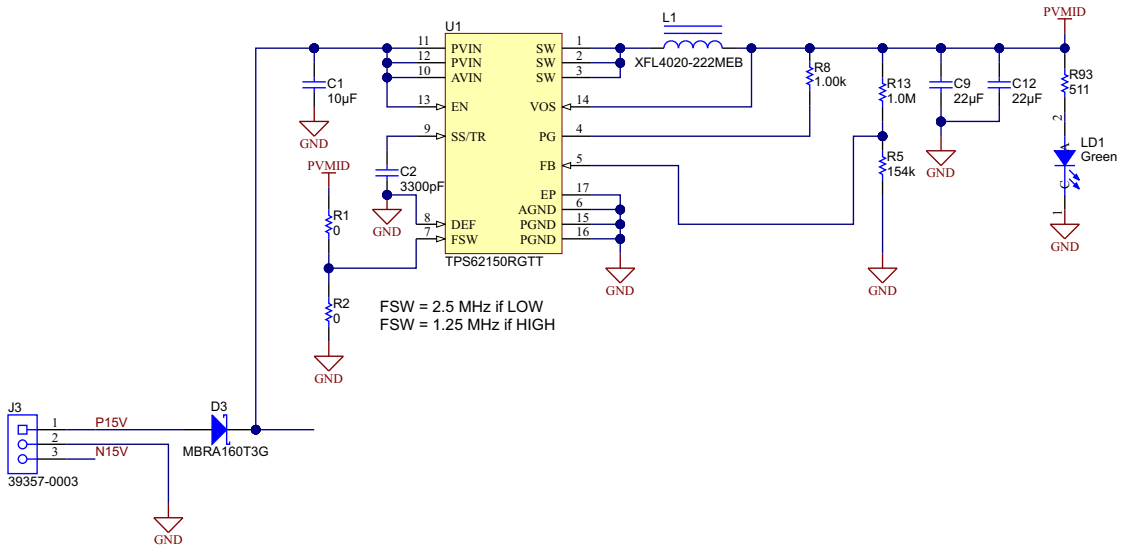


Figure 10. Generation of PVMID Using TPS62150

For most applications, 10 µF is sufficient and is the recommended value for the input capacitor, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply.

A capacitance connected between the SS/TR pin and AGND allows a user-programmable start-up slope of the output voltage. A constant current source supports 2.5 µA to charge the external capacitance. Equation 6 shows the capacitor required for a given soft-start ramp time for the output voltage:

$$C_{SS} = t_{SS} \frac{2.5\ \mu A}{1.25\ v} [F] \quad (6)$$

where

- C_{SS} is the capacitance (F) required at the SS/TR pin
- t_{SS} is the desired soft-start ramp time (seconds)

With CSS = 3300 pF, the soft-start time is 1.65 ms.

5.4 Generation of 5 V

From PVMID (which is equal to 6 V), the user must generate 5 V to power the op-amps and voltage reference ICs. The LP2992 device is used to generate 5 V from PVMID, as Figure 11 shows.

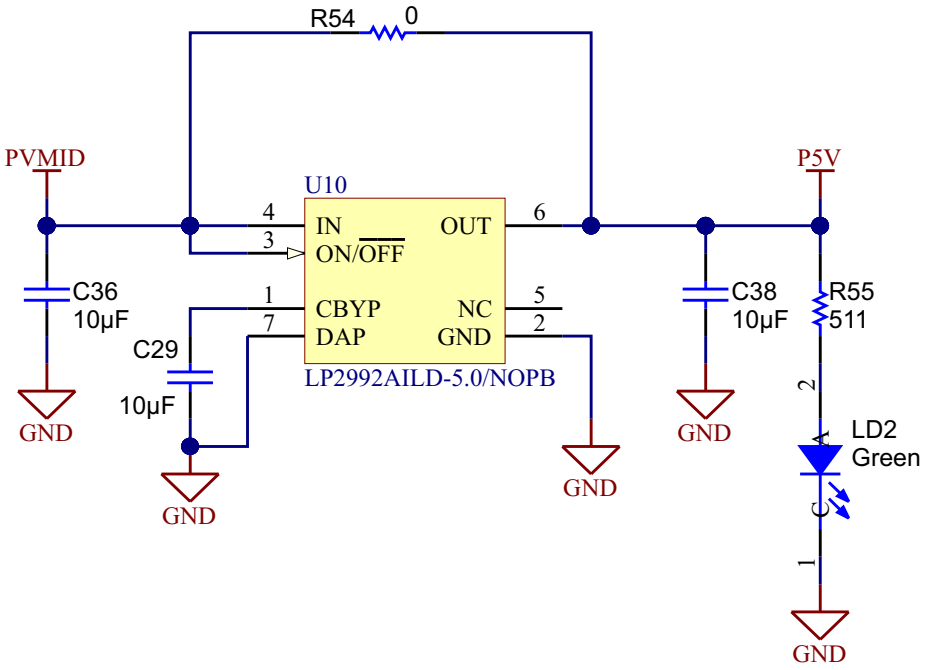


Figure 11. Generation of 5 V Using LP2992

NOTE: PVMID is currently set to 6 V and R54 is DNP. When LP2992 is not used, mount R54 and set PVMID = 5 V.

5.5 Voltage Reference Circuit Design

Using external ADCs

While using external ADCs (which are powered using a 5-V single supply), the reference voltage must be set to 2.5 V.

Using Internal ADCs (of a Delfino controller)

While using differential mode, the reference pin must be powered from a 2.5-V reference (a Delfino controller converts 2.5 V into a 1.25-V reference, internally).

To fulfill these conditions, use a single reference device. Figure 12 shows the schematic section for REF2025, which provides two reference voltages: 1.25 V and 2.5 V. The input to REF2025 is powered from 5 V. Both the reference outputs (2.5 V and 1.25 V) are provided with resistor-capacitor (RC) filters for any noise filtering.

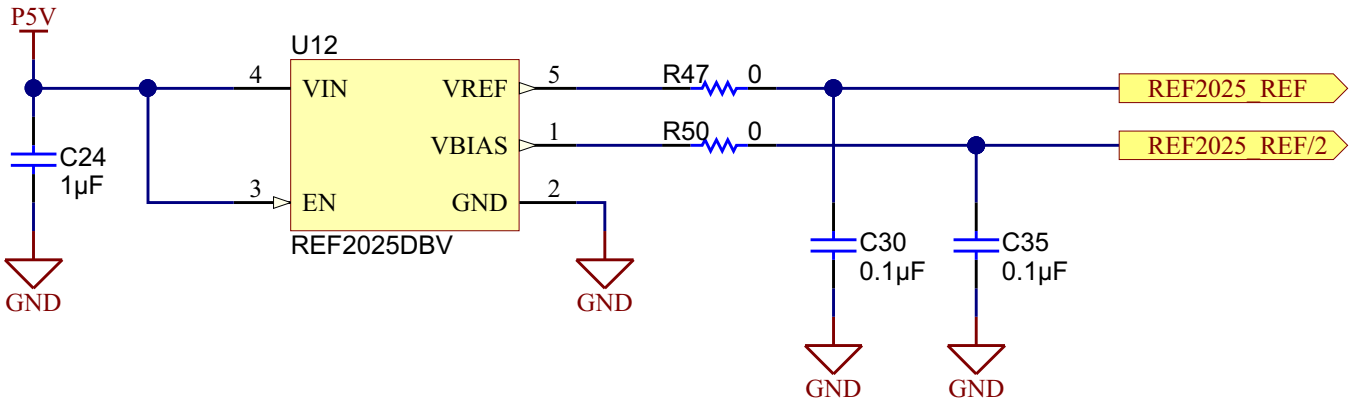


Figure 12. REF2025 Circuit to Provide 1.25 V and 2.5 V as Reference

5.6 Design of Level-Shifting Unipolar Amplifier Stage

Be sure to observe the following important bullet points when designing the level-shifting op-amp circuit. Figure 13 shows the implementation of the same.

1. Single supply operation: The OPA322 device is powered from 5 V. Place one bypass capacitor with a value of 0.1 µF very close to the AVDD pin of the OPA322 device.
2. Unity gain buffer: The OPA322 op-amp is used to buffer the input signal as well as level-shift it to a particular voltage.
3. Level shifting: The non-inverting pin of the op-amp is supplied with 2.5 V (coming from the REF2025 reference) fin case it must interface with an external ADC. However, when using the internal differential ADC of a Delfino F2837x controller, the common-mode voltage must be 1.25 V. When using the Delfino™ F2837x controller, the external voltage on the non-inverting pin of the op-amp is supplied through 1.25 V (coming from the REF2025 REF/2 pin).
4. Selection of components: The 100-pF caps in the feedback help to reduce the overall noise of the system. An important thing to note is that the resistors also have their internal noise. The level of resistor noise depends on the value of the resistor. Selecting the input and feedback resistor values in some kΩ (preferably < 5 kΩ) works well to reduce the effect of noise from resistors.
5. Input protection: The Hall sensor has a supply voltage of ±12 V. In the case of any fault or short circuit condition, diodes D6 and D5 are used to clamp the input of the op-amp to 5V and GND, which protects the op-amp. The input coming from the sensor is also filtered using an RC filter (R15 and C4).

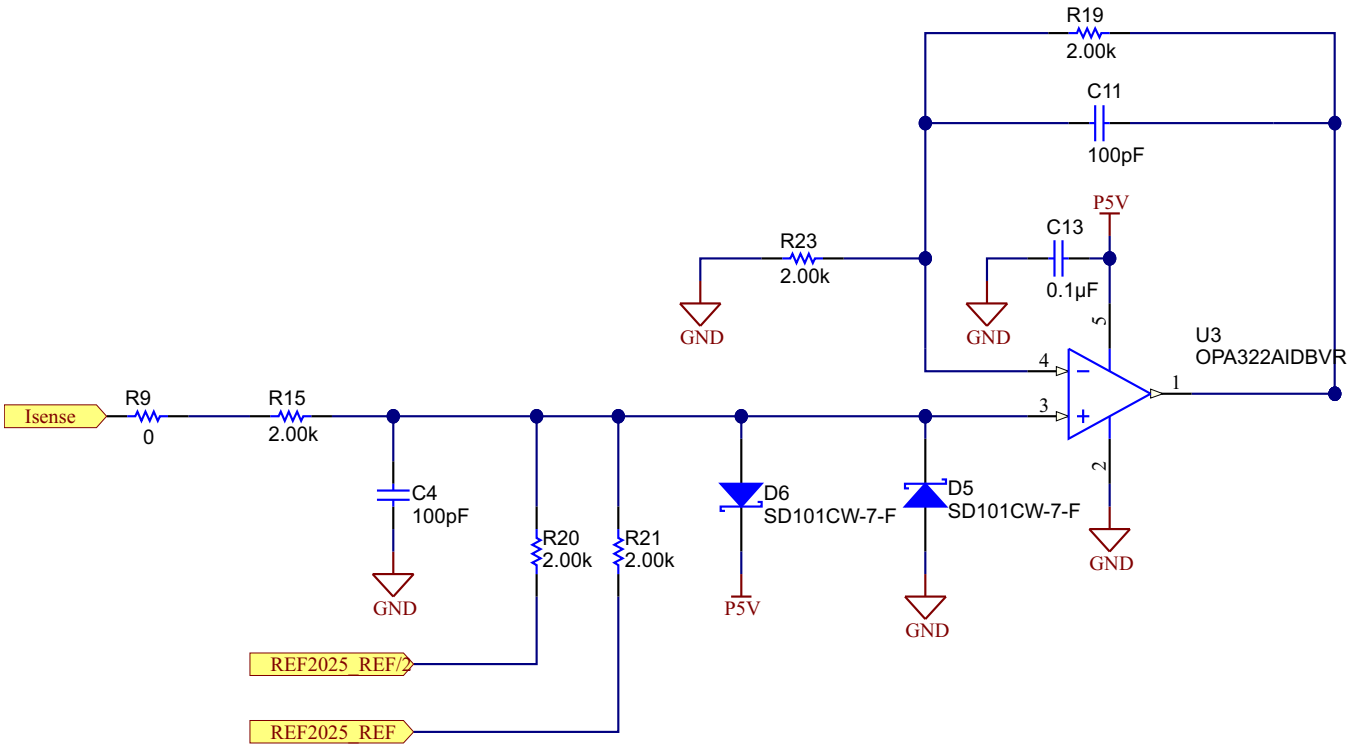


Figure 13. OPA322 as Level Shifter

The output of the OPA322 op-amp is connected to the non-inverting input of the THS4531A device.

5.7 Design of THS4531A and MFB Low-Pass Filter Stage

Be sure to observe the following important bullet points when designing the differential signal conditioning circuit. Figure 16 shows the implementation of the THS4531A device.

1. Single supply operation: The THS4531A device is powered from 5 V. Two bypass capacitors are placed very close to the AVDD pin of the THS4531A device, one 0.1-µF capacitor (package = 0603) and one 0.01-µF capacitor (package = 0402).
2. Unity gain buffer: The THS4531A device is used to buffer the input signal and the gain is set to unity.
3. Output common-mode setting: The output common-mode voltage is set by the voltage provided on the VOCM pin of the THS4531A device. The VOCM pin is supplied with 2.5 V (coming from the REF2025 reference) for situations where it must interface with an external ADC. However, when using the internal differential ADC of a Delfino™ F2837x controller, the common-mode voltage must be 1.25 V. When using the Delfino F2837x controller, the common-mode voltage is supplied through 1.25 V (coming from REF2025 REF/2).
4. Multiple-feedback low-pass filter: The THS4531A device also uses multiple-feedback (MFB) topology for filtering. The cut-off frequency of the filter is set to 165 KHz, which is ten times the maximum switching frequency of an IGBT inverter of an industrial motor drive. The filter components are selected according to Equation 7.

$$f = \frac{1}{2\pi\sqrt{C26 \times R38 \times C27 \times R37}} \quad (7)$$

where

- C26 = 200 pF
- R38 = 255 Ω
- C27 = 9.1 nF
- R37 = 2 kΩ
- The cut-off frequency is 165.196 KHz

5. Selection of components: An important thing to note is that the resistors also have their internal noise. The level of resistor noise depends on the value of the resistor. Select the input and feedback resistor values in some kΩ (preferably < 5 kΩ) to reduce the effect of noise from the resistors. The resistors on both the inverting and non-inverting inputs of the differential amplifier must also match tightly so as not to create any current unbalance. The components used in this design have a 0.1% tolerance.
6. Stability check for THS4531A: When embedding an integrator circuit to drive a capacitive load that is not outside the loop R value, the user must look at the kind of curves that Figure 14 and Figure 15 show and pick off the resistor value for the capacitive load. From these graphs, the R46 and R47 must be about 25 Ω inside the loop for stability.

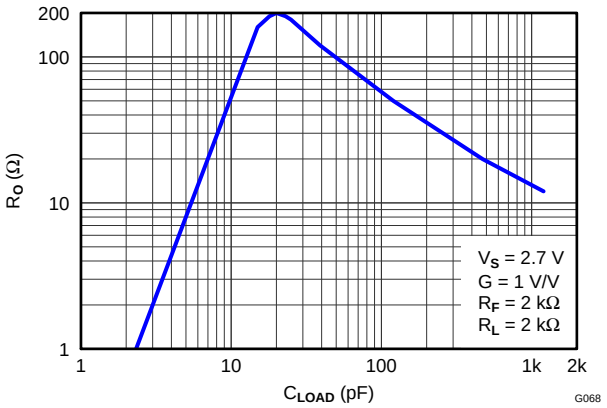


Figure 14. Recommended Series Output Resister Versus Capacitive Load for Flat Frequency Response

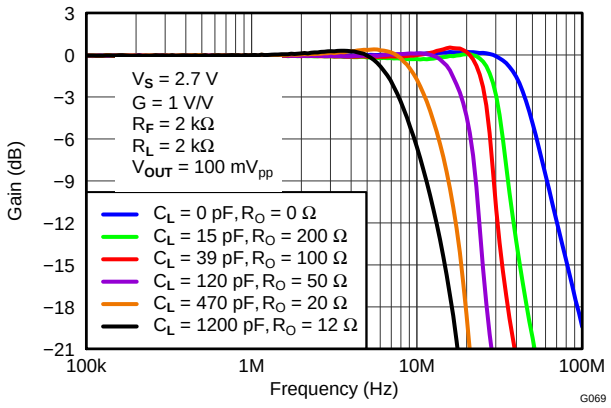


Figure 15. Frequency Response for Various R_O and C_L Values

Figure 16 shows that the output of the differential signal circuit (THS4531A) is connected to SMA jack J6 and J7 in addition to the input of the Delfino™ F2837x control card from TI.

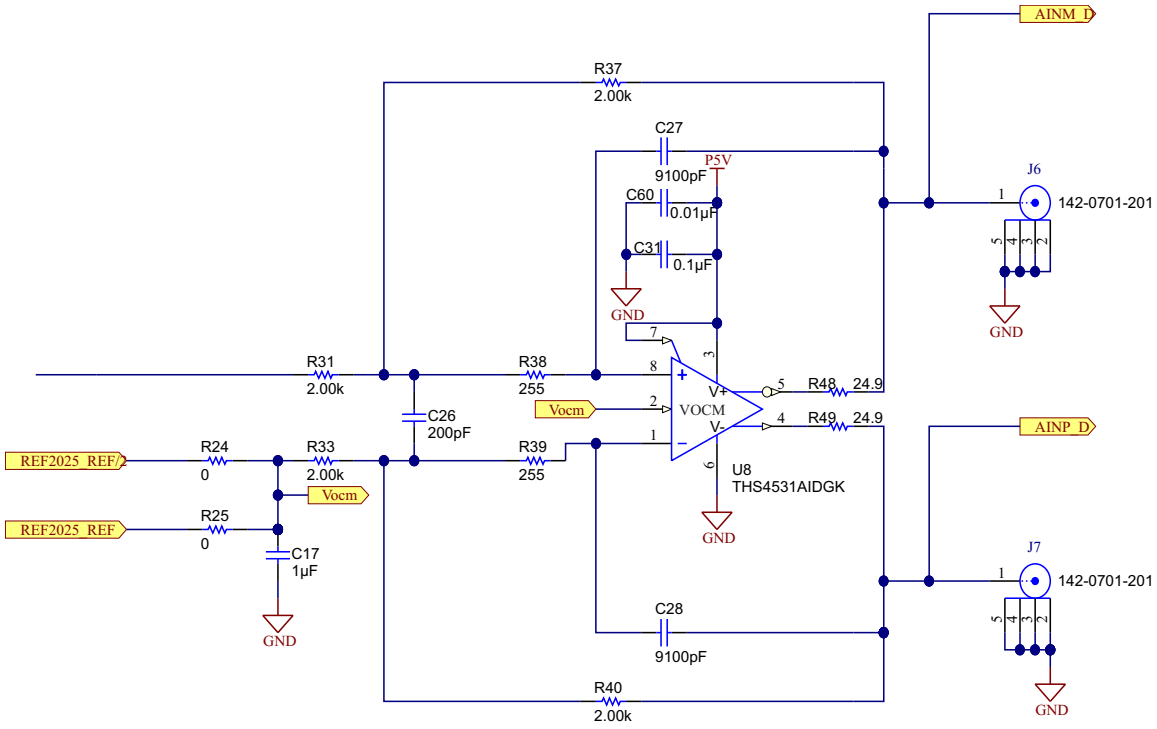


Figure 16. OPA2192 Interface Between Sensor and ADC

Figure 17 shows the simulation from the TINA-TI™ software for the schematic in Figure 16.

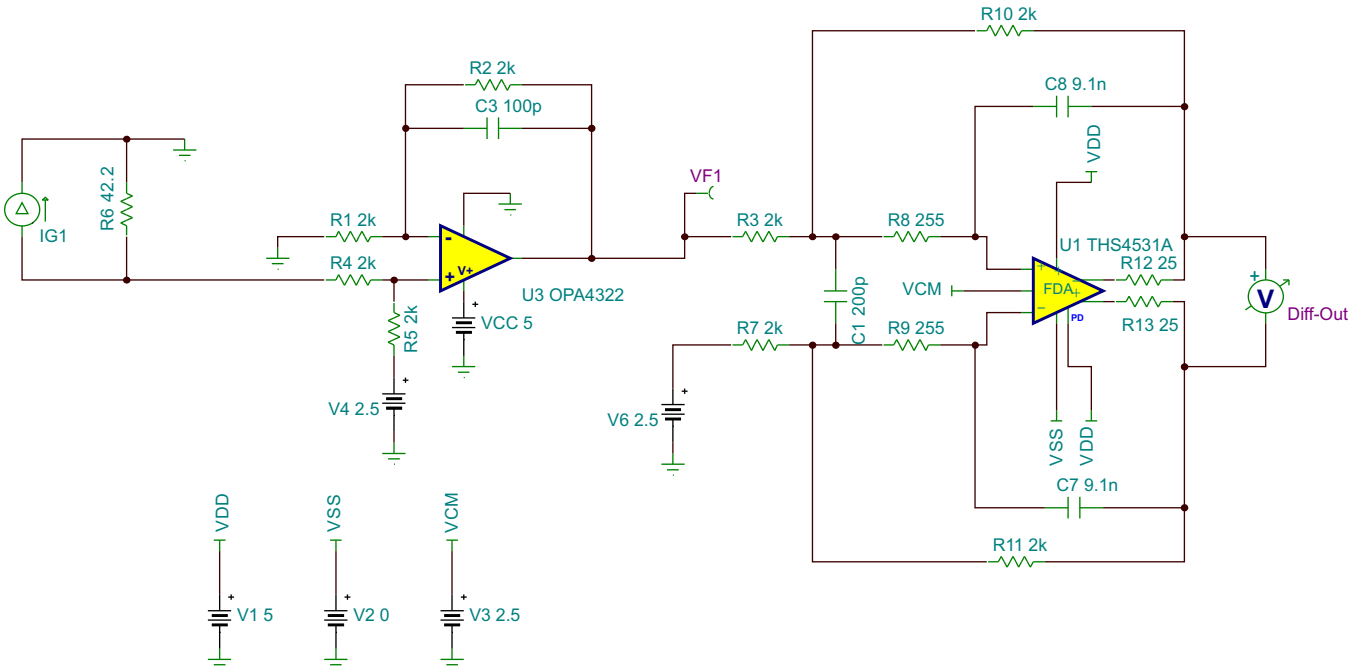


Figure 17. TINA Simulation for Differential Signal Conditioning Circuit

Figure 18 shows the simulated waveforms and Figure 19 shows the stability analysis for Figure 17.

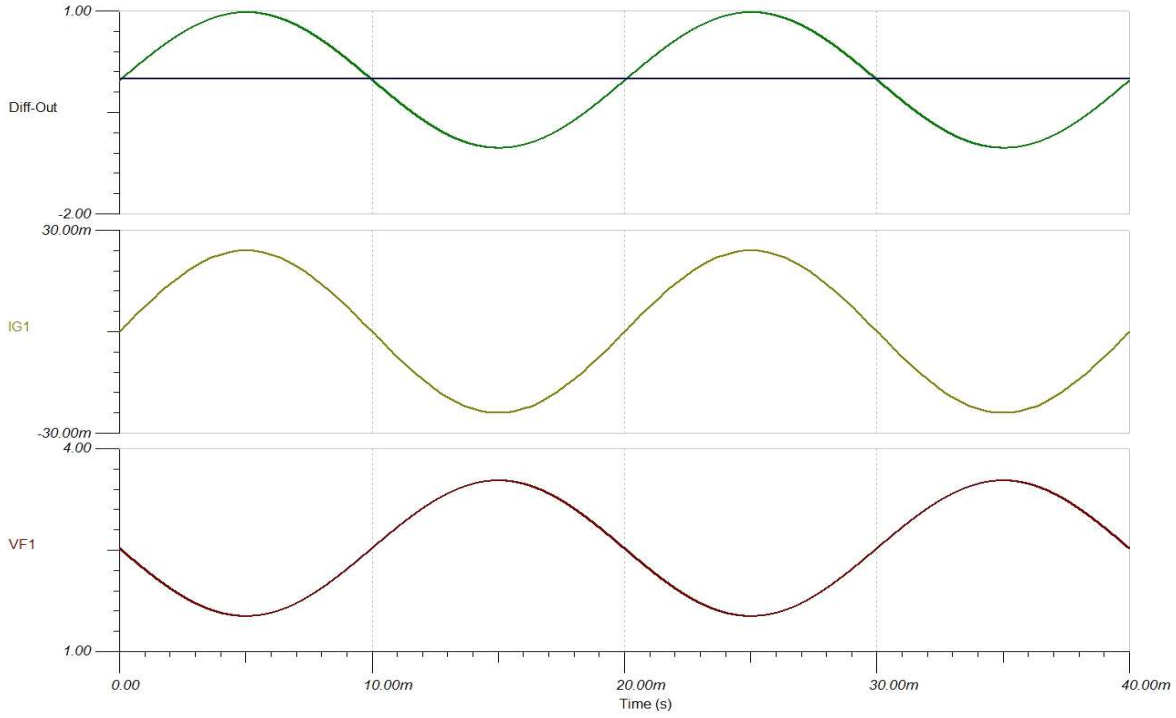


Figure 18. Waveforms for TINA Simulation

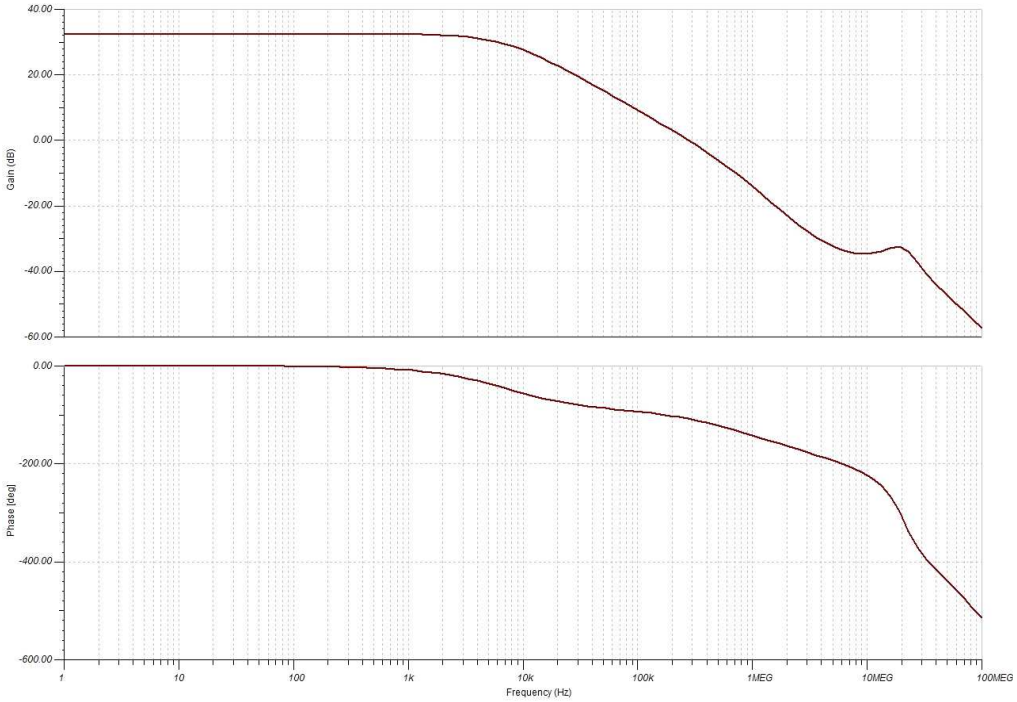


Figure 19. Bode Plot for TINA Simulation

5.8 Design of Overcurrent Detection Circuit

In industrial motor drives, using the sensor until 200% of its rating is a very common practice. If the current goes beyond 200%, the protection mechanism must be enabled. In this design, the thresholds are calculated as below:

Nominal current rating (In) = 8 A

Corresponding nominal output current = 24 mA (from Figure 5)

Maximum current rating = 18 A (which is 225% of the nominal primary current)

Corresponding nominal output current = 54 mA (from Figure 5)

Corresponding output voltage = 2.25 V (with burden resistor = 42.2 Ω)

The overcurrent protection is implemented as Figure 20 shows. The comparators used in the protection circuits are open-drain outputs. The pull-up resistors are connected to 3.3 V (which is typically equal to the digital supply of the MCU or any other motor controller) so that the high and low levels of the comparator outputs are within the sensing range of the controller.

The resistor divider to generate the thresholds is calculated for VTH (positive) = 2.25 V and VTH (negative) = −2.25 V.

Equation 8 and Equation 9 show the calculated value of VTH (positive) and VTH (negative).

$$\text{VTH}\left(\text{pos}\right)=\frac{\left\{12-\left(-12\right)\right\}\times\left(43.2\ \text{k}+20\ \text{k}\right)}{43.2\ \text{k}+20\ \text{k}+43.2\ \text{k}}=14.2556\ \text{V}=+2.2556\ \text{V for}+12\ \text{V} \tag{8}$$

$$\text{VTH}\left(\text{neg}\right)=\frac{\left\{12-\left(-12\right)\right\}\times 43.2\ \text{k}}{43.2\ \text{k}+20\ \text{k}+43.2\ \text{k}}=9.744\ \text{V}=-2.2556\ \text{V for}-12\ \text{V} \tag{9}$$

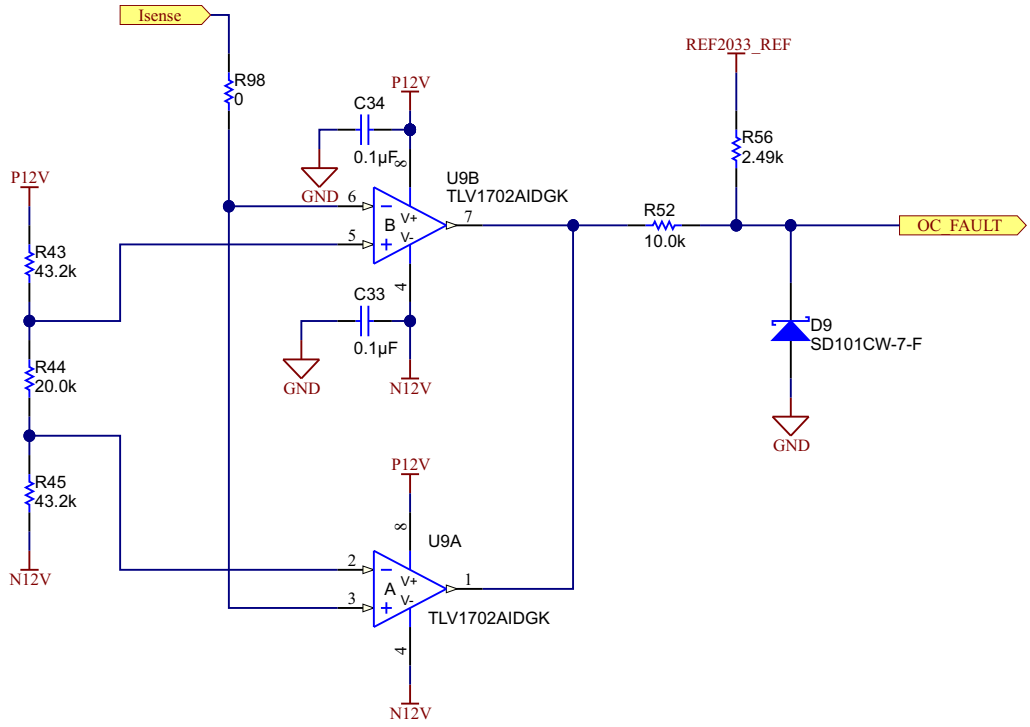


Figure 20. Overcurrent Protection Using TLV1702

5.9 Connection to TI Delfino™ F2837x Control Card

The Texas Instruments Delfino™ F28377D Control Card (TMDSCNCD28377D) provides a great way to learn and experiment with the F2837x device family within the Texas Instrument's C2000™ family of microcontrollers (MCUs). The purpose of this 180-pin control card is to provide a well-filtered, robust design capable of working in most industrial environments.

F28377D control card features:

- Delfino F28377D MCU – This high performance C2000 microcontroller is located on the control card.
- 180-pin HSEC8 edge card interface – This device is compatible with all C2000 180-pin control card application kits and control cards. Compatibility with 100-pin control cards can be accomplished using the TMDSADAP180TO100 adapter card (sold separately).
- Built-in isolated JTAG emulation – A Texas Instruments XDS100v2 emulator provides a convenient interface to the Texas Instruments Code Composer Studio™ (CCS) software without additional hardware. Flipping a switch allows the use of an external JTAG emulator.
- Connectivity – The control card contains connectors that allow the user to experiment with a USB, microSD card, and isolated universal asynchronous receiver/transmitter (UART) or SCI with the F2837x MCU.
- Key signal breakout – Most GPIOs, ADCs, and other key signals are routed to hard gold connector fingers.
- Robust power supply filtering – A single 5-V input supply powers a 3.3-V LDO on the card. All MCU inputs are then decoupled using LC filters near the device.
- ADC clamping – ADC inputs are clamped by protection diodes.

Figure 21 shows an image of the control card.

Figure 21. Image of Delfino™ F2837x Control Card from TI

Pin-mapping for TI Delfino™ F2837x control card:

Figure 22 shows the pin-mapping for the 180-pin connector available on the Delfino F2837x control card. Table 5 shows how the signals are routed.

Table 5. Pin Mapping Details

PIN NUMBER ON CONTROL CARD	PIN FUNCTIONALITY	MAPPING ON TIDA-00368 BOARD (J10 AND J11)
7, 10, 19, 22, 35, 38, 43, 46, 47, 65, 83, 97, 111, 135, 157, 179	GND	GND
11	ADC-A1, DAC	REF2025_REF/2
21	ADC-A4, COMP+	AINP_D
23	ADC-A5	AINM_D
45	All VREFHIs	REF2025_REF
48, 84, 98, 112, 158, 180	AVDD	AVDD (PVMID)

Date:				cCARD Pinout:		F28377D (180pin)				HSEC Pinout:
7-May-2014										2.10
		HSEC pin	MCU pin	HSEC function		HSEC function	MCU pin	HSEC pin		
		1	GPIO-71 **	JTAG-EMU1		JTAG-EMU0	GPIO-70 **	2		
		3	TMS	JTAG-TMS		JTAG-TRSTn	TRSTn	4		
		5	TCK	JTAG-TCK		JTAG-TDO	TDO	6		
		7		GND		JTAG-TDI	TDI	8		
		9	ADC-A0, DAC	ADC1 (and/or DACA)		GND		10		
		11	ADC-A1, DAC	ADC1 (and/or DACB)		ADC2	ADC-B0	12		
		13		Rsvd		ADC2	ADC-B1	14		
		15	ADC-A2, COMP+	ADC1 (and/or CMPIN+)		Rsvd		16		
		17	ADC-A3	ADC1		ADC2	ADC-B2, COMP+	18		
		19		GND		ADC2	ADC-B3	20		
		21	ADC-A4, COMP+	ADC1 (and/or CMPIN+)		GND		22		
		23	ADC-A5	ADC1		ADC2	ADC-B4, COMP+	24		
		25	ADCIN14, COMP+	ADC (and/or CMPIN+)		ADC2	ADC-B5	26		
		27	ADCIN15	ADC		ADC	ADC-D0, COMP+	28		
		29		Rsvd		ADC	ADC-D1	30		
		31	ADC-C2, COMP+	ADC		Rsvd		32		
		33	ADC-C3	ADC		ADC	ADC-D2, COMP+	34		
		35		GND		ADC	ADC-D3	36		
		37	ADC-C4	ADC		GND		38		
		39	ADC-C5	ADC		ADC	ADC-D4	40		
		41		Rsv		ADC	ADC-D5	42		
		43		A-GND (VREFLO on certain MCU)		Rsv		44		
		45	All VREFHIs *	Rsv (VREFHI on certain MCU)		GND		46		
		47		GND		5V0		48		
		49	GPIO-00	PWM1A		PWM3A	GPIO-04	50		
		51	GPIO-01	PWM1B		PWM3B	GPIO-05	52		
		53	GPIO-02	PWM2A		PWM4A	GPIO-06	54		
		55	GPIO-03	PWM2B		PWM4B	GPIO-07	56		
		57	GPIO-08	PWM5A		PWM7A or TZ1	GPIO-12	58		
		59	GPIO-09	PWM5B		PWM7B or TZ2	GPIO-13	60		
		61	GPIO-10	PWM6A		PWM8A or TZ3	GPIO-14	62		
		63	GPIO-11	PWM6B		PWM8B or TZ1/4	GPIO-15	64		
		65		GND		12V0?		66		
		67	GPIO-16	SPISIMOA		QEP1A (McBSP-MDXA)	GPIO-20	68		
		69	GPIO-17	SPISOMIA		QEP1B (McBSP-MDRA)	GPIO-21	70		
		71	GPIO-18	SPICLKA		QEP1S (McBSP-MFSXA)	GPIO-22	72		
		73	GPIO-19	SPISTEA		QEP1I (McBSP-MCLKXA)	GPIO-23	74		
		75	GPIO-24	ECAP1 or SPISIMOB		SCIRXA	GPIO-28	76		
		77	GPIO-25	ECAP2 or SPISOMIB		SCITXA	GPIO-29	78		
		79	GPIO-26	ECAP3 or SPICLKB		CANRXA	GPIO-30	80		
		81	GPIO-27	ECAP4 or SPISTEB		CANTXA	GPIO-31	82		
		83		GND		5V0		84		
		85	GPIO-32	I2CSDAA		GPIO	GPIO-34	86		
		87	GPIO-33	I2CSCLA		GPIO	GPIO-39	88		
		89	GPIO-40	GPIO		GPIO	GPIO-44	90		
		91	GPIO-41	GPIO		GPIO	GPIO-45	92		
		93	GPIO-42 ***	GPIO		GPIO	GPIO-46 ***	94		
		95	GPIO-43 ***	GPIO		GPIO	GPIO-47 ***	96		
		97		GND		5V0		98		
		99	GPIO-48	GPIO		QEP2A or GPIO	GPIO-54	100		
		101	GPIO-49	GPIO		QEP2B or GPIO	GPIO-55	102		
		103	GPIO-50	GPIO		QEP2S or GPIO	GPIO-56	104		
		105	GPIO-51	GPIO		QEP2I or GPIO	GPIO-57	106		
		107	GPIO-52	GPIO		GPIO (McBSP-MCLKRA)	GPIO-58	108		
		109	GPIO-53	GPIO		GPIO (McBSP-MFSRA)	GPIO-59	110		
		111		GND		5V0		112		
		113		Rsv		Rsv		114		
		115		Rsv		Rsv		116		
		117		Rsv		Rsv		118		
		119		Rsv		Device Reset (Active low)	XRSn	120		
		121	GPIO-35	GPIO		GPIO	GPIO-36	122		
		123	GPIO-37	GPIO		GPIO	GPIO-38	124		
		125	GPIO-60	GPIO		GPIO	GPIO-61	126		
		127	GPIO-62	GPIO		GPIO	GPIO-63	128		
		129	GPIO-64	GPIO		GPIO	GPIO-65	130		
		131	GPIO-66	GPIO		GPIO	GPIO-67	132		
		133	GPIO-68	GPIO		GPIO	GPIO-69	134		
		135		GND		12V0?		136		
		137	GPIO-70	GPIO		GPIO	GPIO-71	138		
		139	GPIO-72	GPIO		GPIO	GPIO-73	140		
		141	GPIO-74	GPIO		GPIO	GPIO-75	142		
		143	GPIO-76	GPIO		GPIO	GPIO-77	144		
		145	GPIO-78	GPIO		GPIO	GPIO-79	146		
		147	GPIO-80	GPIO		GPIO	GPIO-81	148		
		149	GPIO-82	GPIO		GPIO	GPIO-83	150		
		151	GPIO-84	GPIO		GPIO	GPIO-85	152		
		153	GPIO-86	GPIO		GPIO	GPIO-87	154		
		155	GPIO-88	GPIO		GPIO	GPIO-89	156		
		157		GND		5V0		158		
		159	GPIO-90	GPIO		GPIO	GPIO-91	160		
		161	GPIO-92	GPIO		GPIO	GPIO-93	162		
		163	GPIO-94	GPIO		GPIO	GPIO-133	164		
		165	GPIO-120 ***	GPIO		GPIO	GPIO-121 ***	166		
		167	GPIO-161	GPIO		GPIO	GPIO-162	168		
		169	GPIO-163	GPIO		GPIO	GPIO-164	170		
		171		Rsv		Rsv		172		
		173		Rsv		Rsv		174		
		175		Rsv		Rsv		176		
		177		Rsv		12V0?		178		
		179		GND		5V0		180		

Analog (HSEC pin 9 – 45)

Analog (HSEC pin 12 – 48)

Digital (HSEC pin 49 – 119)

Digital (HSEC pin 50 – 120)

* Switches may be altered to connect VREFHIs to the HSEC connector

** 0ohm resistors can be removed in order to tie GPIO-70 and 71 to EMU0 and EMU1

*** Can be dedicated to on-card USB or brought through the connector via jumpers on the cCARD

Figure 22. Pin Mapping on Delfino F2837x Control Card (180-Pin Connector)

Figure 23 shows the schematic capture for the pin-mapping that Table 5 shows. Although, the control card has clamping diodes at each of the analog inputs, this design provides an option to mount external clamping diodes, as well.

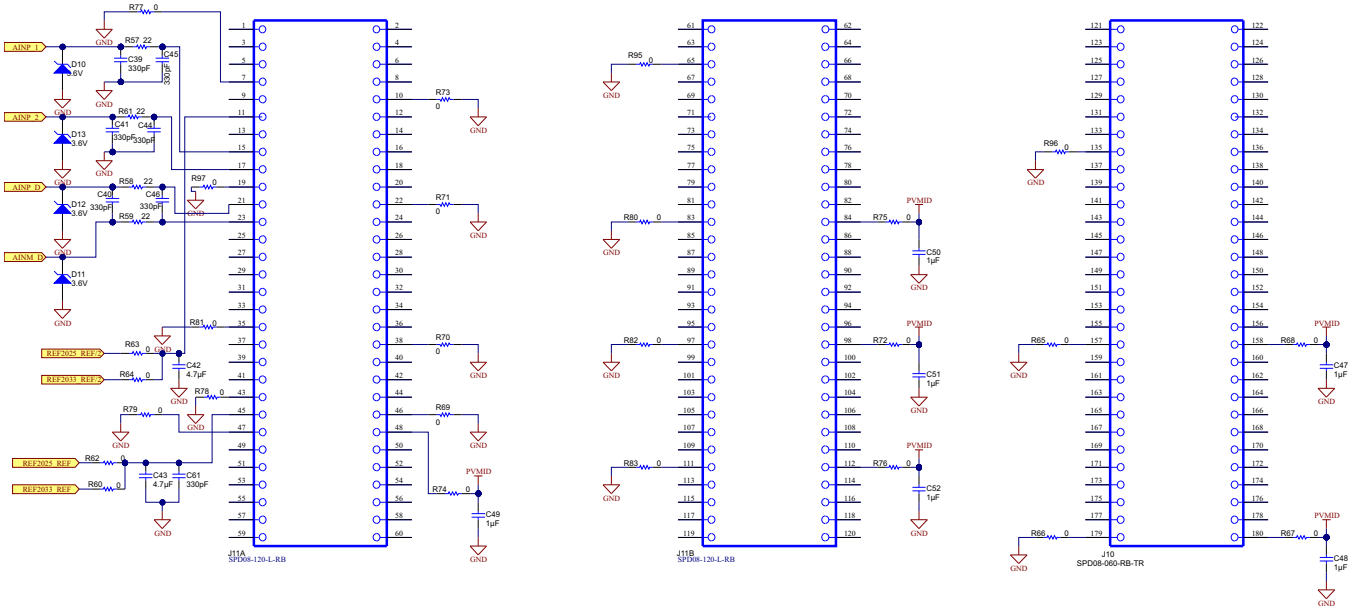


Figure 23. Schematic Capture for J10 and J11 (to Connect to 180-Pin Connector on Control Card)

NOTE: The control card can be powered through the onboard 6 V (that is, PVMID) or by using the external 5 V from a USB. When powering the control card with an external USB connection, TI recommends disconnecting the PVMID voltage by removing the corresponding resistors (see Figure 23).

The output of the differential signal conditioning circuit is connected to Channel A4 and Channel A5 of the internal ADC of the Delfino controller. As Figure 24 shows, the inputs are provided with RC filters for the purpose of anti-aliasing.

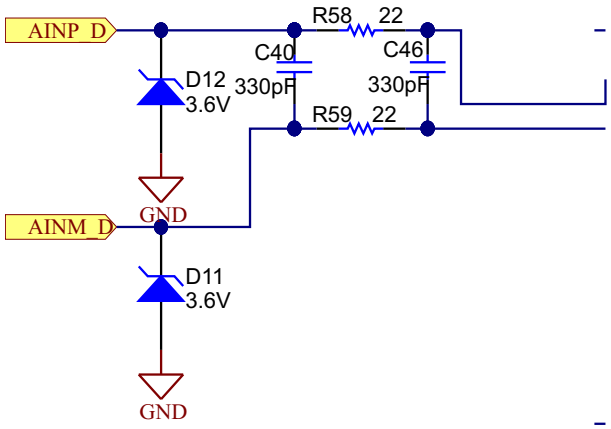


Figure 24. Filtering for ADC Inputs on Control Card

Figure 25 shows the reference, which connects to the VREFHI inputs on the 180-pin control card.

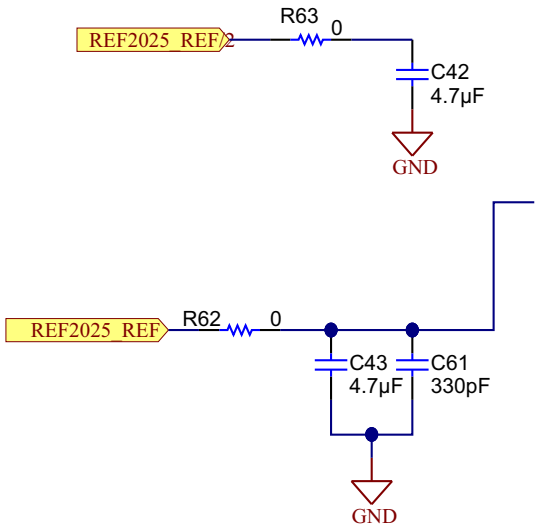


Figure 25. Reference and Common-Mode voltage

5.10 Connectors to Connect With External Motor Controller

As Figure 26 shows, the two connectors J12 and J4 are provided on the board with all of the signals (outputs of signal conditioning circuits, reference voltages, and so forth), which enables interfacing with an external motor controller. The overcurrent fault signal is available on connector J9.

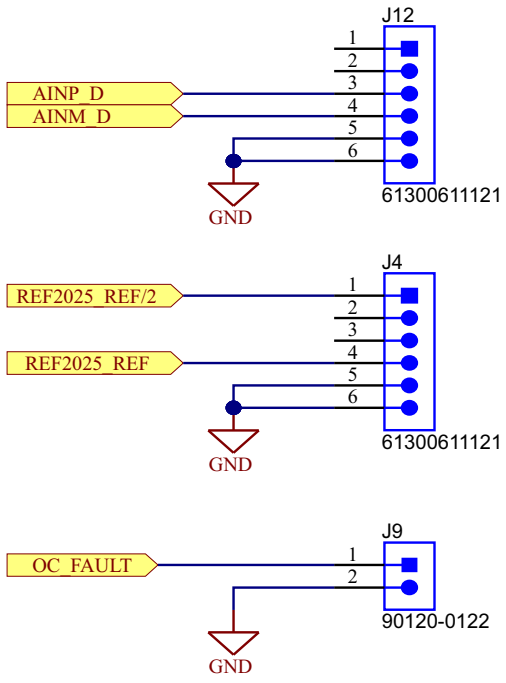


Figure 26. Connectors to Interface With External Motor Controller

6 Test Setup

Figure 27 shows a diagram of the setup used for AC and DC performance measurements in this reference design.

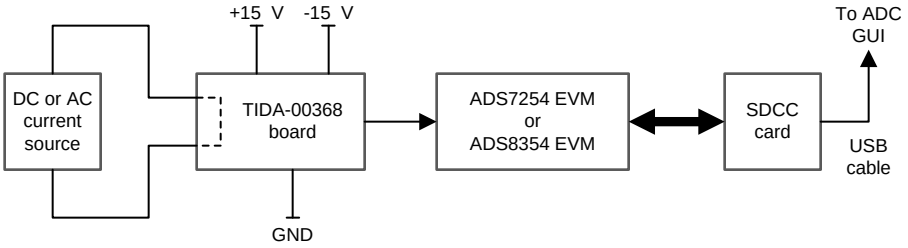


Figure 27. Test Setup for AC and DC Tests Using ADS7254 and ADS8354

7 Test Data

7.1 Power Supply and Reference Circuit Functionality Tests

The power supply circuit is tested for functionality and ripple measurement. Table 6 shows the tested voltages.

Table 6. Power Supply Rails

	RAIL	DESIGNED FOR (IN V)	MEASURED VALUE (IN V)
POWER SUPPLY	PVMID	6	6.0304
	P5V	5	4.9593
	P12V	12	11.9248
	N12V	–12	–11.8757
REFERENCES	REF2025_REF	2.5	2.5001
	REF2025_REF/2	1.25	1.2502

Figure 28 shows the output of TPS62150 set at 6 V.

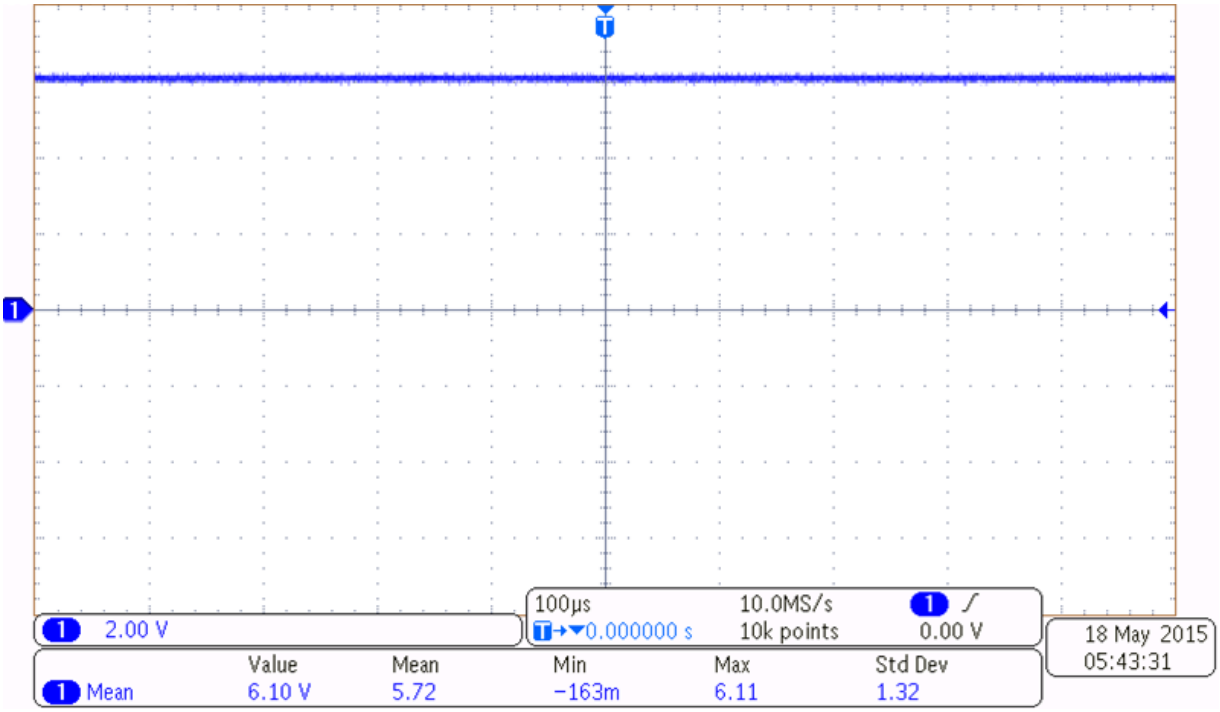


Figure 28. 6-V Signal from TPS62150

Figure 29 shows the ripple measured on the same 6 V. The ripple value is 100 mV.

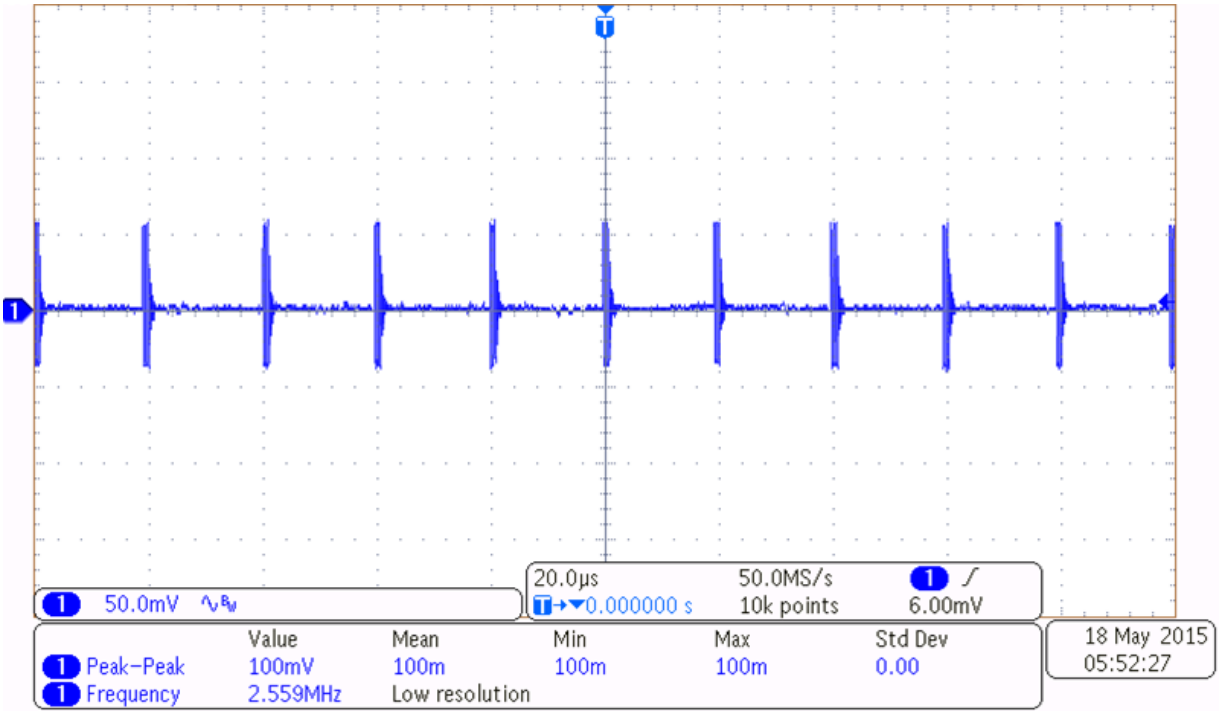


Figure 29. Ripple on 6-V Signal

Figure 30 shows the 5-V supply voltage generated using the LP2992 device.

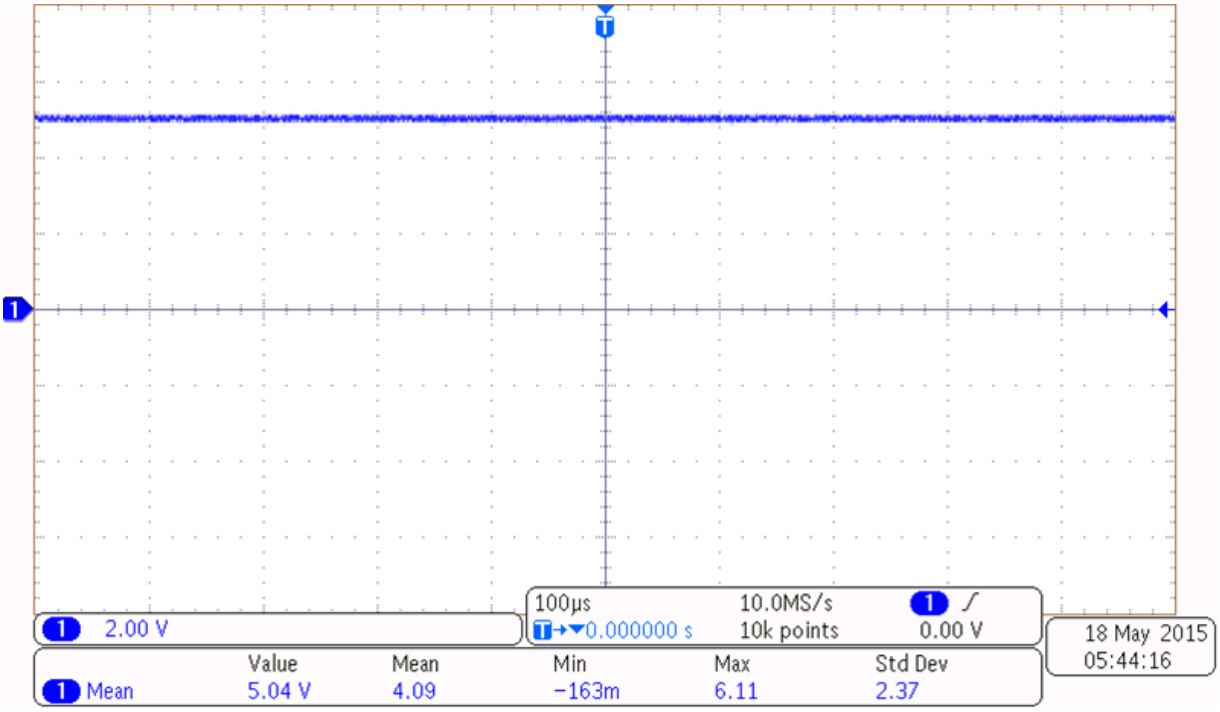


Figure 30. 5-V Signal Generated by LP2992

Figure 31 shows the ripple measured on the same 5 V. The ripple value is much less than 10 mV. The signal captured in Figure 31 also includes noise from the oscilloscope itself. The peak-to-peak ripple is much less than what is visible.

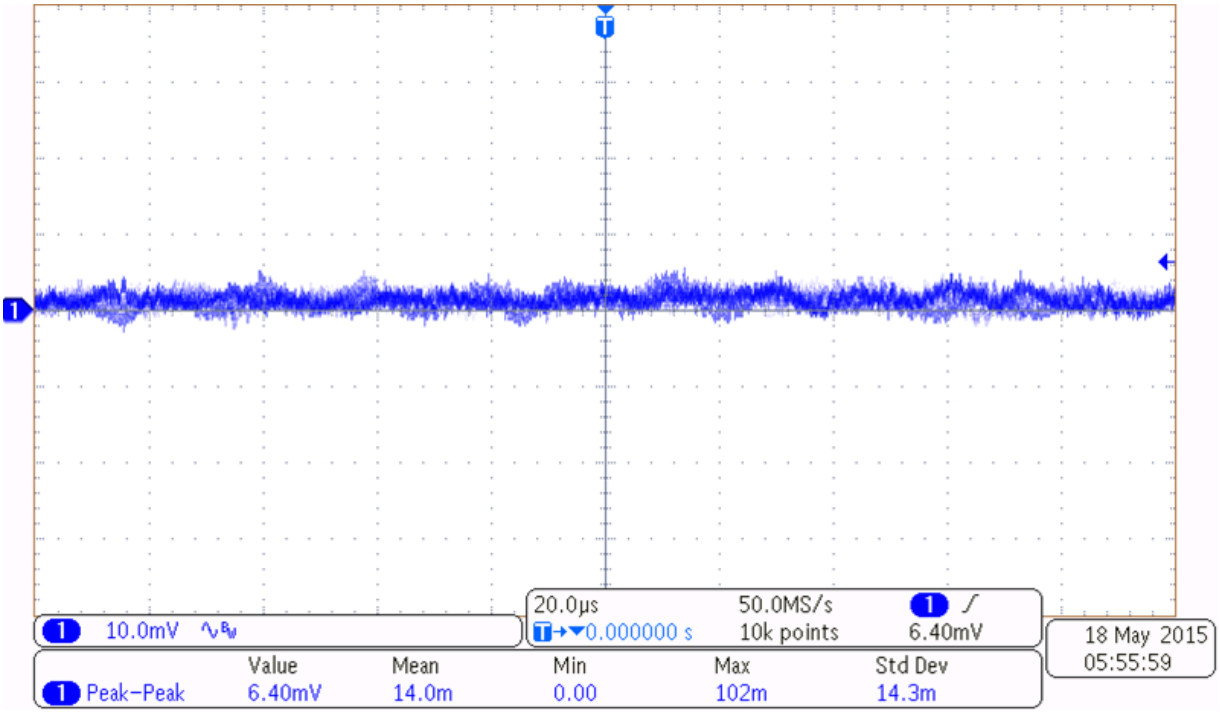


Figure 31. Ripple on 5-V Signal

Figure 32 shows the output of the TPS7A4901 device set at 12 V.

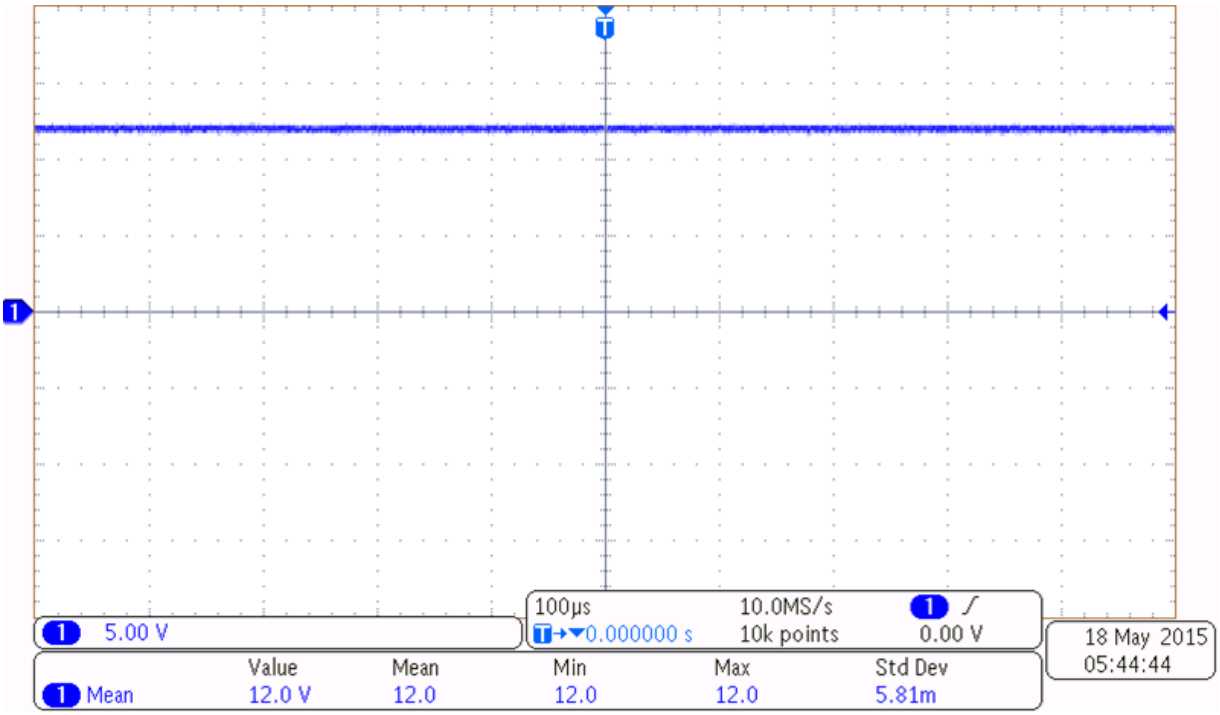


Figure 32. +12-V Signal from TPS7A4901

Figure 33 shows the ripple measured on the same 12 V. The ripple value is less than 10 mV. The signal captured in Figure 33 also includes noise from the oscilloscope itself. The peak-to-peak ripple is much less than what is visible.

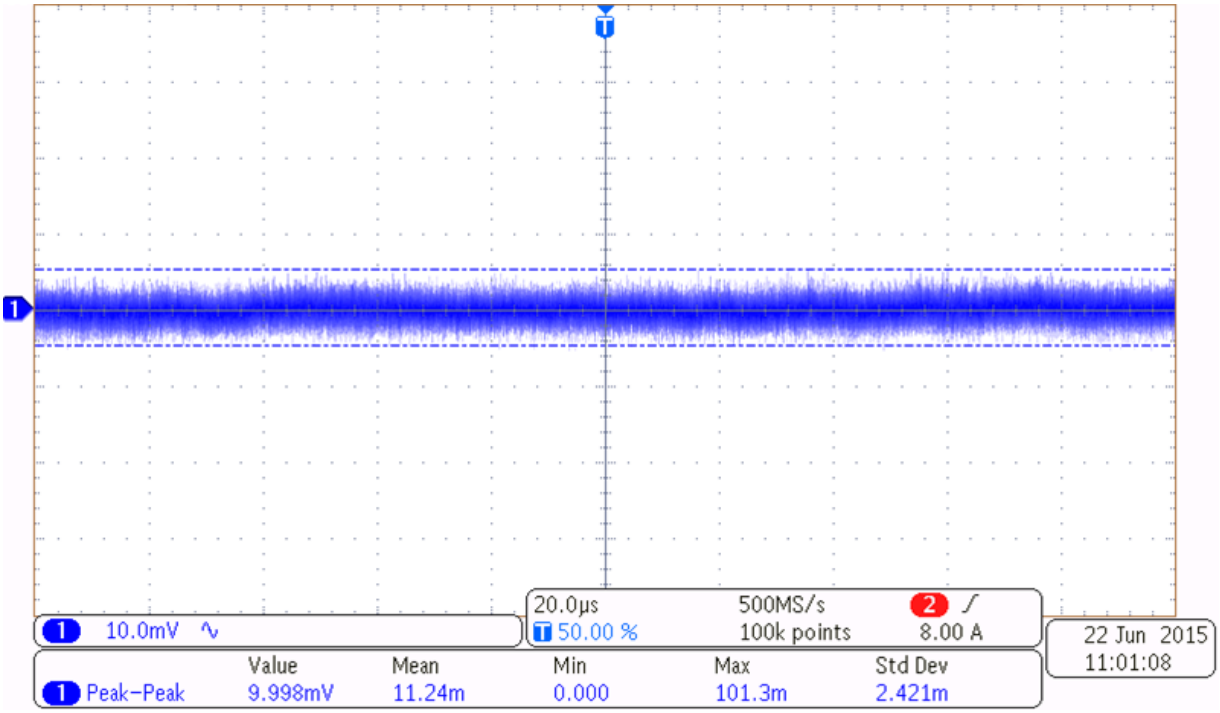


Figure 33. Ripple on 12-V Signal

Figure 34 shows the output of the TPS7A3001 device set at −12 V.

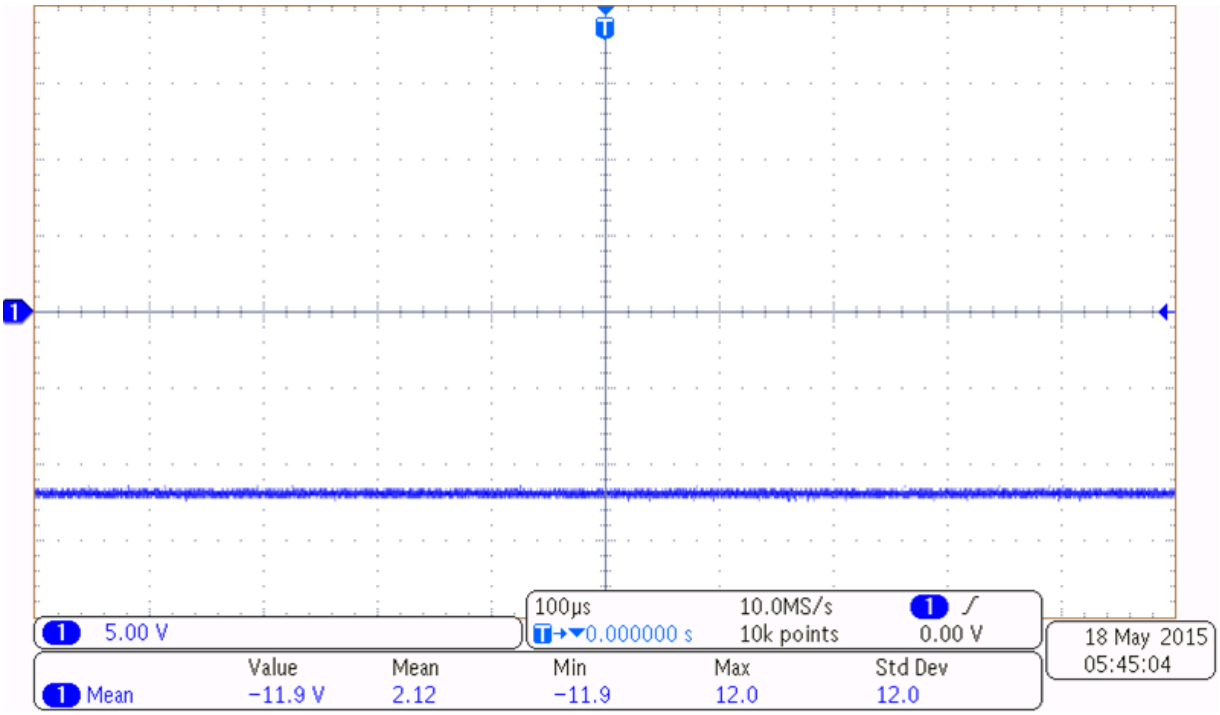


Figure 34. −12-V Signal from TPS7A3001

Figure 35 shows the ripple measured on the same −12 V. The ripple value is much less than 10 mV. The signal captured in Figure 35 also includes noise from the oscilloscope itself. The peak-to-peak ripple is much less than what is visible.

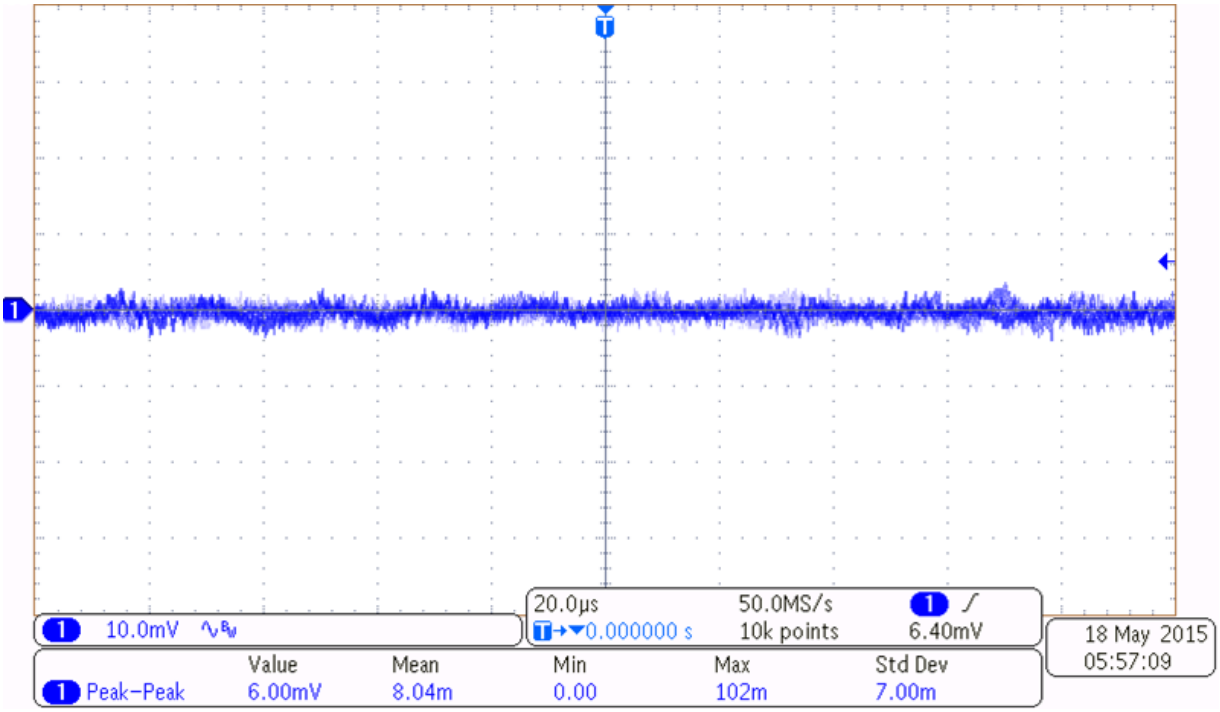


Figure 35. Ripple on −12-V Signal

Figure 36 and Figure 37 show the two outputs of the REF2025 reference set internally at 2.5 V and 1.25 V, respectively.

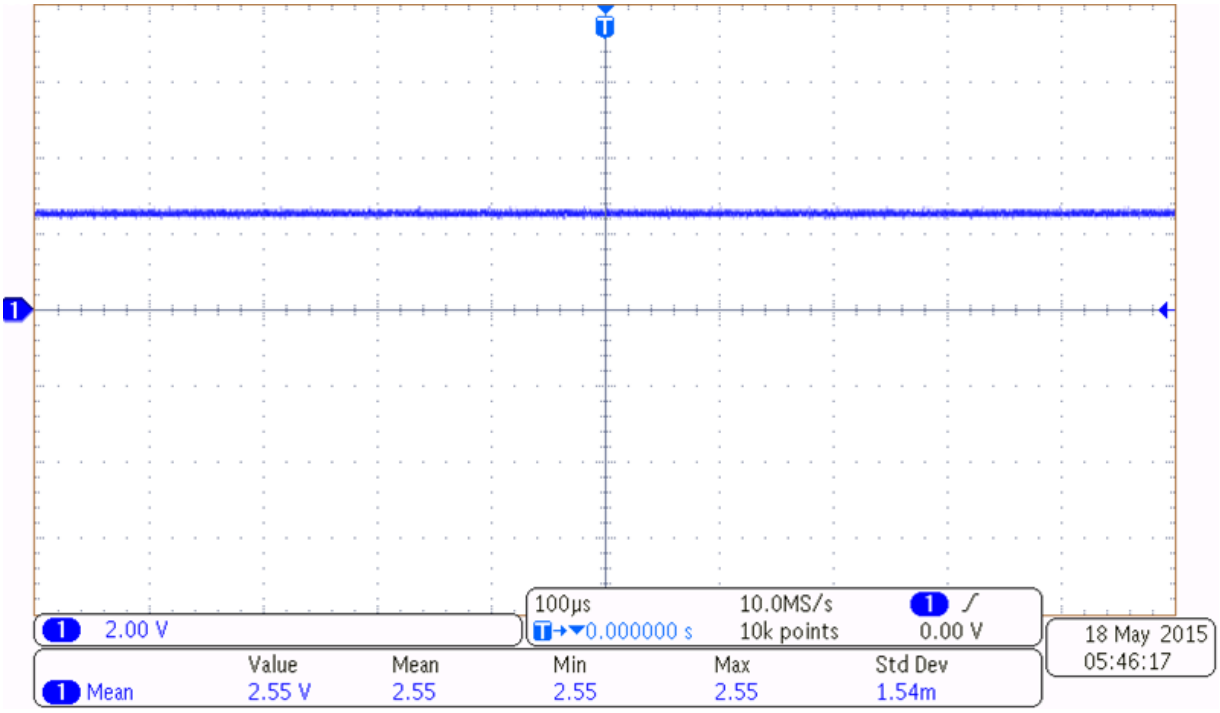


Figure 36. 2.5-V Reference Signal Generated by REF2025

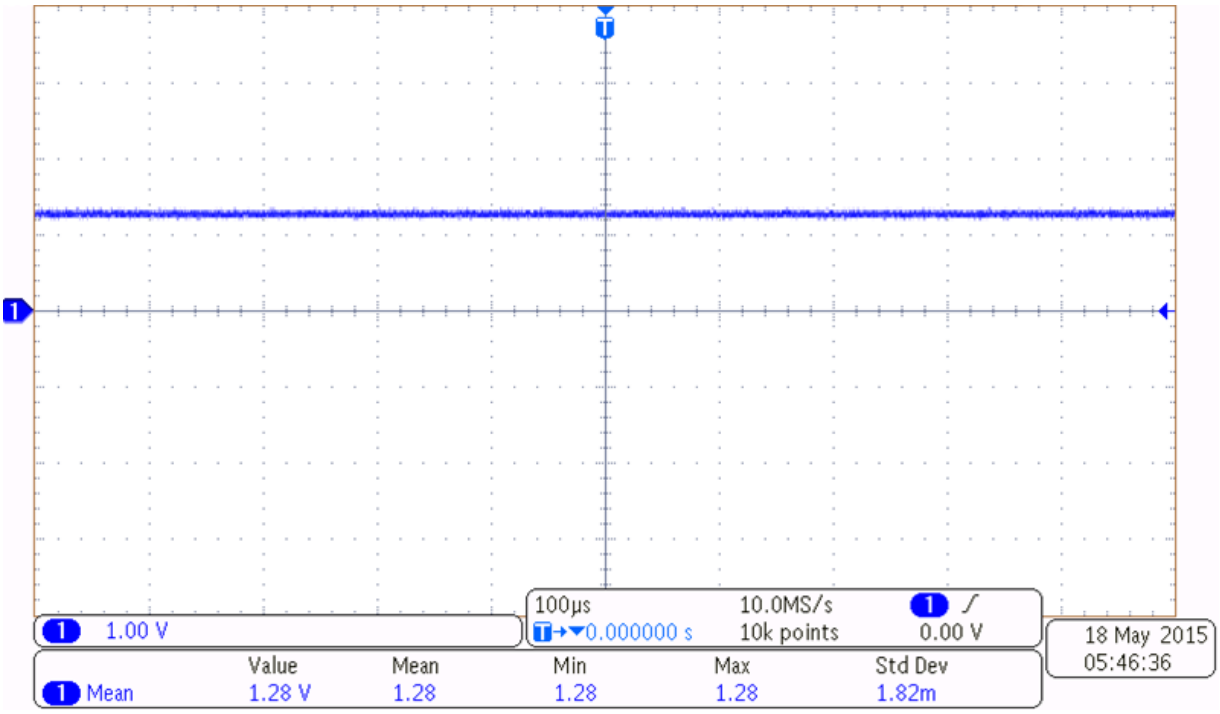


Figure 37. 1.25-V Reference Signal Generated by REF2025

7.2 Power Consumption of Board Under Different Test Conditions

The following Table 7 shows the power consumption of the TIDA-00368 board under different test conditions.

Table 7. Power Consumption Test Data

1	TIDA-00368 BOARD POWERED UP WITH ±15 V (NO CURRENT PASSING THROUGH THE HALL SENSOR)					
	Vin+	14.997	Vin–	15		
	Iin+	0.041	Iin–	0.013		
	Pin+	0.614877	Pin–	0.195	Total power	0.809877
2	TIDA-00368 BOARD POWERED UP WITH ±15 V AND 8 A PASSING THROUGH THE HALL SENSOR					
	Vin+	14.997	Vin–	15		
	Iin+	0.066	Iin–	0.012		
	Pin+	0.989802	Pin–	0.18	Total power	1.169802
3	TIDA-00368 BOARD POWERED UP WITH ±15 V AND –8 A PASSING THROUGH THE HALL SENSOR					
	Vin+	14.997	Vin–	15		
	Iin+	0.041	Iin–	0.037		
	Pin+	0.614877	Pin–	0.555	Total power	1.169877
4	TIDA-00368 BOARD POWERED UP AND F2837X CONTROL CARD CONNECTED (NO CURRENT PASSING THROUGH THE HALL SENSOR)					
	Vin+	14.997	Vin–	15		
	Iin+	0.112	Iin–	0.013		
	Pin+	0.614877	Pin–	0.198	Total power	1.874664
5	TIDA-00368 BOARD POWERED UP AND F2837X CONTROL CARD CONNECTED (8 A PASSING THROUGH THE HALL SENSOR)					
	Vin+	14.997	Vin–	15		
	Iin+	0.137	Iin–	0.012		
	Pin+	2.054589	Pin–	0.18	Total power	2.234589
6	TIDA-00368 BOARD POWERED UP AND F2837X CONTROL CARD CONNECTED (–8 A PASSING THROUGH THE HALL SENSOR)					
	Vin+	14.997	Vin–	15		
	Iin+	0.113	Iin–	0.037		
	Pin+	1.694661	Pin–	0.555	Total power	2.249661

7.3 DC Performance Tests

Knowing the DC accuracy and performance is important for any signal conditioning circuit. Note that in a typical drive application, the current sensor is used from 30% to 100% of its nominal current rating. So consider the accuracy of a primary current from ±2 A to ±8 A for the LAH 25-NP device.

7.3.1 DC Performance of Differential Signal Conditioning Circuit

To analyze the DC performance of the differential signal conditioning circuit, use the ADS7254EVM and ADS8354EVM (for 12-bit and 16-bit performance respectively) along with the TIDA-00368 board, as Figure 27 shows. The DC accuracy is measured at each of the following stages:

1. On TIDA-00368 board:
   - Sensor output
   - Output of level-shifting op-amp (OPA322)
   - Output of differential amplifier (THS4531A)
2. On ADC board:
   - Input of ADC
   - Output data on ADC GUI

7.3.1.1 DC Performance of Signal Chain (Level-Shifting Amplifier, Differential Amplifier, and ADC)

The DC accuracy is observed for the differential signal chain. Figure 38 and Figure 39 show the two accuracy graphs for a negative current range (−1 A to −8 A) and a positive current range (1 A to 8 A), respectively.

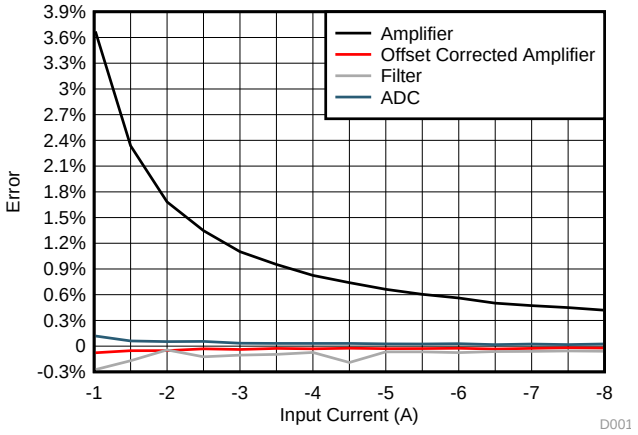


Figure 38. Signal Chain DC Accuracy (for Negative Input Current Range)

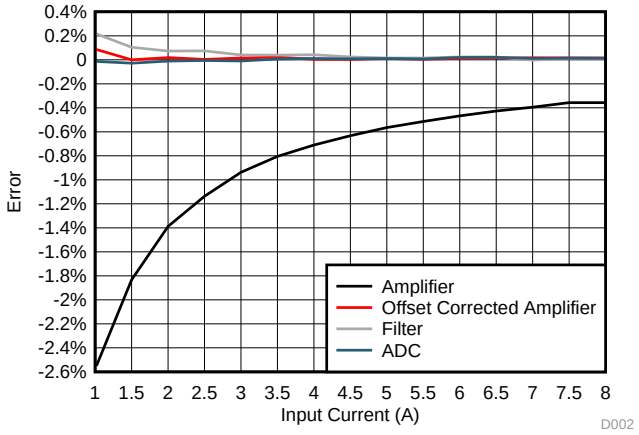


Figure 39. Signal Chain DC Accuracy (for Positive Input Current Range)

7.3.1.2 DC Performance of Differential Signal Chain With ADS7254EVM (12-Bit ADC)

The total DC accuracy is measured at 25°C, 75°C, and −25°C. Figure 40 and Figure 41 show the two accuracy graphs for a negative current range (−1 A to −8 A) and a positive current range (1 A to 8 A), respectively.

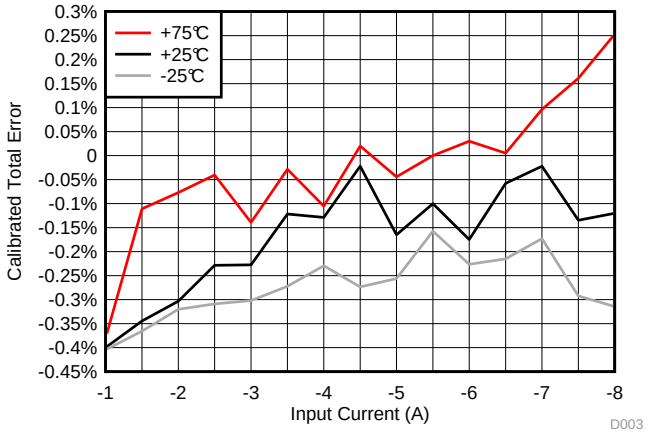


Figure 40. Differential Signal Chain Circuit DC Accuracy at Three Different Temperatures (For Negative Input Current Range) With 12-Bit ADC

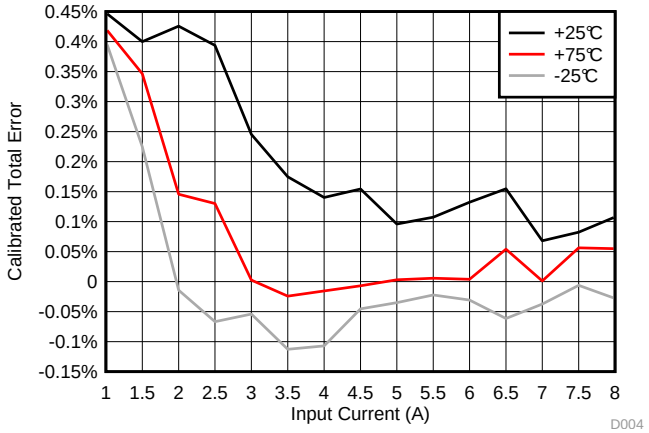


Figure 41. Differential Signal Chain Circuit DC Accuracy at Three Different Temperatures (For Positive Input Current Range) With 12-Bit ADC

While measuring the voltages at each of the outputs of the differential signal chain for Figure 40, the following changes in the reference voltages are observed:

At −25°C the reference voltage on the TIDA-00368 board changes by 1.5 mV and the reference on the ADS7254EVM device changes by 1.4 mV throughout the negative input current range. At 75°C the reference voltage on the TIDA-00368 board changes by 1.7 mV and the reference on the ADS7254EVM device changes by 1.7 mV throughout the negative input current range.

While measuring the voltages at each of the outputs of the differential signal chain for Figure 41, the following changes in the reference voltages are observed:

At −25°C the reference voltage on the TIDA-00368 board changes by 1.6 mV and the reference on the ADS8354EVM device changes by 1.6 mV throughout the positive input current range. At 75°C the reference voltage on the TIDA-00368 board changes by 2 mV and the reference on the ADS8354EVM device changes by 1.9 mV throughout the positive input current range.

The DC code histogram is also observed using the ADS7254EVM GUI. Figure 42 shows this DC code histogram. The histogram shows that the effective number of bits (ENOB) (calculated using standard deviation) = 12 bits and the noise free bits (calculated using peak-to-peak noise) = 12 bits.

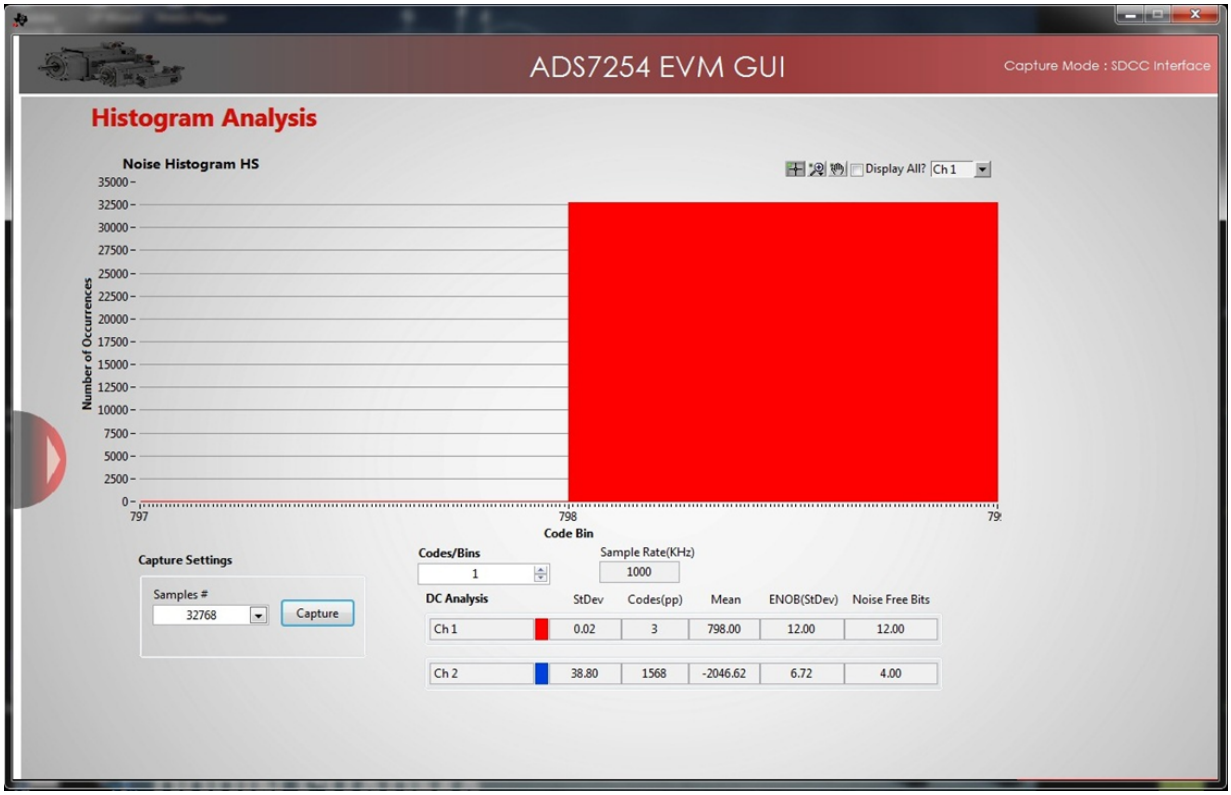


Figure 42. DC Code Histogram

7.3.1.3 DC Performance of Differential Signal Chain With ADS8354EVM (16-Bit ADC)

The total DC accuracy is measured at 25°C, 75°C, and −25°C. Figure 43 and Figure 44 show the two accuracy graphs for a negative current range (−1 A to −8 A) and a positive current range (1 A to 8 A), respectively.

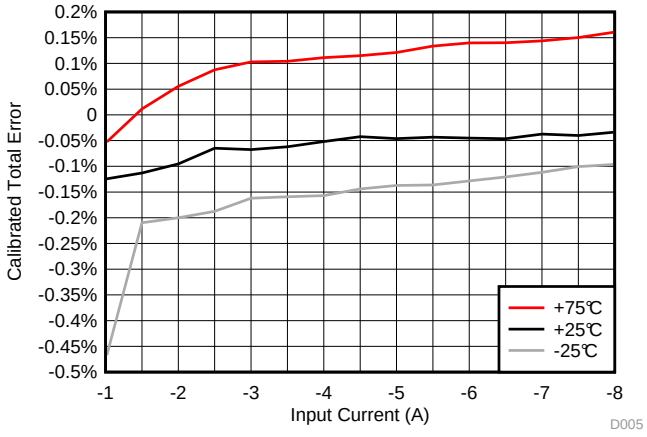


Figure 43. Differential Signal Chain Circuit DC Accuracy at Three Different Temperatures (For Negative Input Current Range) With 16-Bit ADC

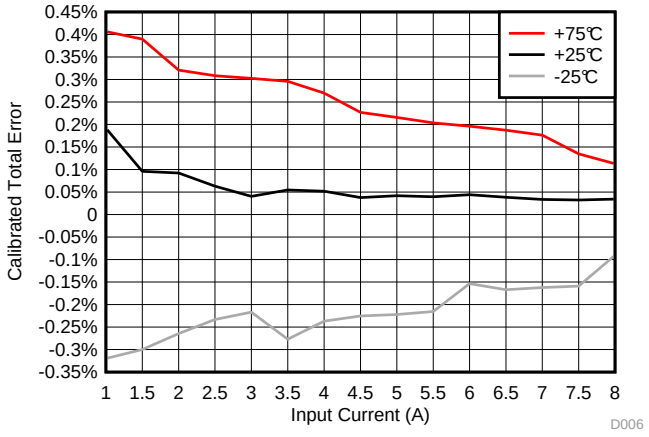


Figure 44. Differential Signal Chain Circuit DC Accuracy at Three Different Temperatures (For Positive Input Current Range) With 16-Bit ADC

While measuring the voltages at each of the outputs of the bipolar signal for Figure 43, the following changes in the reference voltages are observed:

At −25°C the reference voltage on the TIDA-00368 board changes by 1.5 mV and the reference on the ADS8354EVM device changes by 1.5 mV throughout the negative input current range. At 75°C the reference voltage on the TIDA-00368 board changes by 1.5 mV and the reference on the ADS8354EVM changes by 1.6 mV throughout the negative input current range.

While measuring the voltages at each of the outputs of the differential signal chain for Figure 44, the following changes in the reference voltages are observed:

At −25°C the reference voltage on the TIDA-00368 board changes by 1.7 mV and the reference on the ADS8354EVM changes by 1.6 mV throughout the negative input current range. At 75°C the reference voltage on the TIDA-00368 board changes by 1.9 mV and the reference on the ADS8354EVM changes by 1.9 mV throughout the negative input current range.

The DC histogram is observed using the ADS8354EVM GUI. Figure 45 shows this DC code histogram. The histogram shows that the ENOB (calculated using standard deviation) = 15.71 bits and the noise free bits (calculated using peak-to-peak noise) = 12.99 bits.

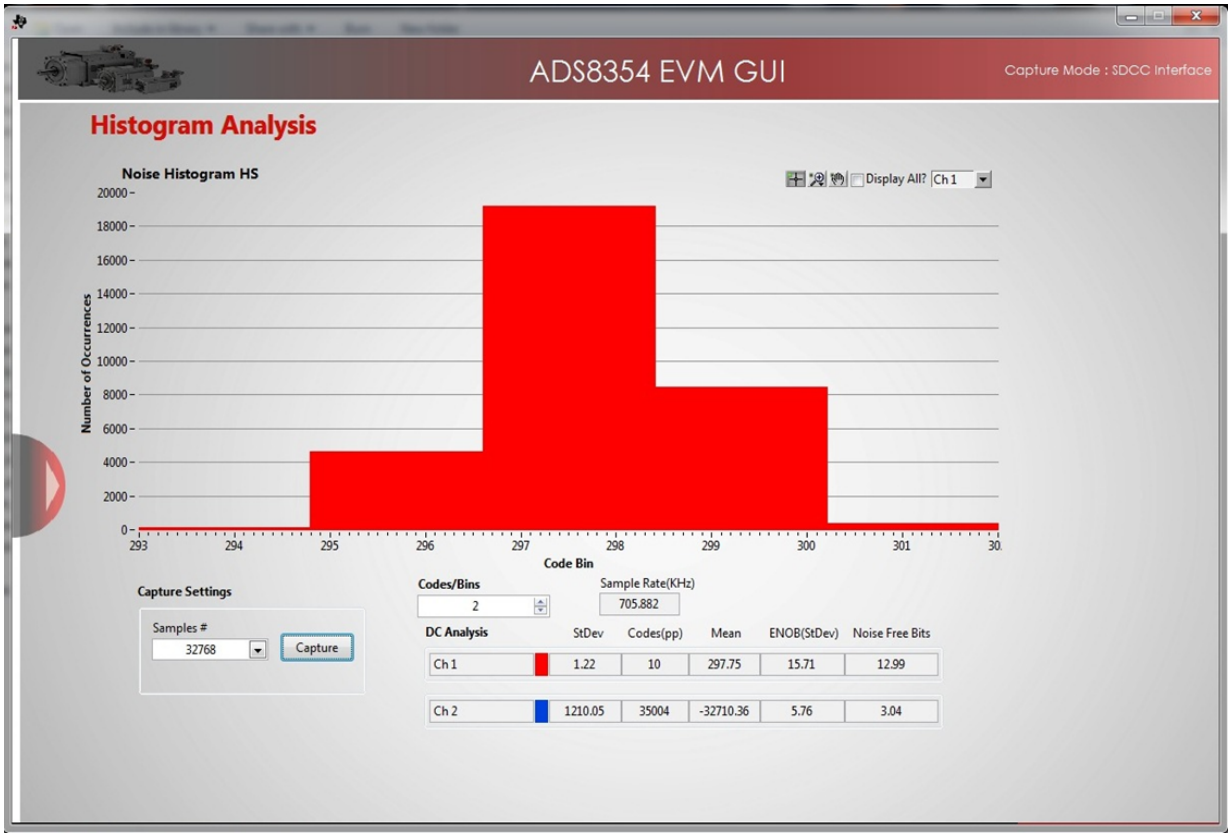


Figure 45. DC Code Histogram

7.3.1.4 DC Performance of Differential Signal Conditioning Circuit Using TI's Delfino™ F2837x Internal ADC

The DC accuracy of the differential signal conditioning circuit is also measured using the internal ADC of the Delfino F2837x device. Figure 46 shows the DC accuracy graph for a negative input current range and Figure 47 shows the DC accuracy graph for a positive input current range.

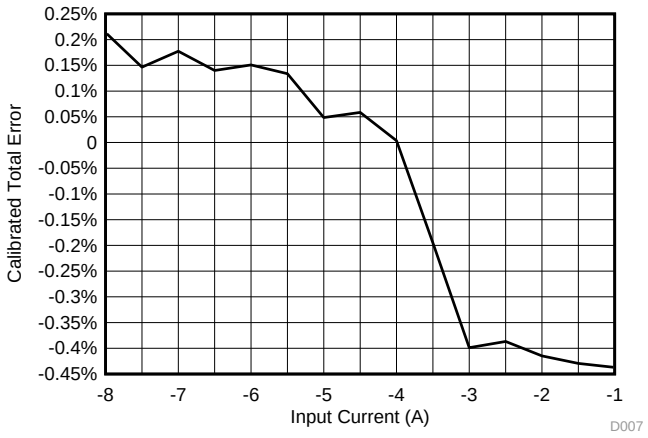


Figure 46. Differential Signal Chain Circuit DC Accuracy (For Negative Input Current Range) With 16-Bit Internal ADC of Delfino™ Controller from TI

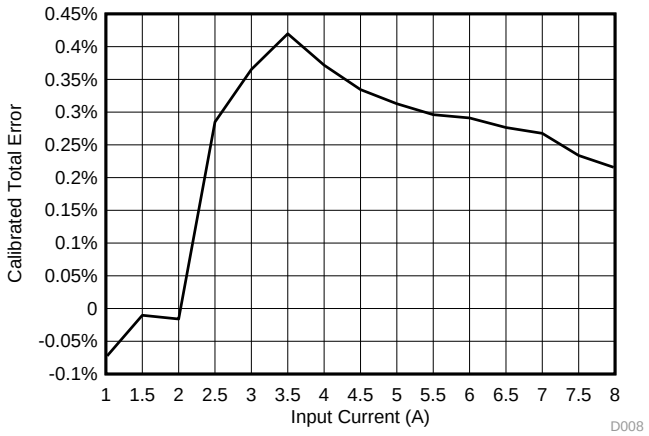


Figure 47. Differential Signal Chain Circuit DC Accuracy (For Positive Input Current Range) With 16-Bit Internal ADC of Delfino™ Controller from TI

7.4 AC (or Dynamic) Performance

An essential task for any data acquisition system is to achieve an excellent dynamic performance while minimizing the total power consumption of the system. The main AC specifications to consider are the total harmonic distortion (THD), signal-to-noise ratio (SNR), signal-to-noise and distortion ratio (SINAD), and ENOB. Essentially, all of these parameters are different ways of quantifying the noise and distortion performance of an ADC that is based on a fast-Fourier transform (FFT) analysis. Figure 48 shows a typical FFT plot for an ADC.

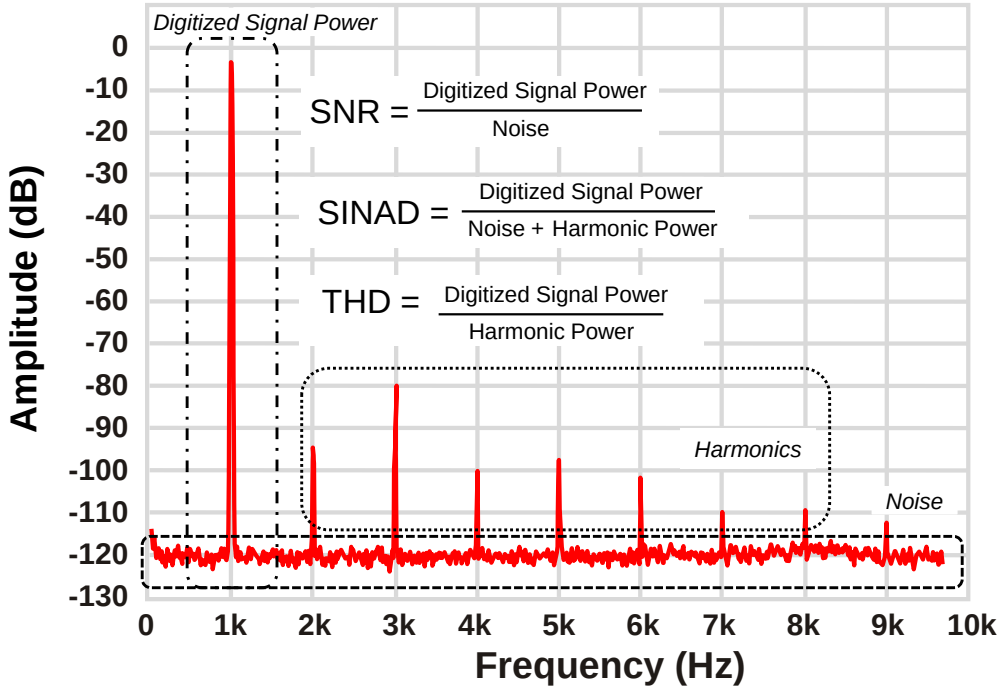


Figure 48. Typical FFT Plot Showing Different Dynamic Parameters

Signal-to-noise ratio (SNR)

The SNR provides insight into the total noise of the system. The total noise of the data acquisition system is the rss of the front-end amplifier noise ($V_{n\_AMP\_RMS}$) and the ADC noise ($V_{n\_ADC\_RMS}$). The ADC noise includes the quantization noise as well as the noise contributed by the ADC internal circuitry, or the input-referred noise of the ADC. The total noise contributions from all these sources, denoted as $V_{n\_TOT\_RMS}$, are referred to the input of the ADC to calculate the total SNR of the system (SNR_{SYS}) in Equation 10:

$$V_{n\_TOT\_RMS} = \sqrt{V_{n\_AMP\_RMS}^2 + V_{n\_ADC\_RMS}^2}$$

$$SNR_{SYS} = \frac{V_{SIG\_RMS}}{V_{n\_TOT\_RMS}} \quad (10)$$

Effective number of bits (ENOB)

The ENOB is an effective measurement of the quality of a digitized signal from an ADC by specifying the number of bits above the noise floor. For an ideal N-bit ADC with only quantization noise, the SNR (in dB) can be calculated as the following Equation 11 shows:

$$SNR = 6.02 \times N + 1.76 \quad (11)$$

While ENOB provides a good summary of the ADC dynamic performance, it does not describe the converter's entire performance over the operating frequency ranges and input signals. Additionally, the ENOB does not include the ADC DC specifications, such as offset and gain error. This means that the user must also pay attention to other converter specifications depending on the application in which the ADC is being used.

7.4.1 AC Performance of Differential Signal Conditioning Circuit Using ADS8354EVM

Observe and capture the waveform signal as well as the FFT of the signal with the following test conditions, the waveform signal as well as FFT of the signal is observed and captured using the ADS8354EVM device with the following test conditions:

- Input current flowing through the LAH 25-NP = ±8 A (peak-to-peak) at 50 Hz
- Corresponding output voltage of the LAH 25-NP (with burden resistor = 42.2 Ω) = ±1.05 V (peak-to-peak)

The following list shows the settings for the ADS8354EVM GUI while capturing the signal:

- Number of samples = 32768
- Sample rate = 476.471 KHz
- Internal reference = 2.5 V
- V_{REF} mode selected

Figure 49 shows the waveform captured using the ADS8354EVM GUI. The measured voltage is approximately 2 V (peak-to-peak) at 50 Hz.

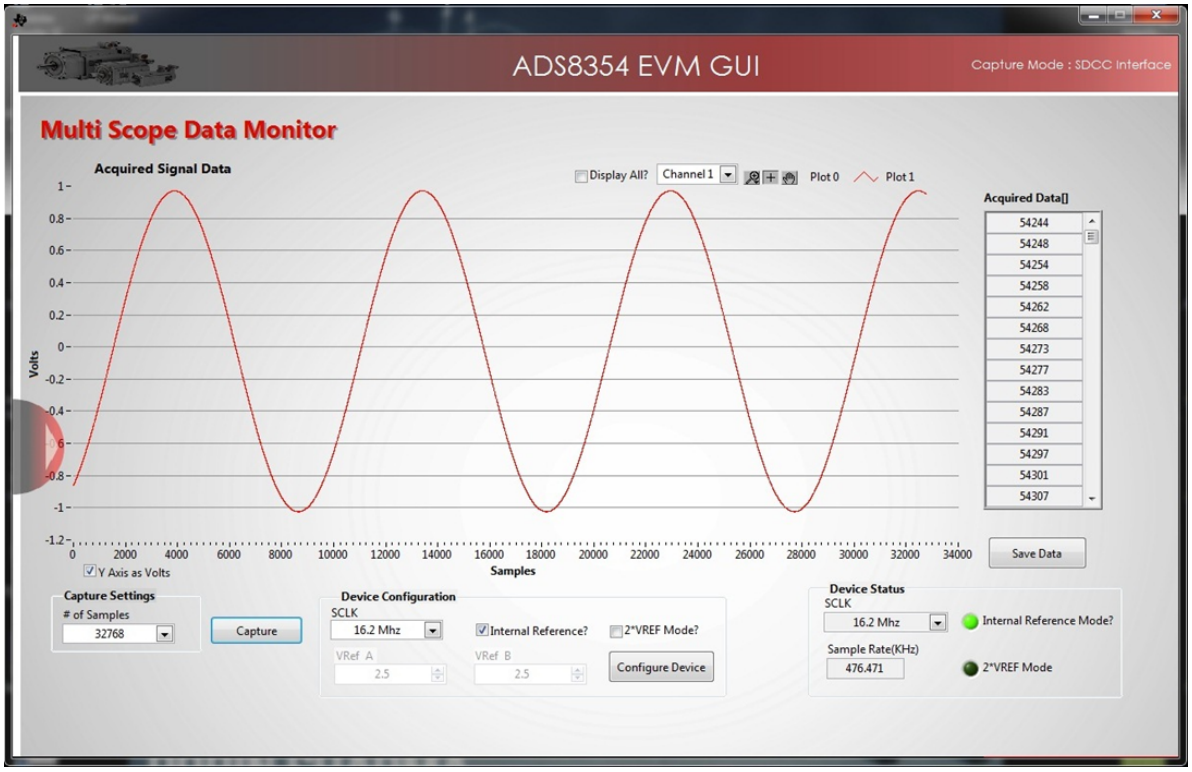


Figure 49. Current Waveform Captured With ADS8354EVM GUI

For the same signal, use the ADS8354EVM GUI to capture the FFT. The settings for capturing the FFT are:

- Number of samples = 65536
- Window = 7-term B-Harris
- Sample rate = 705.88 KHz

Figure 50 shows the FFT signal captured using the ADS8354EVM GUI. The measured SNR at the signal level of −7.97452 dBFS is 84.1058 dB. An important thing to note is that the 8-A current is not the full-scale value for which the signal chain is designed. For this reason, the signal level shows −7.97452 dBFS and not 0 dBFS.

Figure 50. FFT Captured With ADS8354EVM GUI

The observed results are:

- SNR = 84.1058 dB
- THD = −94.6940 dB
- SINAD = 83.7422 dB

Figure 51 shows the zoomed-in version of the FFT with a 50-Hz signal.

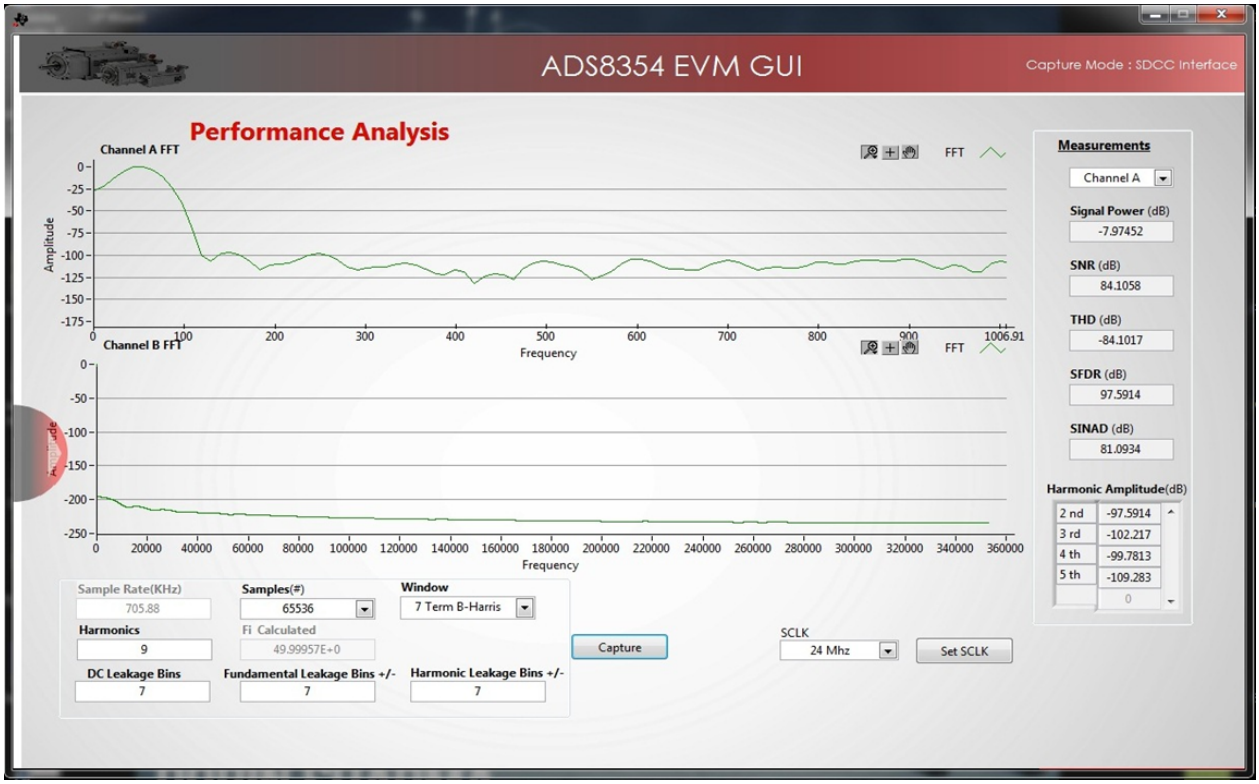


Figure 51. Zoomed-In FFT Showing 50-Hz Signal

7.4.2 AC Performance of Differential Signal Conditioning Circuit Using TI's Delfino F2837x Internal ADC

With the following test conditions, the waveform signal as well as FFT of the signal is observed and captured using the Delfino™ F2837x control card from Texas Instruments:

- Input current flowing through the LAH 25-NP = ±8 A (peak-to-peak) at 50 Hz
- Corresponding output voltage of the LAH 25-NP (with burden resistor = 27 Ω) = ±422 mV (peak-to-peak)

The following list shows the settings for the Delfino F2837x software while capturing the signal:

- ADC mode = differential
- Resolution = 16 bits
- ADC clock frequency = 15 MHz
- Throughput (including the ACQPS and conversion time) = 320.9847 KSPS
- Reference voltage = 2.5 V
- Supply voltage = 3.3 V
- Number of samples = 1048576
- FFT window = 7-term B-Harris

Figure 52 shows the waveform captured using the Delfino GUI.

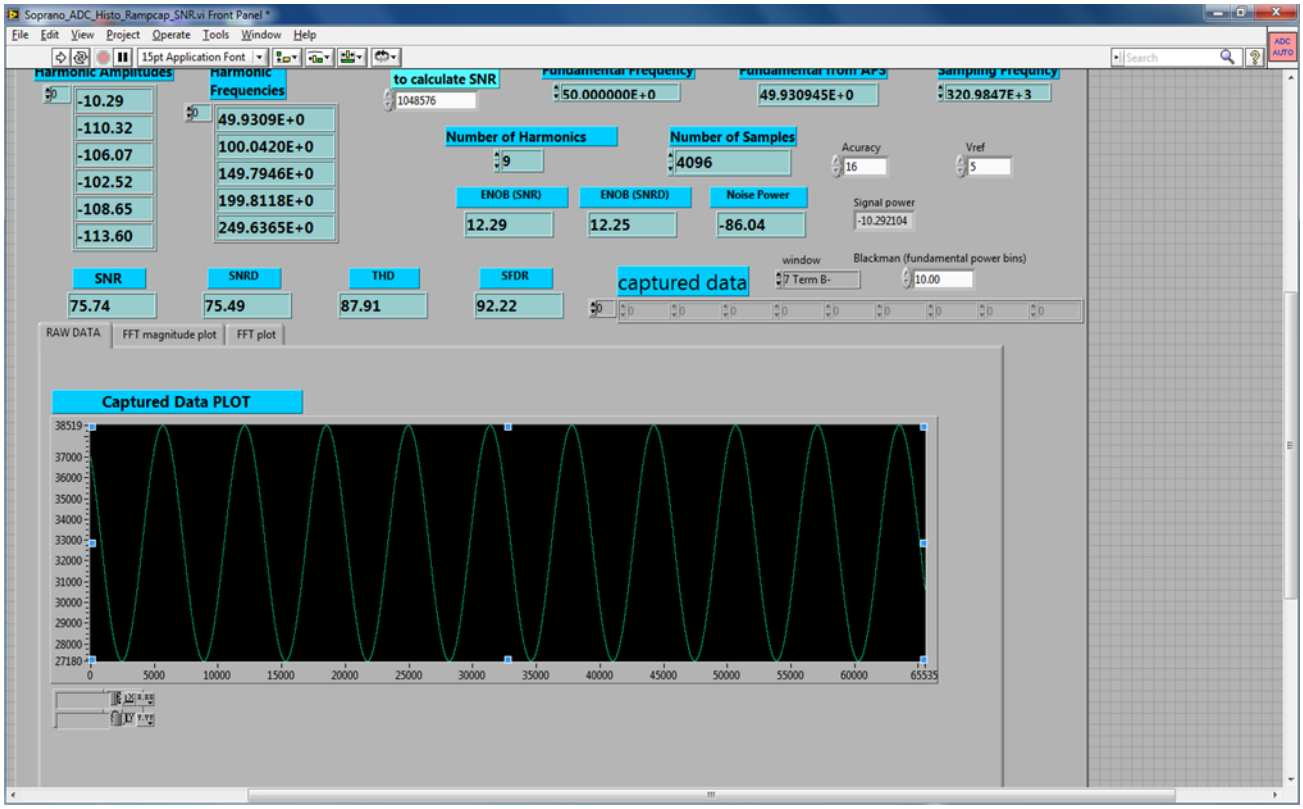


Figure 52. Current Waveform Captured With Delfino GUI From TI

For the same signal FFT is also captured using Delfino GUI. Figure 53 shows the FFT signal captured using the Delfino GUI.

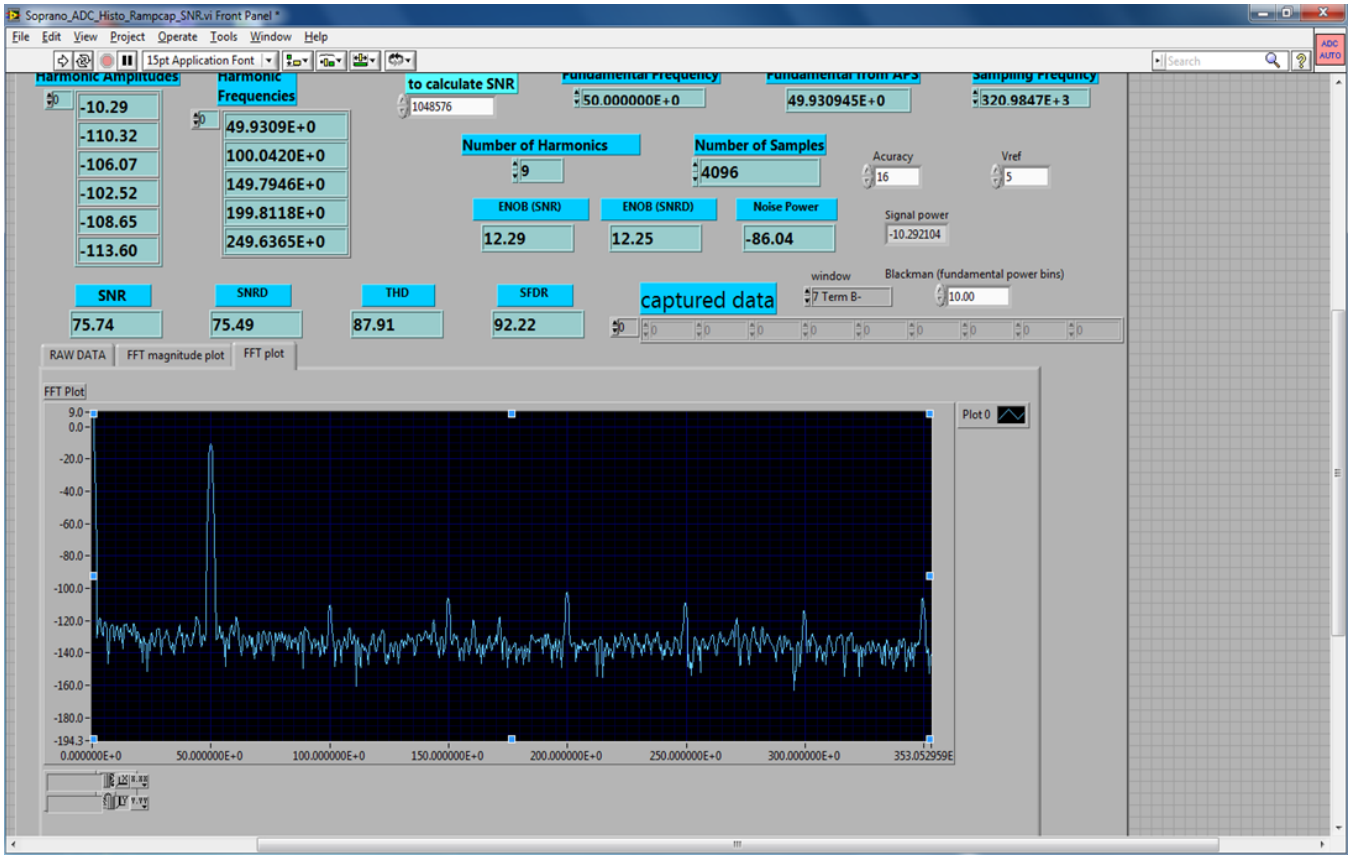


Figure 53. FFT Captured With Delfino GUI (Showing 50-Hz Signal)

The observed results are:

- SNR = 75.74 dB (with signal strength = −10.292104 dBFS)
- SINAD or SNRD = 75.49 dB
- THD = 87.91 dB
- SFDR = 92.22 dB
- ENOB (calculated using SNR) = 12.29 bits

The measured SNR at the signal level of −10.292104 dBFS is 75.74 dB. An important thing to note is that the 8-A current is not the full-scale value for which the signal chain is designed. For this reason, the signal level shows −10.292104 dBFS and not 0 dBFS.

7.5 Testing With ACIM and Motor Drive

The design is tested with a 3-kW AC motor drive and 2-HP AC induction motor. Figure 54 shows the test setup.

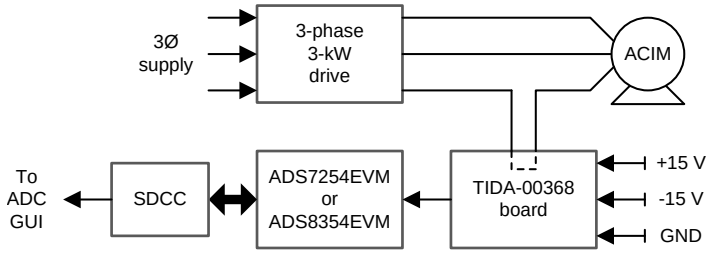


Figure 54. Test Setup Block Diagram

Figure 55 shows a picture of the physical test setup.

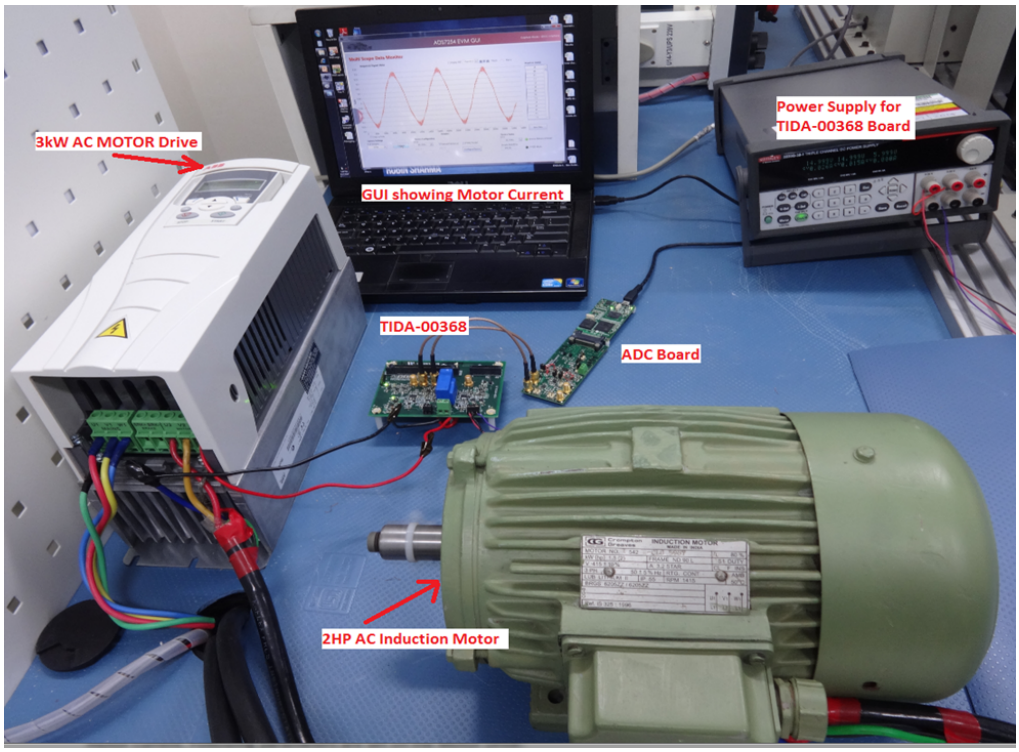


Figure 55. Image Showing Test Setup

As Figure 55 shows, the TIDA-00368 board is connected with the ADC board (ADS8354EVM) to capture the motor current. The following parameters are set on the motor drive:

- Motor voltage = 415-V AC
- Motor frequency = 50 Hz
- Motor speed = 1440 RPM
- Motor current = 1.4 A
- Acceleration and deceleration time = 5 seconds

The ADC board (ADS8354EVM) is connected to SMA jack J6 and J7 and the motor current is monitored using the ADS8354EVM GUI. The sinewave signal (see Figure 56) as well as the FFT (see Figure 58) of the motor current is captured using the ADS8354EVM GUI. The motor current is also measured with a current probe using an oscilloscope (see Figure 57). The inverter switching frequency of the motor drive (used for testing) is 4 KHz and is visible from the zoomed-in FFT plot (see Figure 59) as well as the FFT captured on the oscilloscope (see Figure 60).

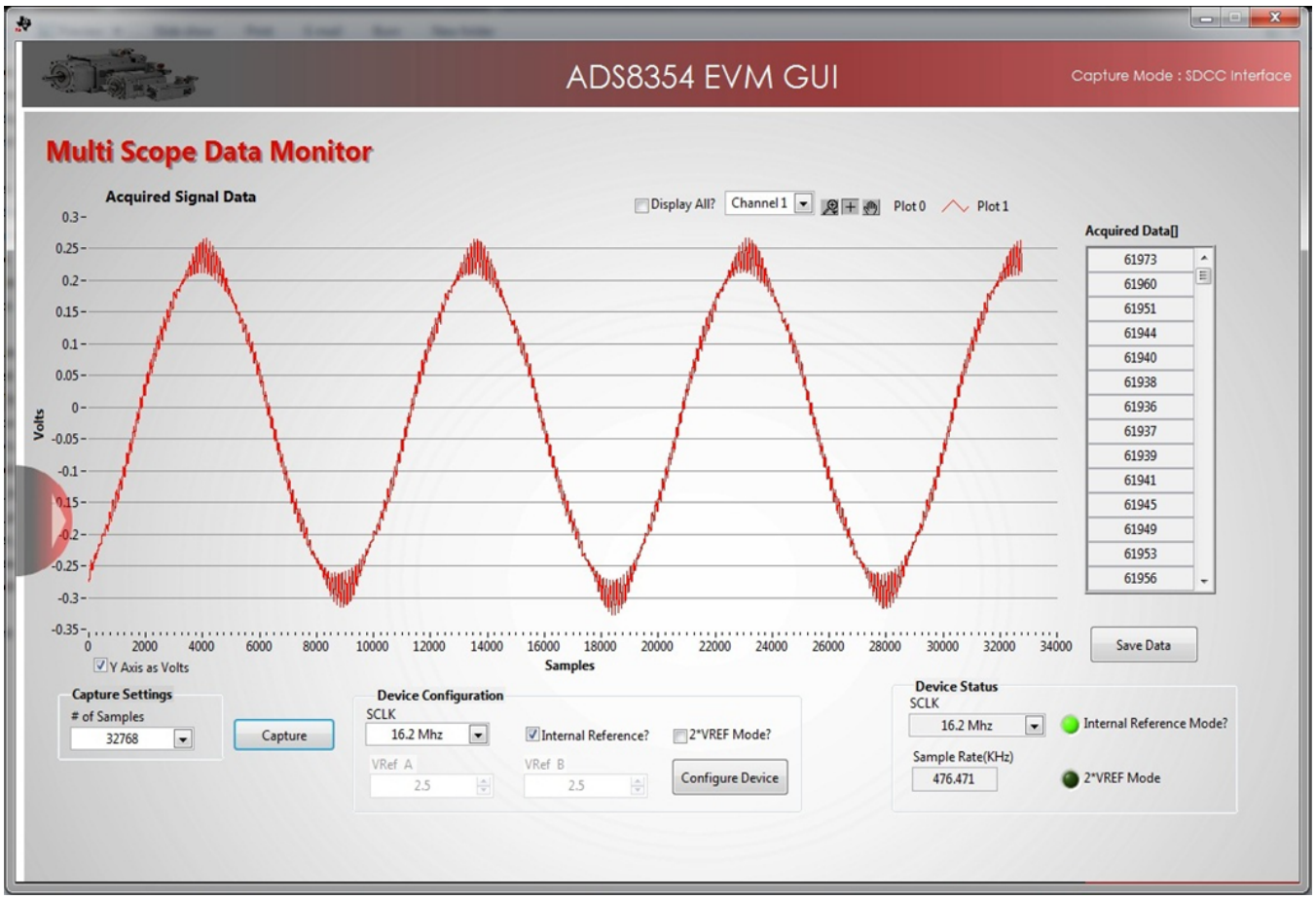


Figure 56. Motor Current Waveform Observed on ADS8354EVM GUI

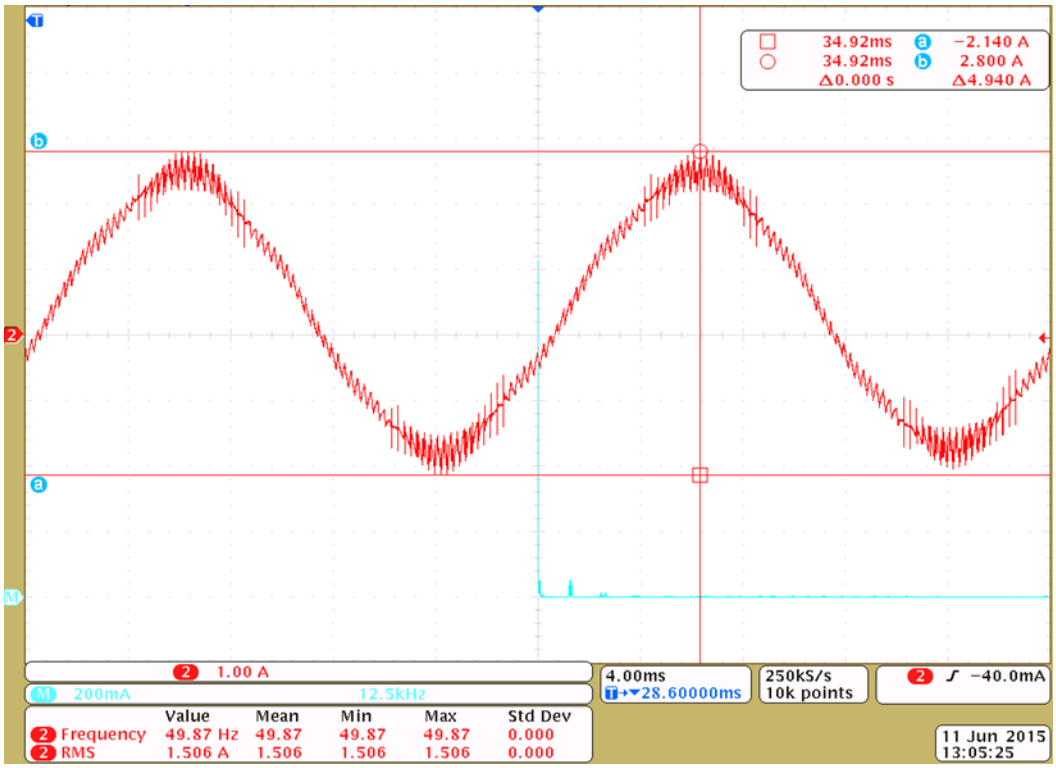


Figure 57. Motor Current Waveform Measured Using Oscilloscope

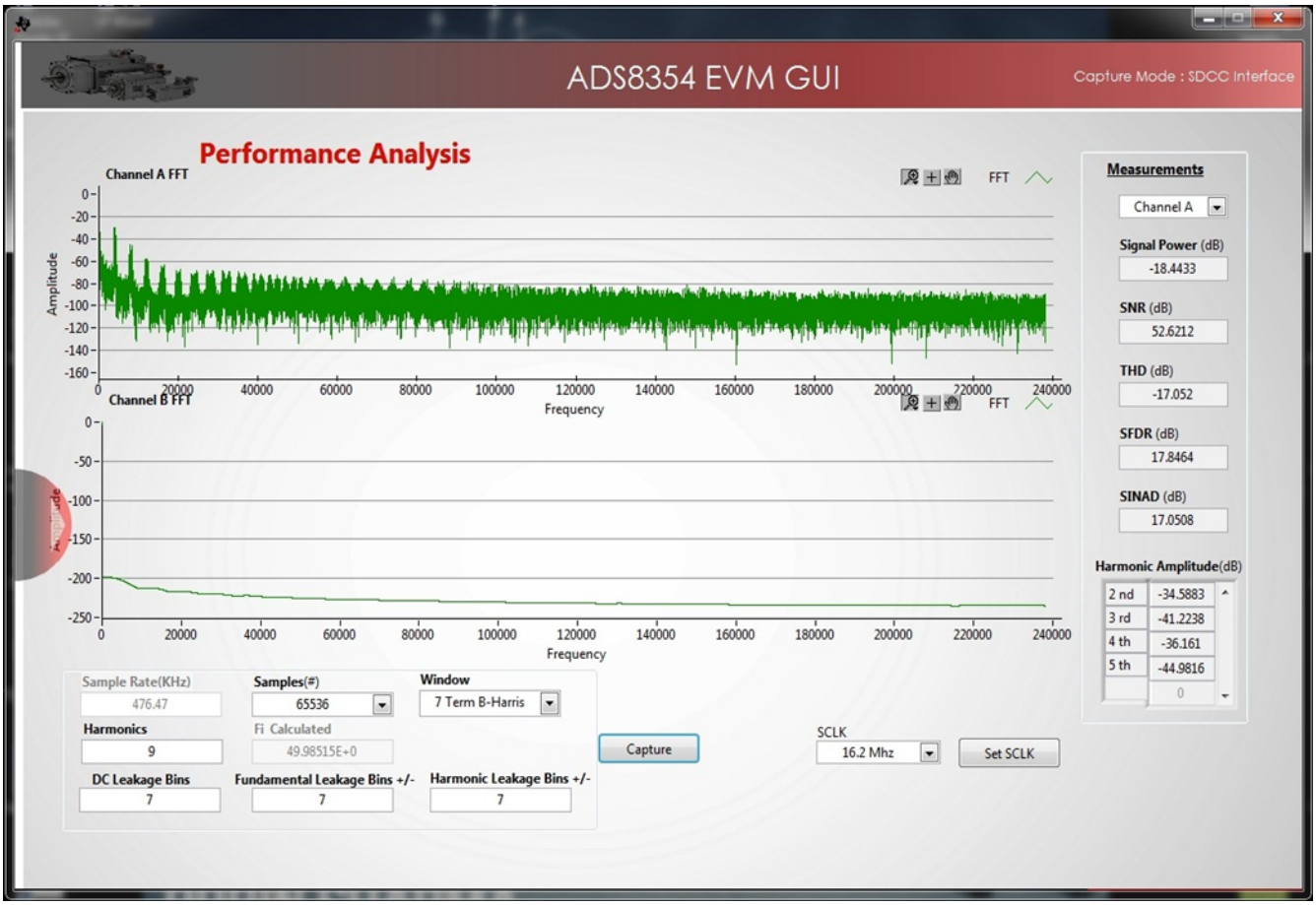


Figure 58. FFT of Motor Current (Measured Using ADS8354 EVM GUI)

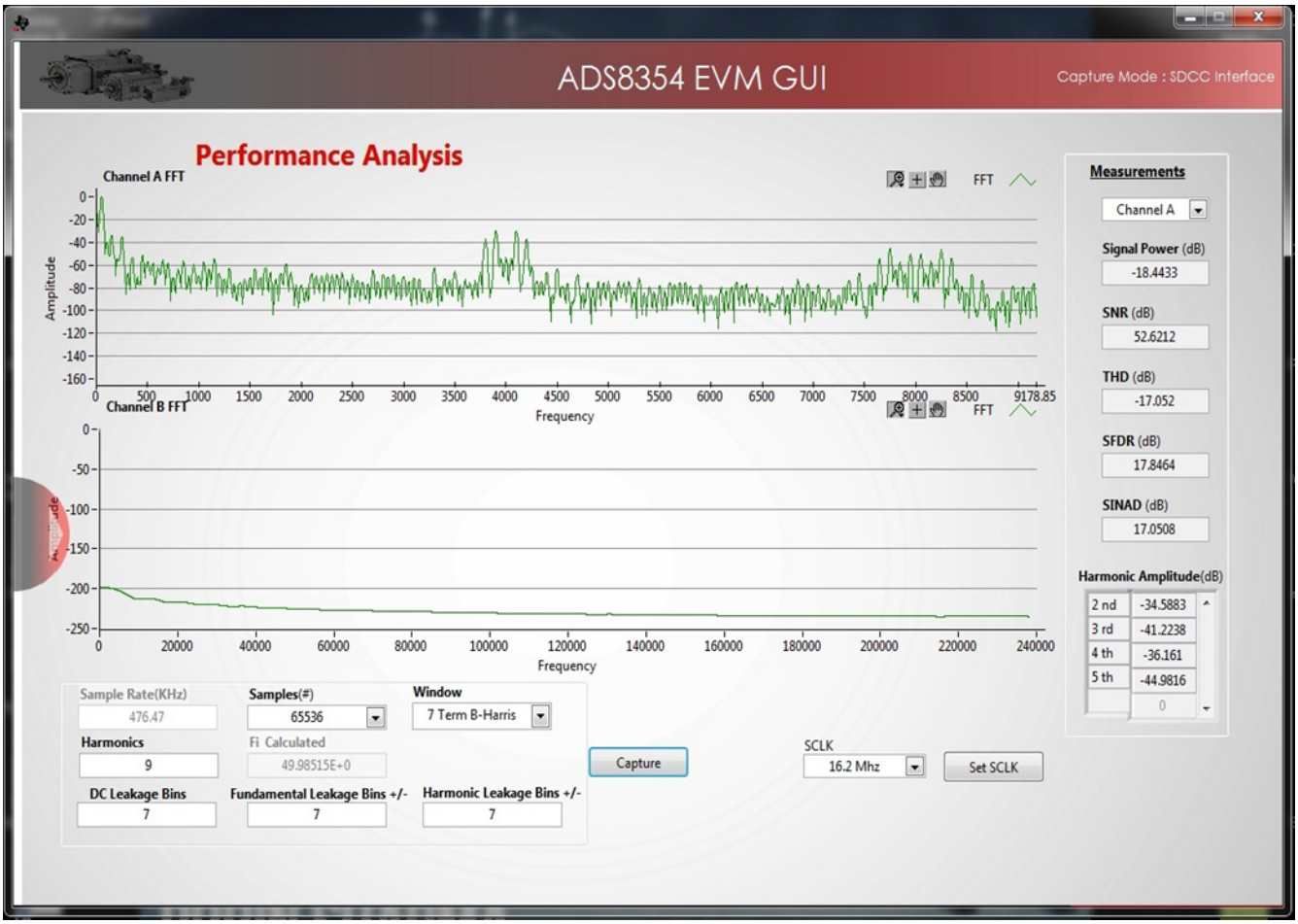


Figure 59. FFT of Motor Current (Zoomed-In) Showing Switching Frequency at 4 KHz and eHarmonics

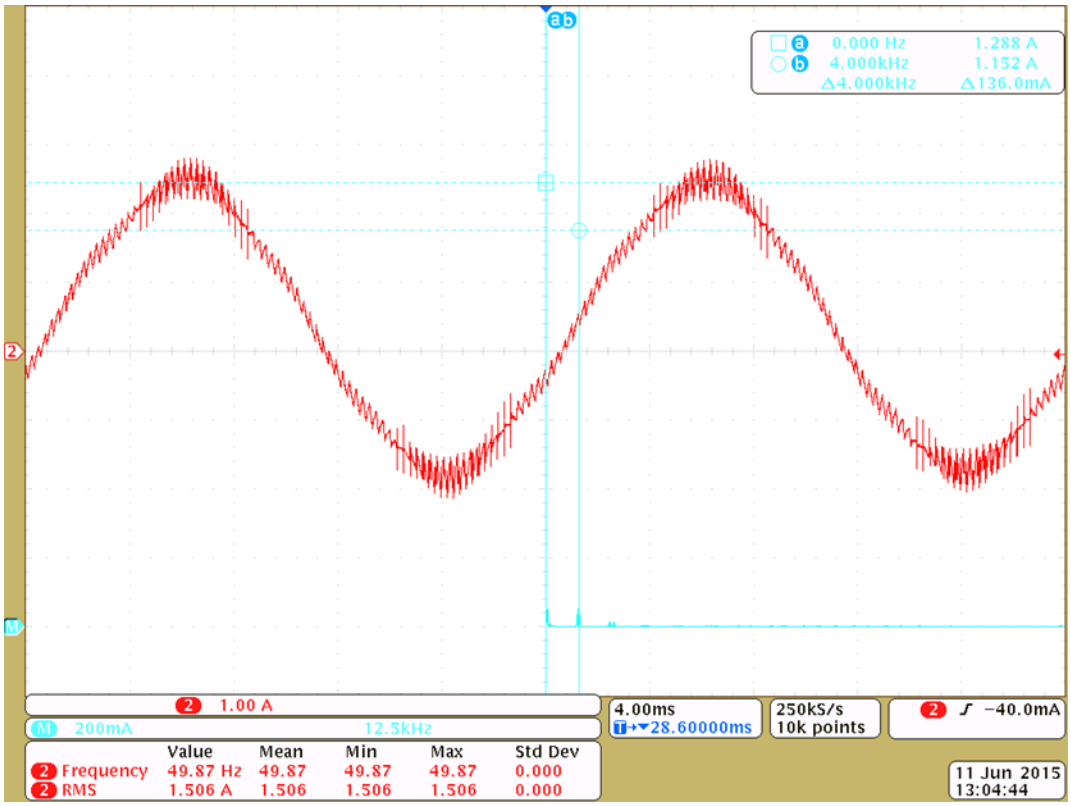


Figure 60. FFT of Motor Current Shown With Blue Graph

7.6 Overcurrent Protection Test Results

The overcurrent protection circuit is typically tested above 200% of the nominal current of the Hall effect current sensor. As Figure 5 shows, an LAH 25-NP device with an I_{NP} of 8 A can take up to 18 A of peak current. The overcurrent protection at 18 A is 225% of the nominal primary current. The TIDA-00368 reference design is tested at 18 A. The waveforms that Figure 61 and Figure 62 show indicate the sensing of overcurrent conditions at the positive threshold VTH(pos). The time required to detect the signal is 800 ns.

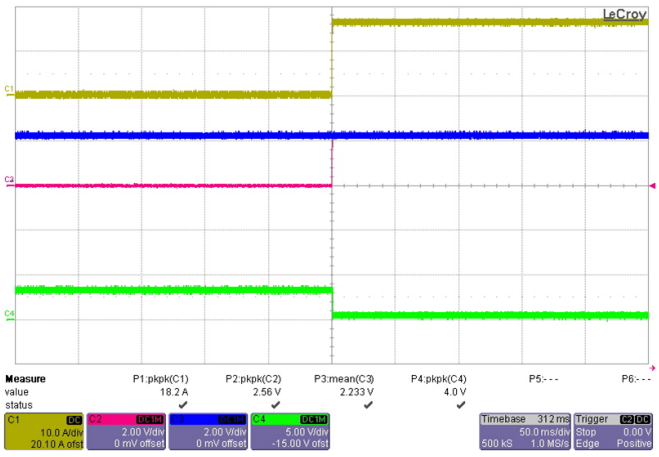


Figure 61. Overcurrent Detection at VTH (Positive)

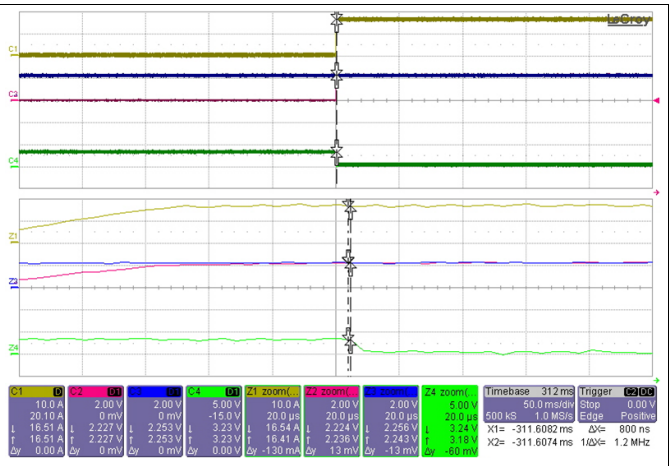


Figure 62. Overcurrent Detection at VTH (Positive)—Zoomed-In

The waveforms that Figure 63 and Figure 64 indicate the sensing of overcurrent conditions at the negative threshold VTH(neg). The time required to detect the signal is 800 ns.

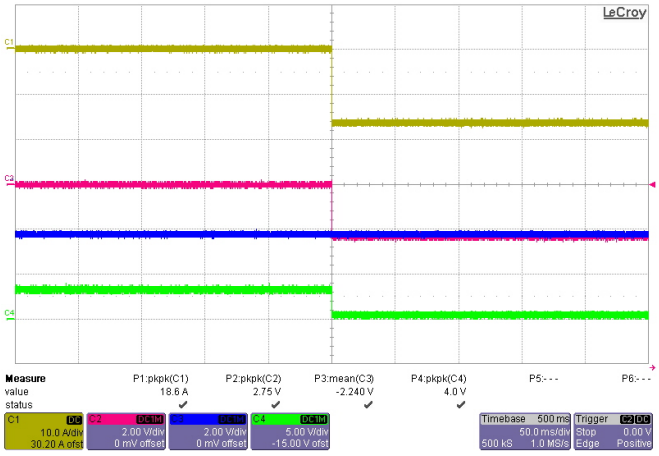


Figure 63. Overcurrent Detection at VTH (Negative)

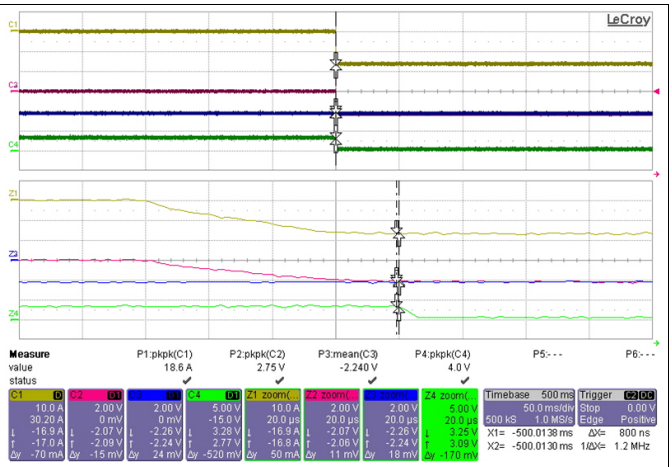


Figure 64. Overcurrent Detection at VTH (Negative)—Zoomed-In

7.7 Testing With Current Transformer (CT)

This design has an option to connect an external CT to connector J2. The burden resistor for a CT still remains same (R6) as it does for the LAH 25-NP device. The CT turns ratio = 7: 3750 and the burden resistor (R6) = 42.2 Ω.

NOTE: When testing with an external CT, the resistor R84 must be unpopulated to prevent any error in the outputs.

Table 8 shows the voltage measured at the output of the differential signal conditioning circuit.

Table 8. Test Results While Testing With CT

AC INPUT CURRENT (IN A)	OUTPUT VOLTAGE (IN V) FOR BIPOLAR SIGNAL CONDITIONING
0	0.002 mV
1	0.040149
2	0.080297
3	0.12057
4	0.16059
5	0.2008
6	0.24094
7	0.28104
8	0.32124
9	0.36136
10	0.40152
11	0.4416
12	0.48177
13	0.52184
14	0.56202
15	0.60213
16	0.64307

While the CT primary current is 16 A, Figure 65 shows the output voltage captured on the ADS8354 EVM for the differential signal conditioning circuit.

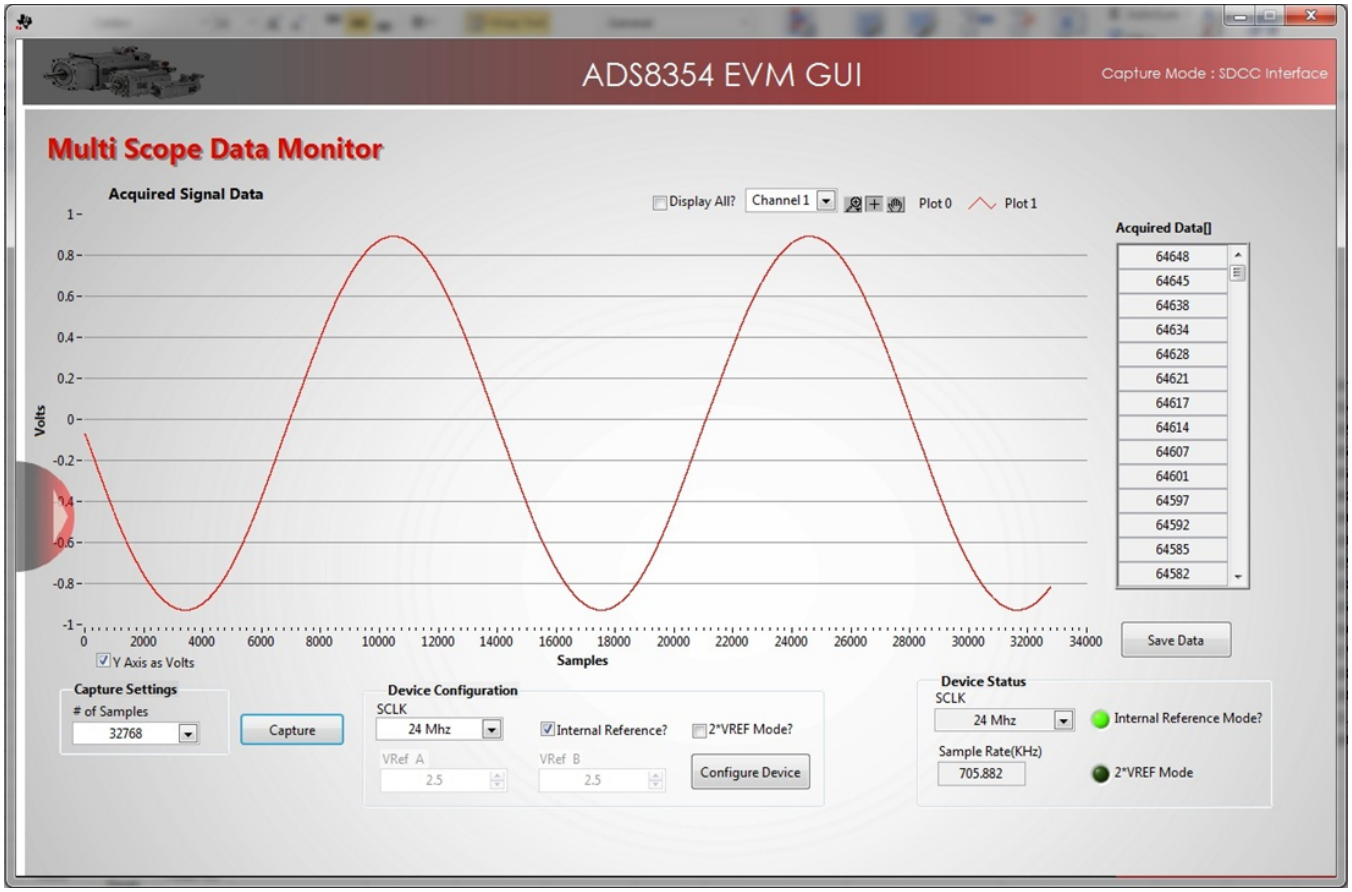


Figure 65. Output Voltage Captured While Testing With CT

8 Design Files

8.1 Schematics

To download the schematics for each board, see the design files at TIDA-00368.

8.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-00368.

8.3 PCB Layout Recommendations

To download the layout prints for each board, see the design files at TIDA-00368.

8.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00368.

8.5 Layout Guidelines

Note that the total dimension of the board is 112 mm x 85 mm. The following subsections provide a few guidelines and examples for the layout of the devices used in the design.

8.5.1 Layout of Differential Signal Chain

Figure 66 shows the layout of the differential signal conditioning circuit (using the OPA322 and THS4531A devices) on the TIDA-00368 board.

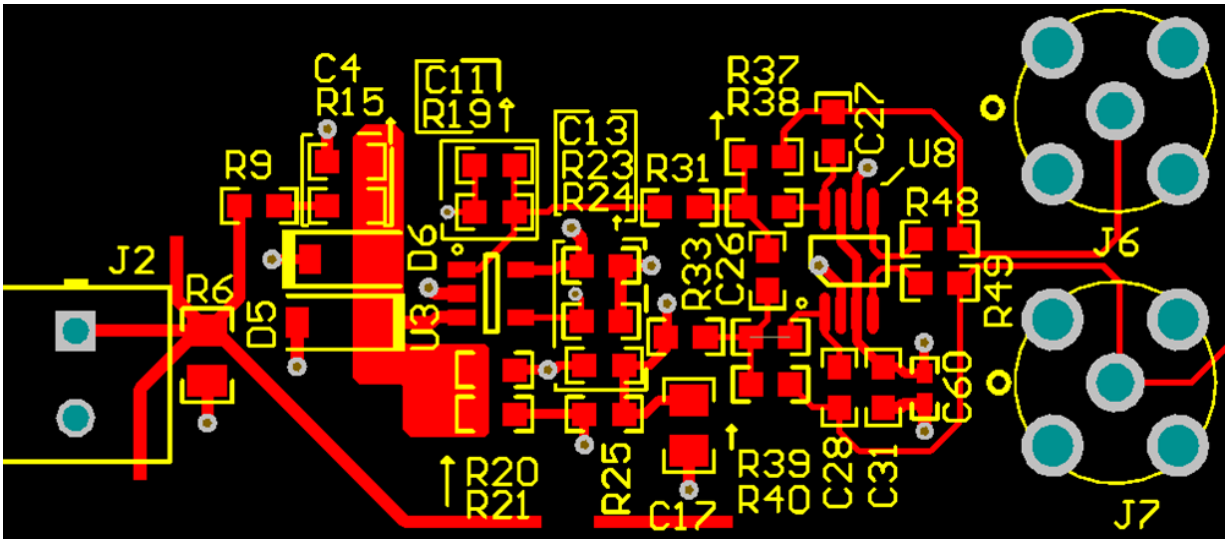


Figure 66. Layout of Bipolar Signal Conditioning Circuit

The datasheet of THS4531A provides a few guidelines for the layout of the external components near the amplifier, ground plane construction, and power routing. The general guidelines are:

1. The signal routing must be direct and as short as possible into and out of the op-amp.
2. The feedback path must be short and direct avoiding vias if possible.
3. The ground or power planes must be removed from directly under the amplifier's input and output pins.
4. TI recommends placing a series output resistor as near to the output pin as possible.
5. A power supply decoupling capacitor should be placed within 2 in of the device and can be shared with other op-amps. For a split supply, a capacitor is required for both supplies.
6. Place a 0.1-µF power supply decoupling capacitor as near to the power supply pins as possible, preferably within 0.1 of an inch. For a split supply, a capacitor is required for both supplies.

The PD pin uses transistor-transistor logic (TTL) levels referenced to the negative supply voltage (VS−). When not used, the PD pin must tie to the positive supply to enable the amplifier. When used, the PD pin must be actively driven high or low and must not be left in an indeterminate logic state. A bypass capacitor is not required, but can be used for robustness in noisy environments.

As per the recommendations, the ground and power planes are cut below the input and output pins of the THS4531A device, as Figure 67 shows.

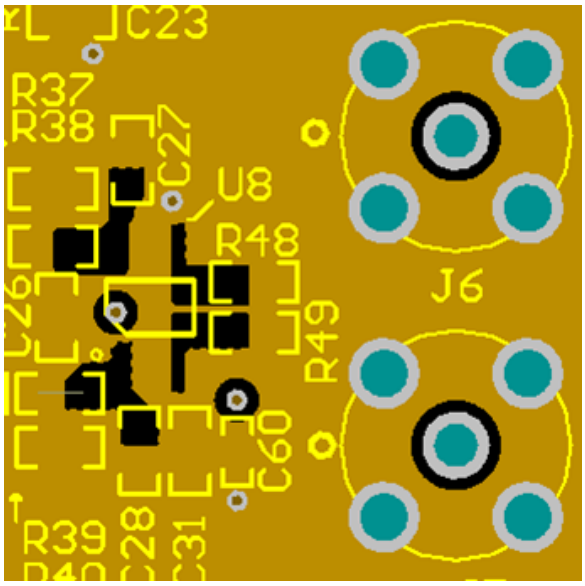


Figure 67. Cut Planes Below THS4531A Input and Output Pins

8.5.2 Layout of TPS7A4901 and TPS7A3001

The TPS7A4901 family of positive, high-voltage linear regulators achieves stability with a minimum input and output capacitance of 2.2 µF; however, TI highly recommends using a 10-µF capacitor to maximize the AC performance. The input and output capacitors must be placed as close to the pin as possible, on the same side as the IC. Do not use vias between the capacitor and the pin.

The following list shows what to do and what to avoid when choosing the layout for the TPS7A4901 device:

1. Place at least one, low-equivalent-series-resistance (ESR), 2.2-µF capacitor as close as possible to both the IN and OUT terminals of the regulator to the GND pin.
2. Provide adequate thermal paths away from the device.
3. Do not place the input or output capacitor more than 10 mm away from the regulator.
4. Do not exceed the absolute maximum ratings.
5. Do not float the enable (EN) pin.
6. Do not resistively or inductively load the NR or SS pin.

The layout is a critical part of a good power-supply design. Several signal paths conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin must be bypassed to ground with a low-ESR ceramic bypass capacitor. The GND pin must be tied directly to the PowerPAD™ integrated circuit package from Texas Instruments and under the IC. The PowerPAD must be connected to any internal PCB ground planes using multiple vias directly under the IC. Every capacitor (C_{IN}, C_{OUT}, $C_{NR/SS}$, and C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself. Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively, and even cause instability. Figure 68 shows the layout of TPS7A4901 and TPS7A3001 done on TIDA-00368 Board.

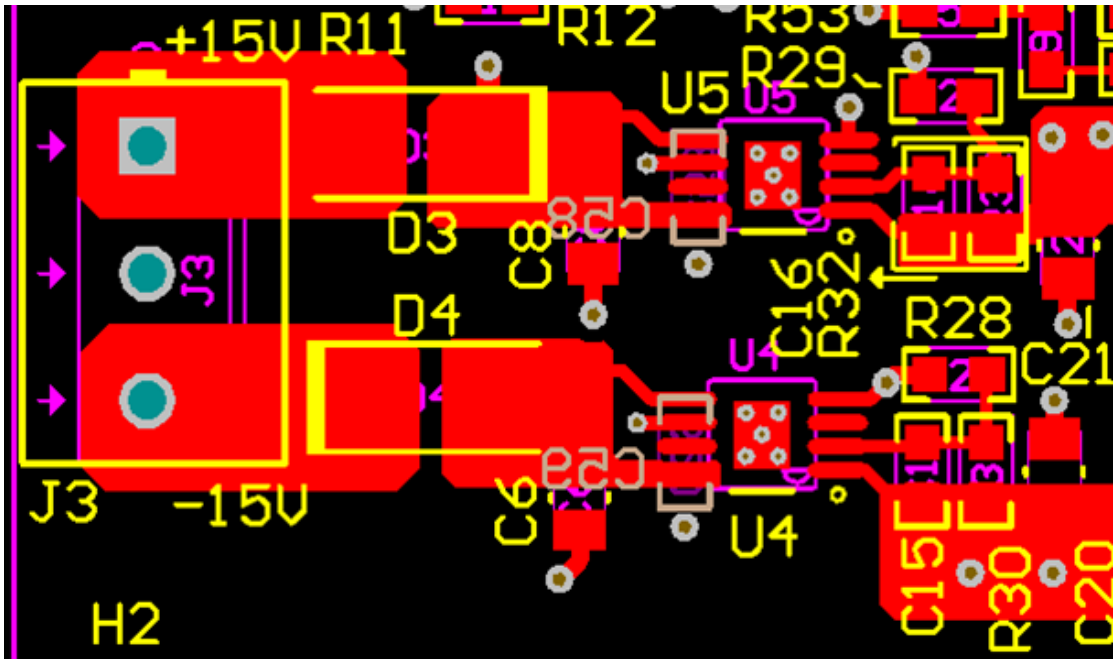


Figure 68. Layout of TPS7A4901 and TPS7A3001

8.5.3 Layout for TPS62150

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS62150 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased electromagnetic interference (EMI) radiation and noise sensitivity.

Both AGND and PGND pins are directly connected to the Exposed Thermal Pad. On the PCB, the direct common ground connection of AGND and PGND to the Exposed Thermal Pad and the system ground (ground plane) is mandatory. Also connect the VOS pin in the shortest way to VOUT at the output capacitor. Provide low inductive and resistive paths for loops with high di/dt. Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated. Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (for example SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin and on AVIN as well as the FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the system ground plane. The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

Figure 69 shows the layout of the TPS62150 device on the TIDA-00368 board.

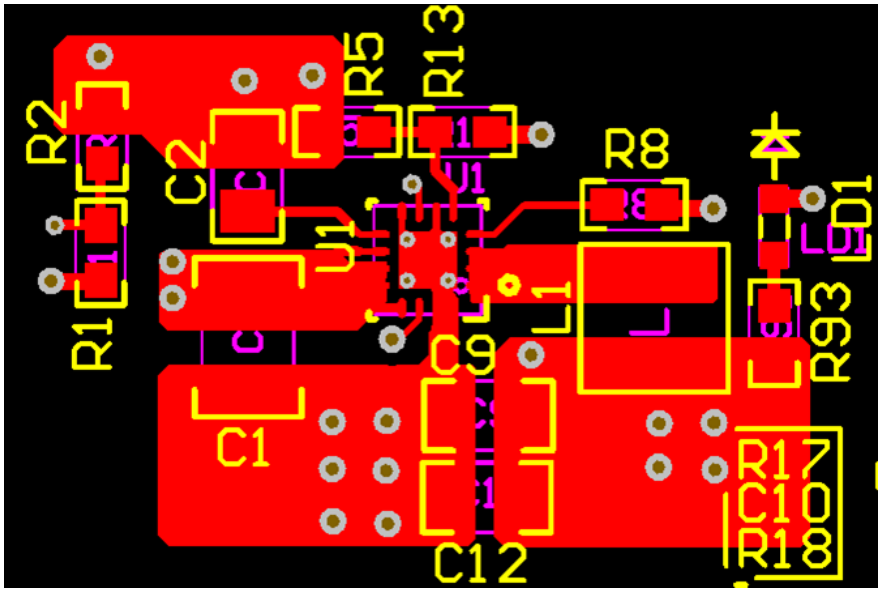


Figure 69. Layout of TPS62150

8.5.4 Layout of REF2025

Some key considerations for the layout of the REF2025 reference are:

1. Connect low-ESR, 0.1-µF ceramic bypass capacitors at the VIN, VREF, and VBIAS of the REF20XX reference.
2. Decouple other active devices in the system per the device specifications.
3. Using a solid ground plane helps distribute heat and reduces EMI noise pickup.
4. Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
5. Minimize the trace length between the reference and bias connections to the INA and ADC devices to reduce noise pickup.
6. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

Figure 70 shows the layout of the REF2025 reference on the TIDA-00368 board.

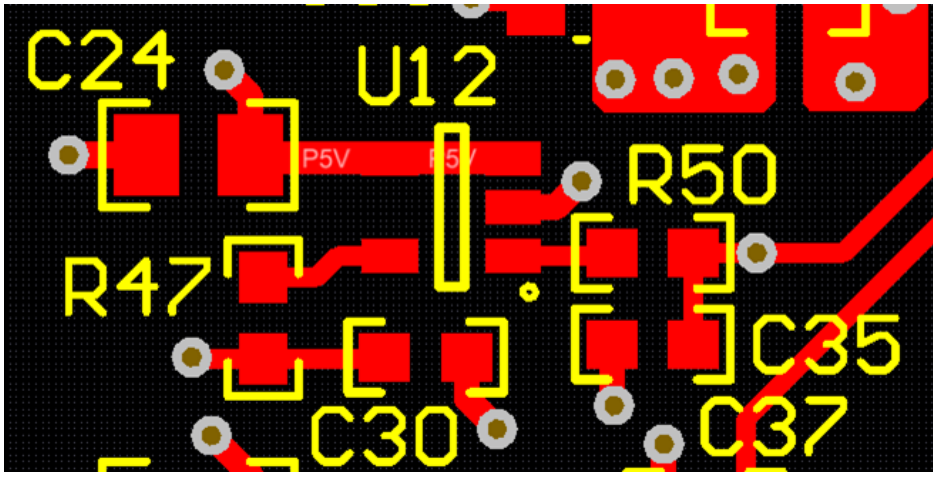


Figure 70. Layout of Voltage Reference eDevice

8.5.5 Layout of Anti-Aliasing Filters for Control Card

The anti-aliasing filters for ADC inputs are not available on the Delfino Control Card. Therefore, they are provided on the TIDA-00368 PCB. Figure 71 shows these filters:

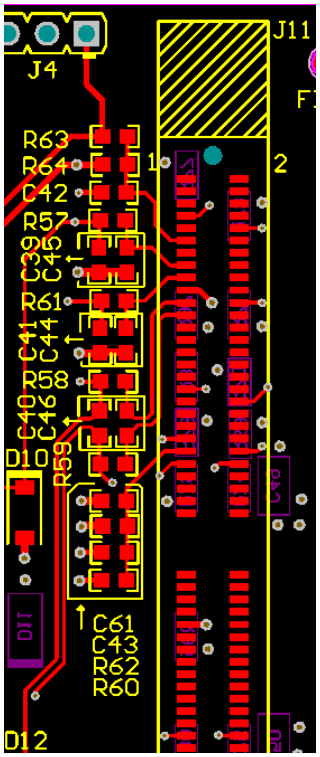


Figure 71. Layout Capture for ADC Inputs (and Filter Components) for Delfino Control Card

8.5.6 Layout of Sensor LAH 25-NP

Figure 72 shows the layout of the LAH 25-NP sensor. An important thing to note is that the traces through which the current passes are thick.

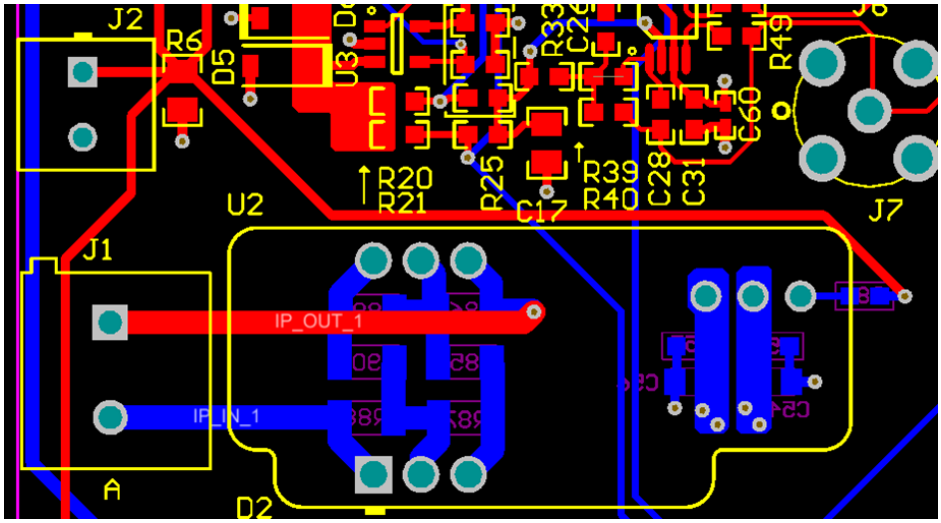


Figure 72. Sensor Circuit

The current (measured in the motor drive) can have higher voltages that require special isolation and spacings on the board. Figure 73 and Figure 74 show that there is no ground plane or power plane placed below the sensor as well as the input connector.

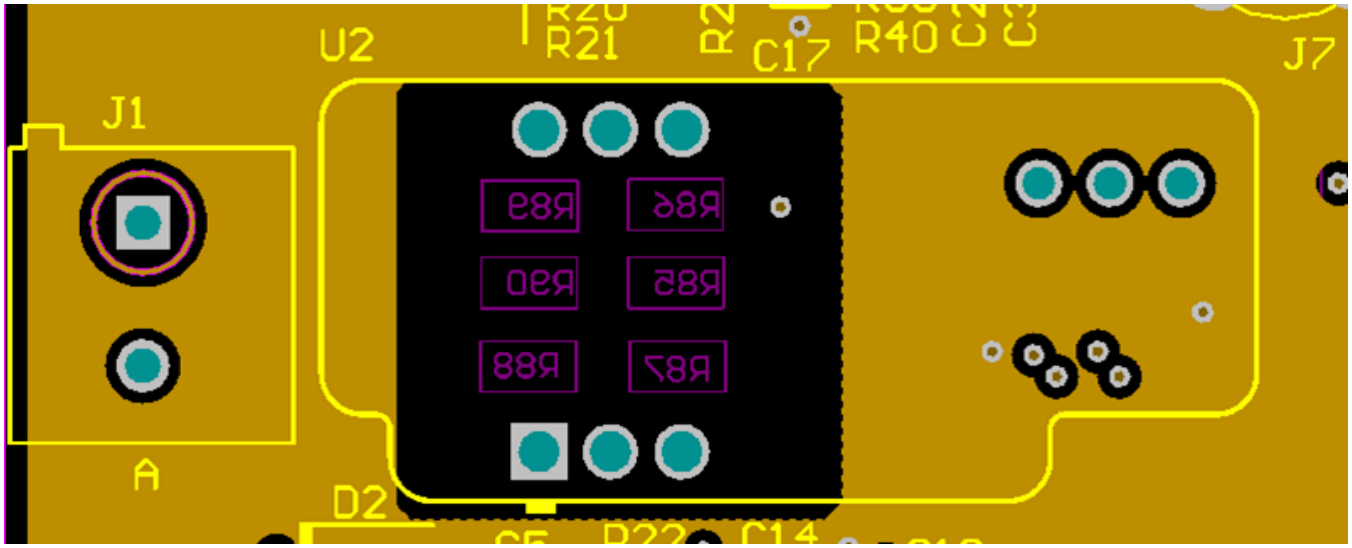


Figure 73. Cut in Ground Plane for Isolation to High-Voltage Sections

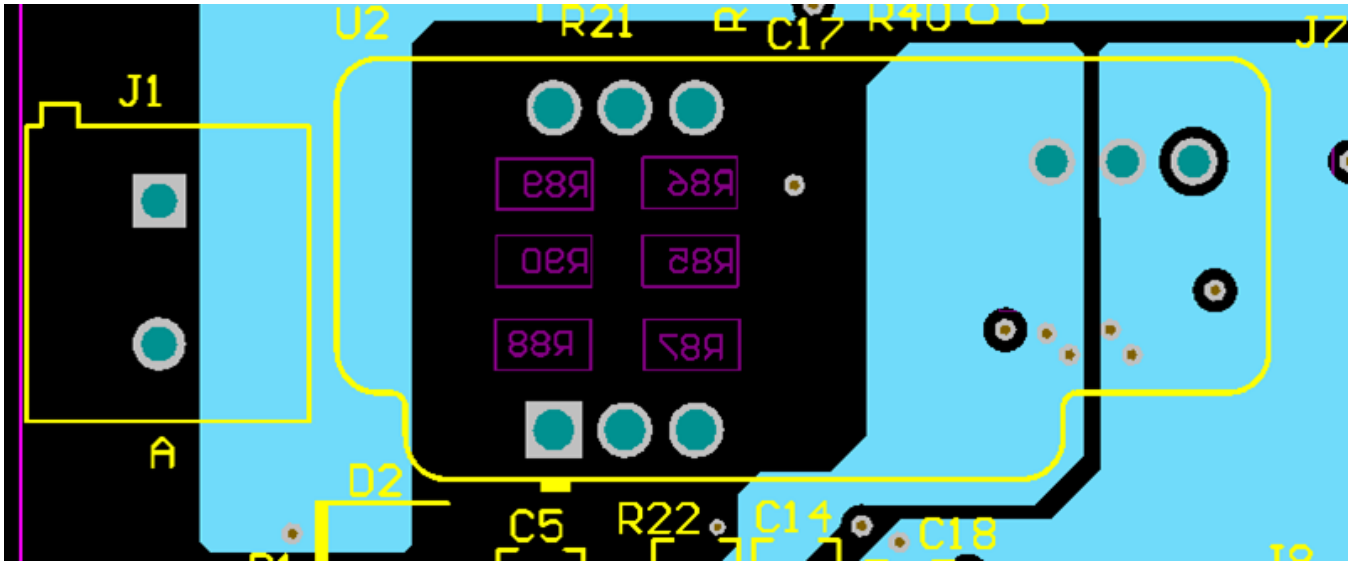


Figure 74. Cut in Power Plane for Isolation to High-Voltage Sections

8.5.7 Ground Plane and Power Planes

Figure 75 shows the power plane for the TIDA-00368 PCB.

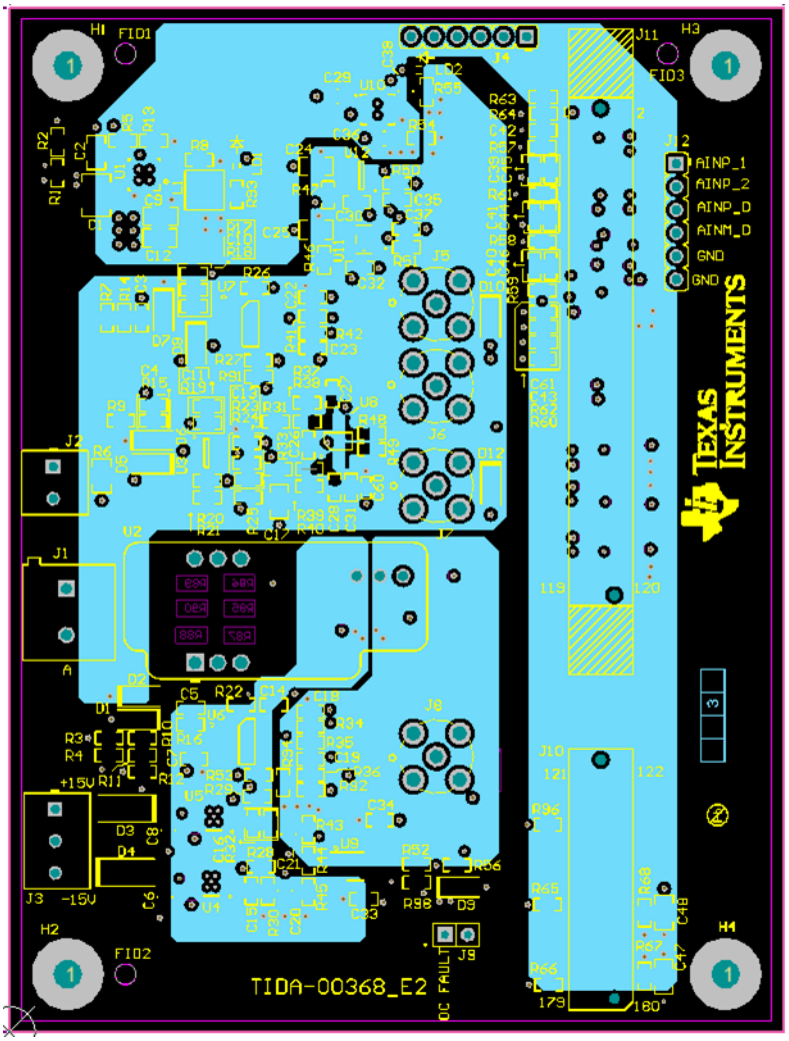


Figure 75. Power Planes

Figure 76 shows the ground plane for the TIDA-00368 PCB.

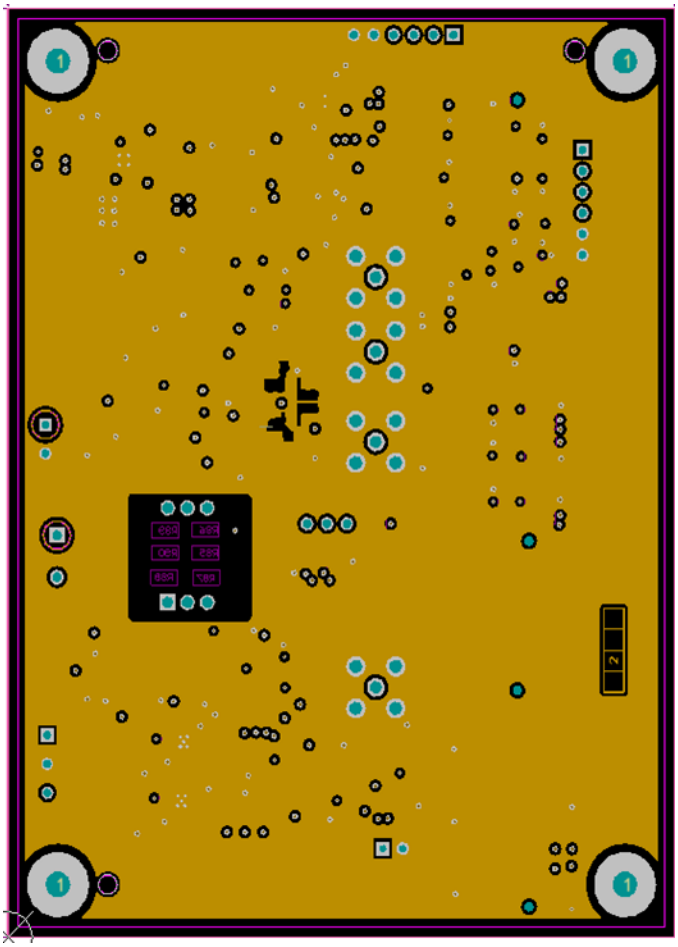


Figure 76. Ground Plane

8.6 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00368.

9 References

1. Texas Instruments, *FilterPro*™, FilterPro™ User's Guide (SBFA001)
2. Texas Instruments, *FilterPro Active Filter Design Application (NRND)*, FilterPro™ v3.1 Software Description http://www.ti.com/lsds/ti/analog/webench/webench-filters.page#active-filter
3. LEM Technologies, *Closed Loop transducers with small footprint up to 100 A nominal* , Technical Information http://www.lem.com/hq/en/content/view/261/200/
4. Prosser, Stephen J.; Schmidt, Ernest D.D.; *Smart sensors for industrial applications*, Microelectronics International, Vol. 16 Iss: 2 (1999), pp.20 - 23

10 Acknowledgment

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