Test Data
For PMP9419
07/24/2014

Power Specification

Specs:

Vout:

+15V port: 14.8V to 16V @ 7mA to 107mA;

-15V port: -15.55V to -18V @ 7mA to 30mA;

+5V port: 4.51V to 5V @ 5mA to 17mA;

Nominal Vin = 24V

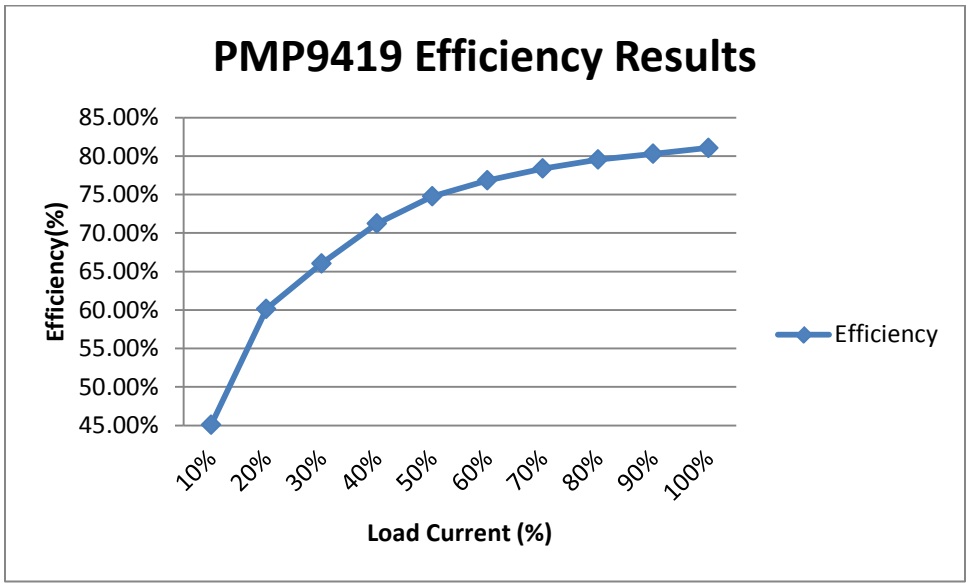
Fsw = 450kHz

Board Photo

Efficiency

	Vin(V)	Iin(mA)	Vosec(+15V)	Iosec(mA)	Vosec(-15V)	Iosec(mA)	Vosec(5V)	Iosec(mA)	Efficiency(%)
0%	24.13	13.3	15.574	0	-16.698	0	4.955	0	
10%	24.12	23	15.498	11.3	-16.618	3.8	4.9288	2.4	45.08%
20%	24.12	33.9	15.45	23.4	-16.576	6.7	4.9113	3.9	60.14%
30%	24.12	42.8	15.418	32.1	-16.546	9.7	4.9	5.4	66.05%
40%	24.12	52.5	15.38	42.7	-16.535	12.8	4.89	6.9	71.24%
50%	24.12	62.3	15.348	53.4	-16.535	15.9	4.8813	8.4	74.77%
60%	24.12	72.2	15.316	63.8	-16.54	18.9	4.8775	9.9	76.84%
70%	24.12	82.2	15.29	74.3	-16.548	21.9	4.8738	11.4	78.38%
80%	24.12	93.6	15.256	86.3	-16.559	24.7	4.86663	14.4	79.54%
90%	24.12	103.4	15.23	96.8	-16.563	27.2	4.8613	16	80.29%
100%	24.12	113.7	15.198	107.4	-16.556	30.6	4.8538	17.4	81.07%

Note that there're 2kohm at each of the outputs to maintain some load current (2.5mA – 7.4mA).



Cross Line Regulation

Vosec(+15V) port fulfills 14.8V – 16V.

Vin = 24V	Vosec(+15)	Iosec(mA)	Vosec(-15)	Iosec(mA)	Vosec(5V)	Iosec(mA)	cross line regulation
	15.533	7	-16.594	7	4.9063	5	0.54%
	15.541	7	-16.425	30	4.8975	5	0.59%
	15.524	7	-16.579	7	4.86	17	0.48%
	15.536	7	-16.42	30	4.8538	17	0.56%
	15.369	107	-16.638	7	4.8975	5	-0.52%
	15.389	107	-16.54	30	4.9	5	-0.39%
	15.366	107	-16.643	7	4.8513	17	-0.54%
	15.385	107	-16.543	30	4.8538	17	-0.42%

Vosec(5V) port fulfills 4.51V – 5V.

Vin = 24V	Vosec(5V)	Iosec(mA)	Voosec(-15)	Iosec(mA)	Vosec(15)	Iosec(mA)	cross line regulation
	4.9063	5	-16.594	7	15.533	7	0.13%
	4.8975	5	-16.425	30	15.541	7	-0.05%
	4.8975	5	-16.638	7	15.369	107	-0.05%
	4.9	5	-16.54	30	15.389	107	0.00%
	4.86	17	-16.579	7	15.524	7	-0.82%
	4.8538	17	-16.42	30	15.536	7	-0.94%
	4.8513	17	-16.643	7	15.366	107	-0.99%
	4.8538	17	-16.543	30	15.385	107	-0.94%

Vosec(-15V) port fulfills -18V ~ -15.5V.

	Vosec(-15)	Iosec(mA)	Vosec(15)	Iosec(mA)	Vosec(5V)	Iosec(mA)	cross line regulation
Vin = 24V	-16.594	7	15.533	7	4.9063	5	0.57%
	-16.638	7	15.369	107	4.8975	5	0.84%
	-16.579	7	15.524	7	4.86	17	0.48%
	-16.643	7	15.366	107	4.8513	17	0.87%
	-16.425	30	15.541	7	4.8975	5	-0.45%
	-16.638	30	15.369	107	4.8975	5	0.84%
	-16.42	30	15.536	7	4.8538	17	-0.48%

	-16.543	30	15.385	107	4.8538	17	0.26%

Note that for each of the Vosec outputs, we put 2kohm to remain some load (2.5mA – 7.5mA).

The formula for calculating the numbers in the cross line regulation column is:

Cross Line Regulation (+15V) = (Vosec(+15V)-15V)/15V * 100%;

Corss Line Regulation (+5V) = (Vosec(+5V) – 5V) / 5V * 100%;

Cross Line Regulation (-16V) = (Vosec(-16V)-16.5V)/(-16.5V) * 100%;

Start-up vs. Shut-down

Note that the input voltage is 24V. and when the current in the waveform is with some value, it means all the Vosec outputs are at full load. Vo(+15V)@107mA, Vo(-16V)@30mA, Vo(+5V)@17mA; When the current in the waveform is 0, it means all the outputs are at no load.

Also, all the Vosec outputs doesn't exceed their maximum voltage during start up or shut down, but as a matter of fact, oscilloscope doesn't give 100% accuracy of what the voltage level really is. After being tested by voltmeter, the actual voltage level is 0.25V – 0.5V lower than the number shown in the waveform, which gives a safer margin compared to the voltage range spec.

Note that there's no particular reason to measure the time delay between the ramping up of Vin and Vo(added on Aug, 27th, 2014)

Vosec(+15V)

Test condition: The input voltage was set at 24V, and all outputs were set at full load.

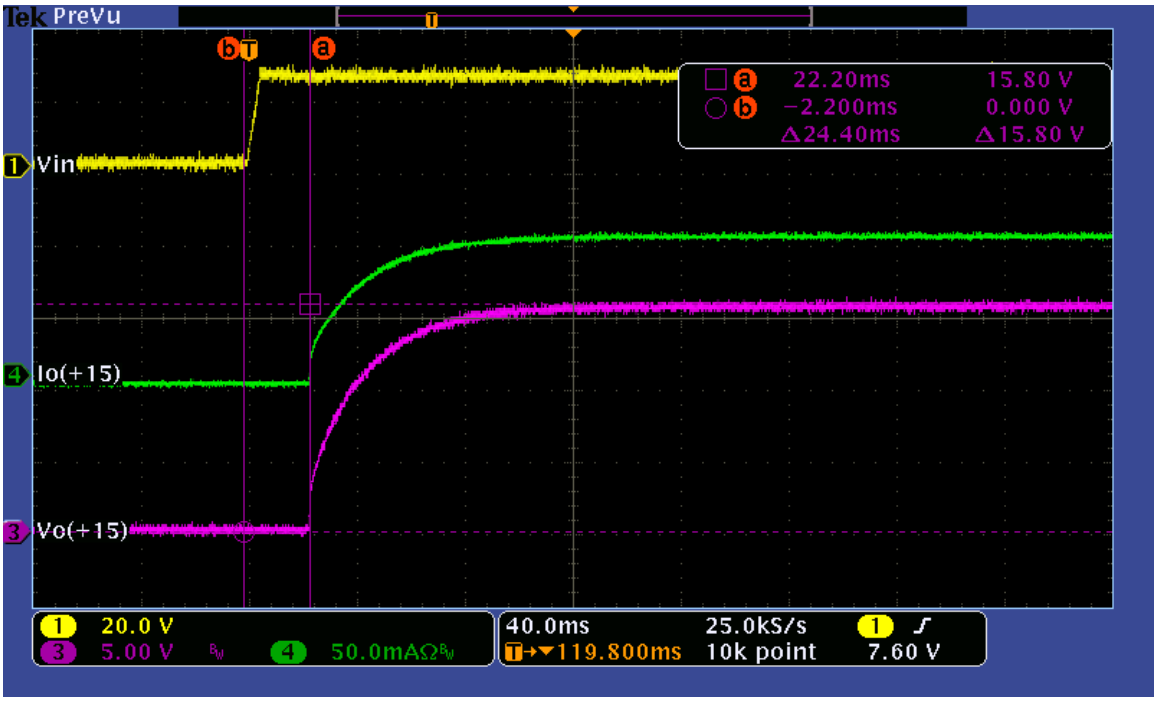


Fig. Start-up

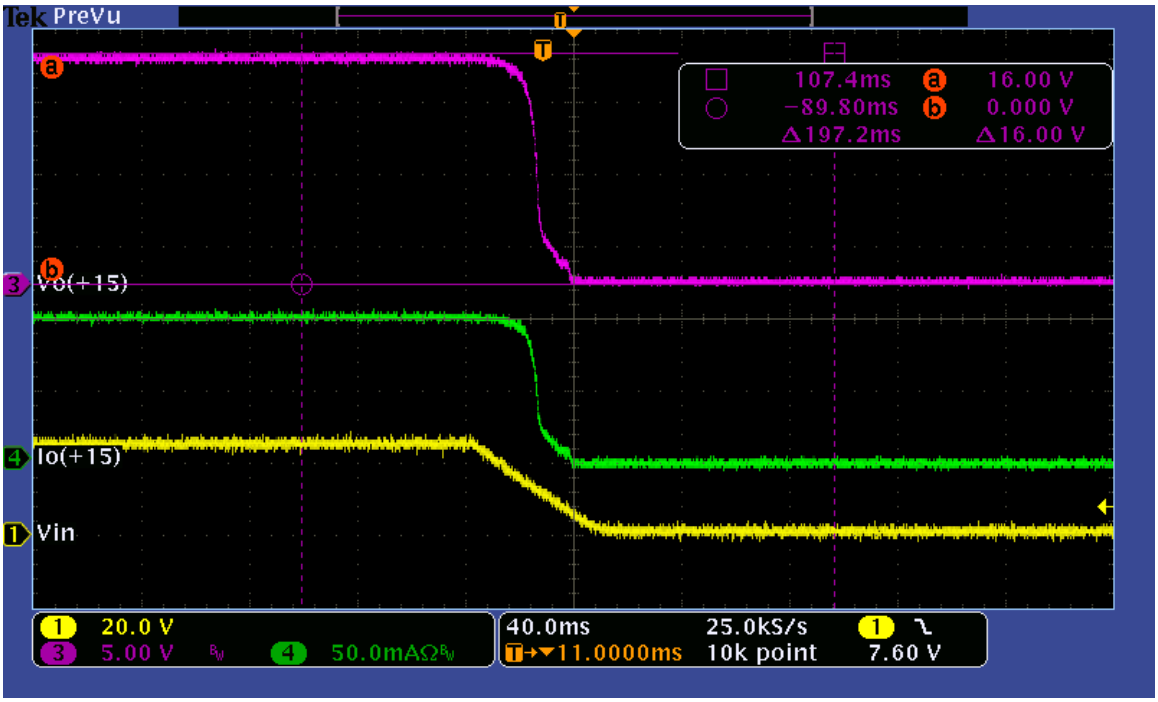


Fig. Shut-down

Test condition: The input voltage was set at 24V, and all outputs were set at no load.

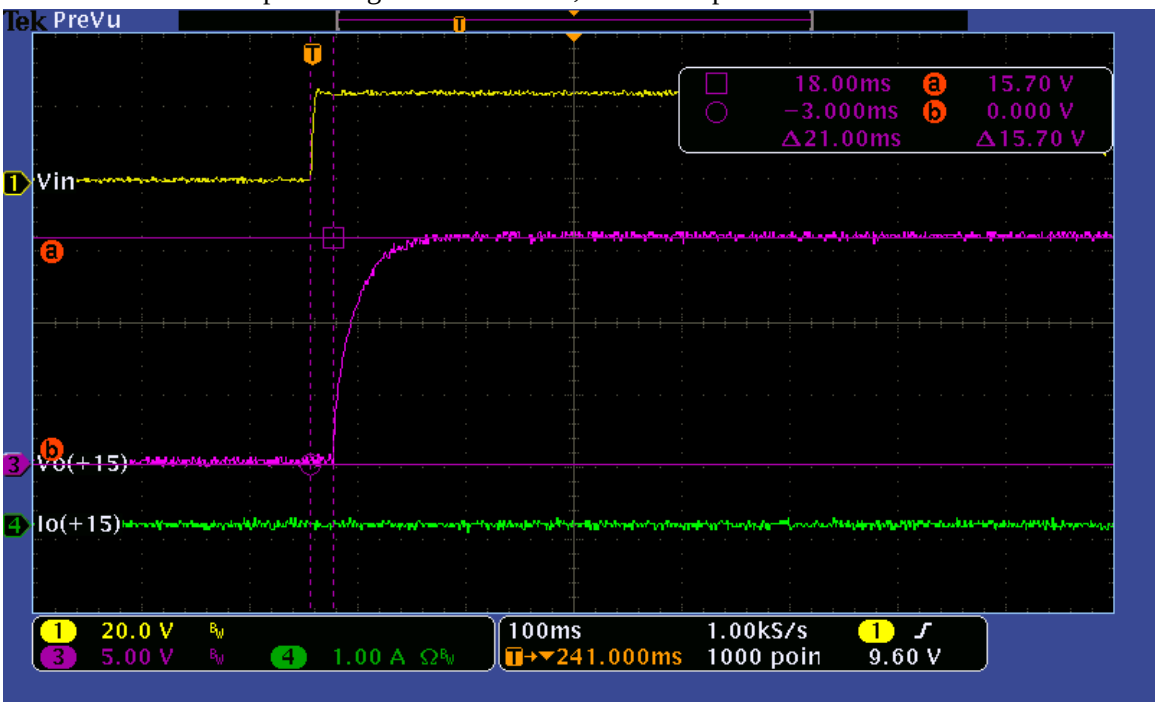


Fig. Start-up

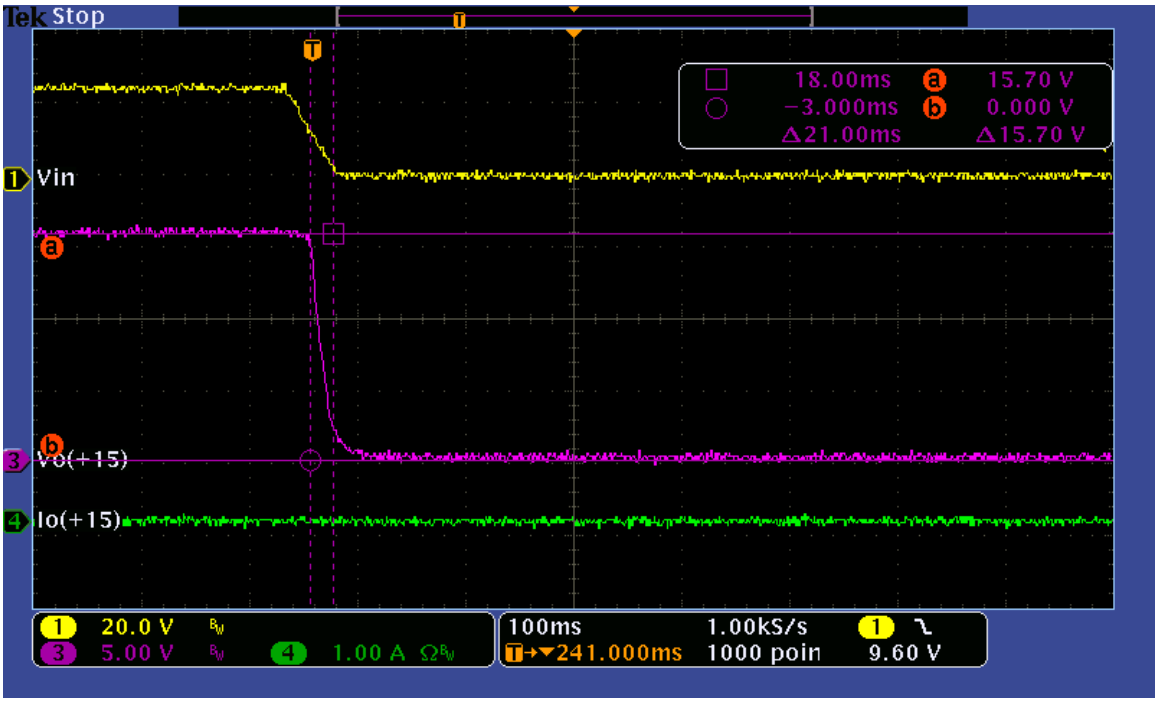


Fig. Shut-down

Note that Vo(+15V) range is 14.8V – 16V, as we can see from the waveform, the Vo(+15V) doesn't exceed its maximum allowed voltage, which is 16V, but as a matter of fact, oscilloscope doesn't present 100% accuracy of what the voltage level really is. The actual voltage of Vo(+15V) for this case is 15.53V.

Vosec(-16V)

Test condition: The input voltage was set at 24V, and all outputs were set at full load.

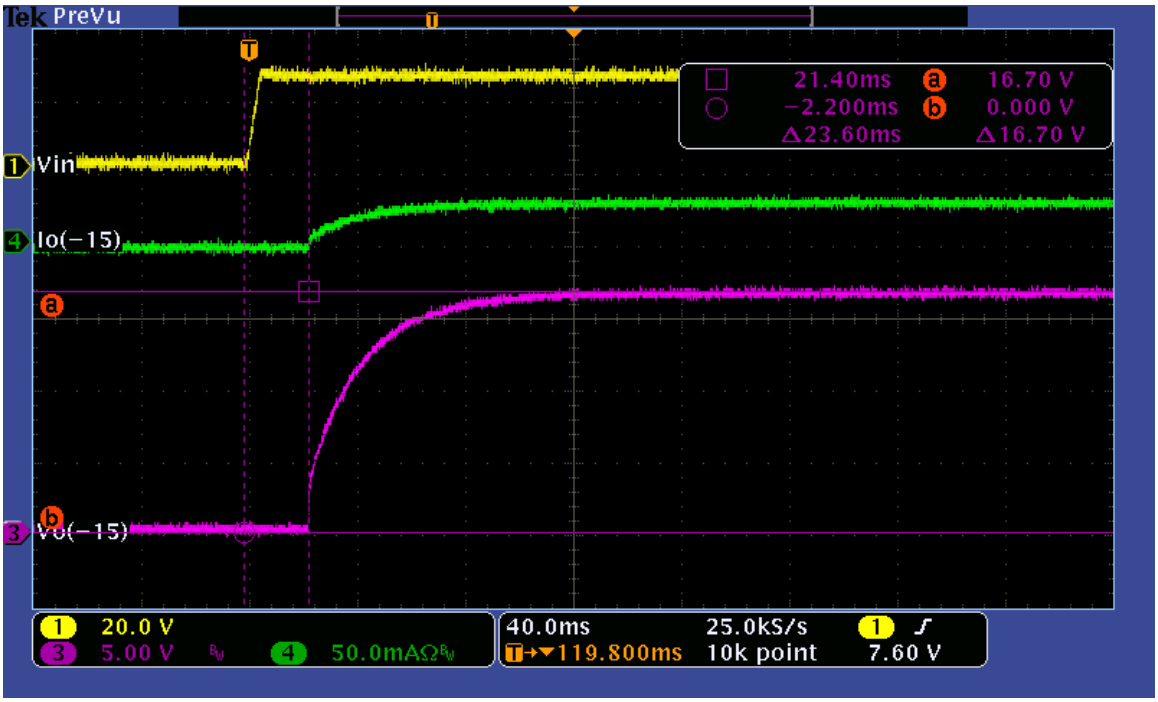


Fig. Start-up

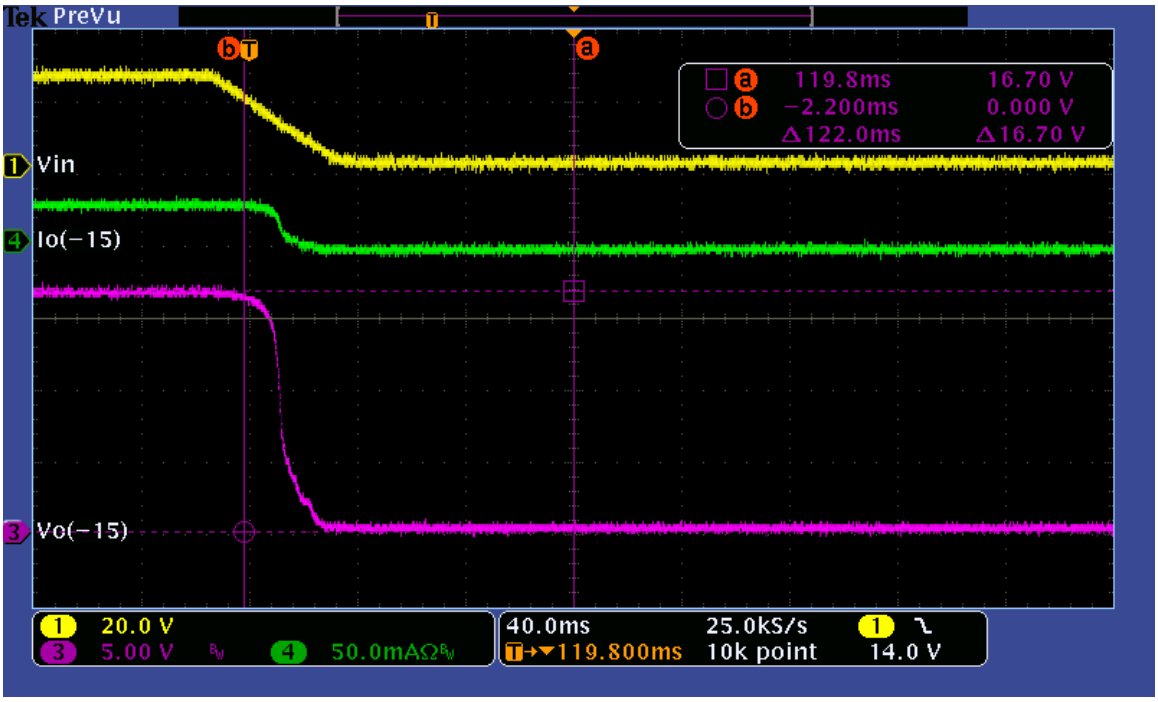


Fig. Shut-down

Test condition: The input voltage was set at 24V, and all outputs were set at no load.

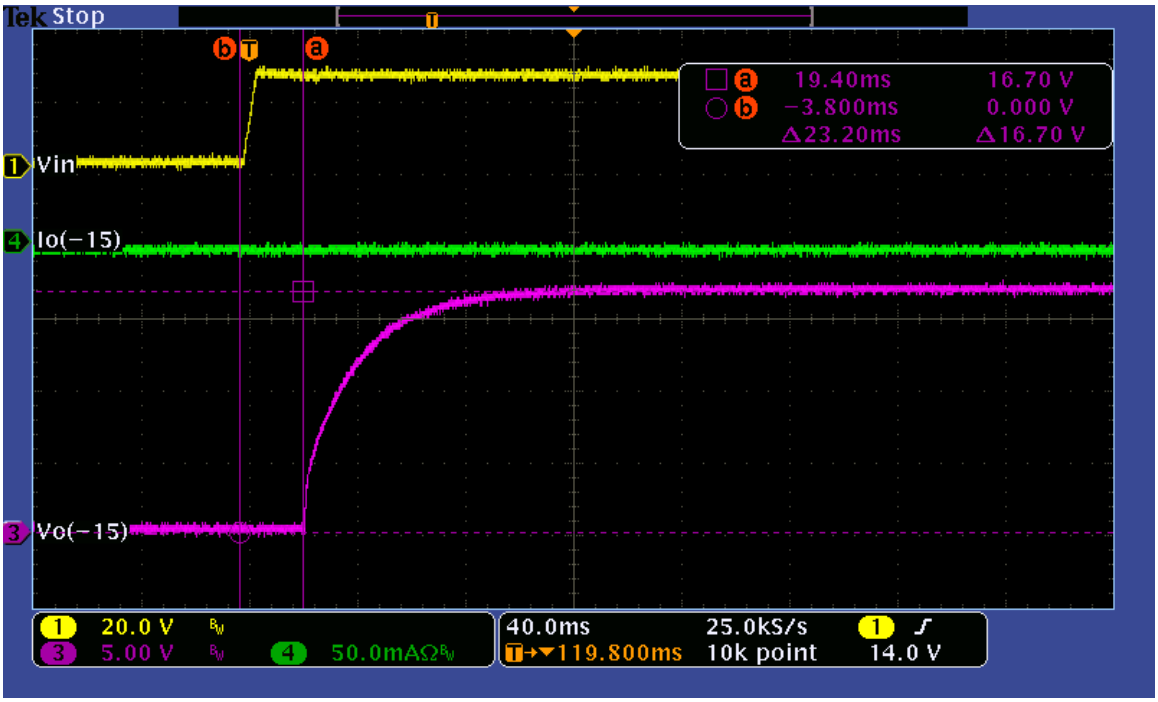


Fig. Start-up

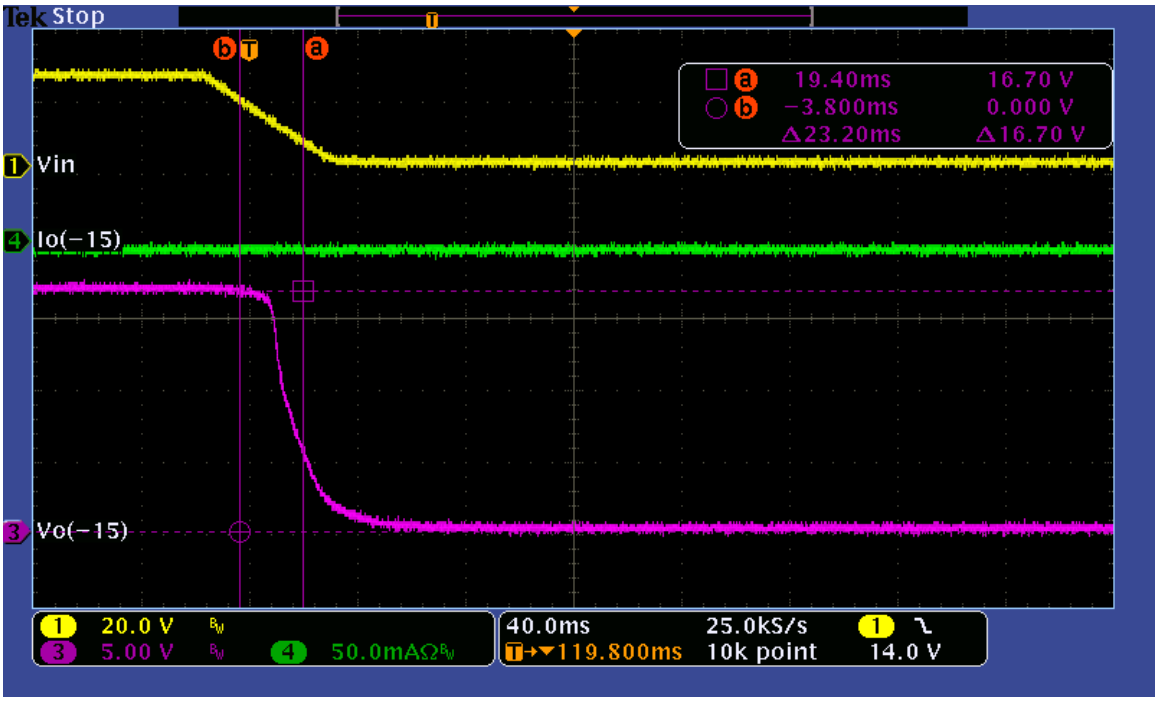


Fig. Shut-down

Vosec(+5V)

Test condition: The input voltage was set at 24V, and all outputs were set at full load.

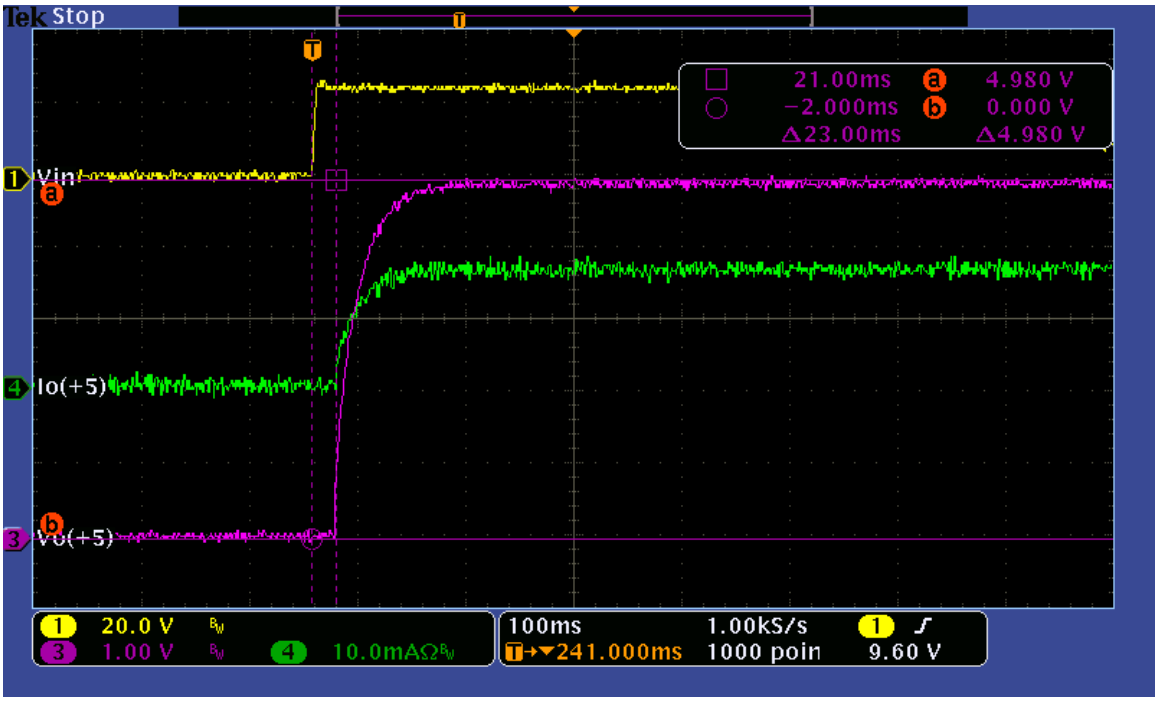


Fig. Start-up

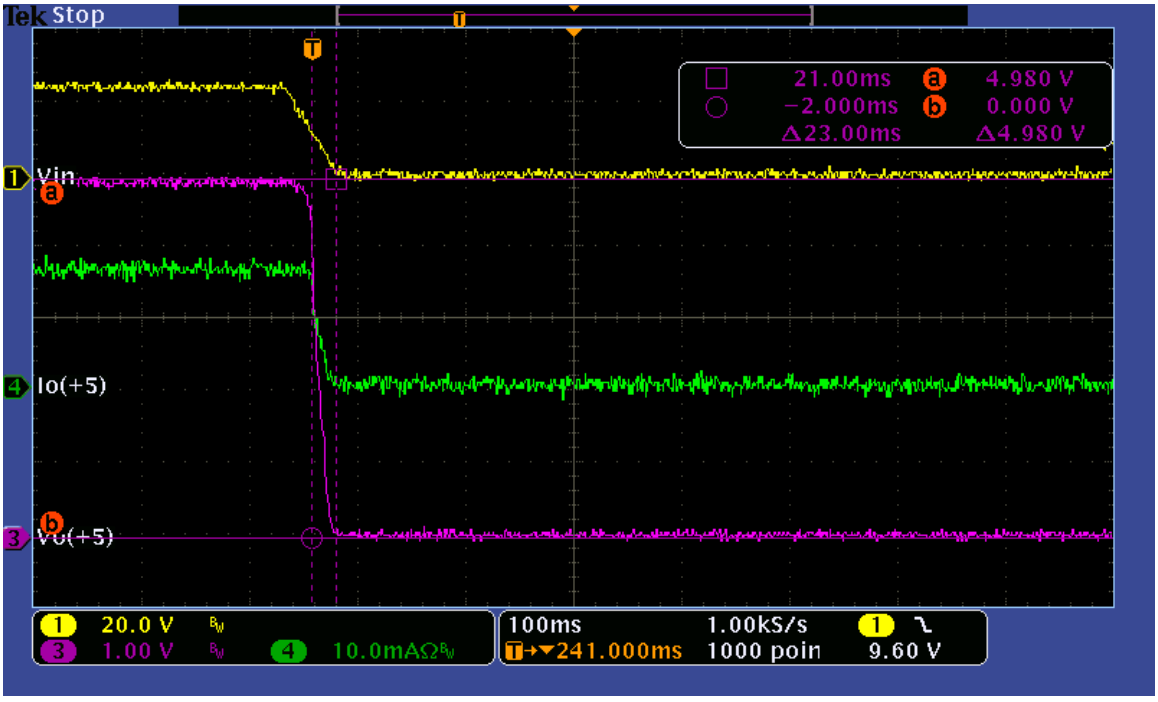


Fig. Shut-down

Test condition: The input voltage was set at 24V, and all outputs were set at no load.

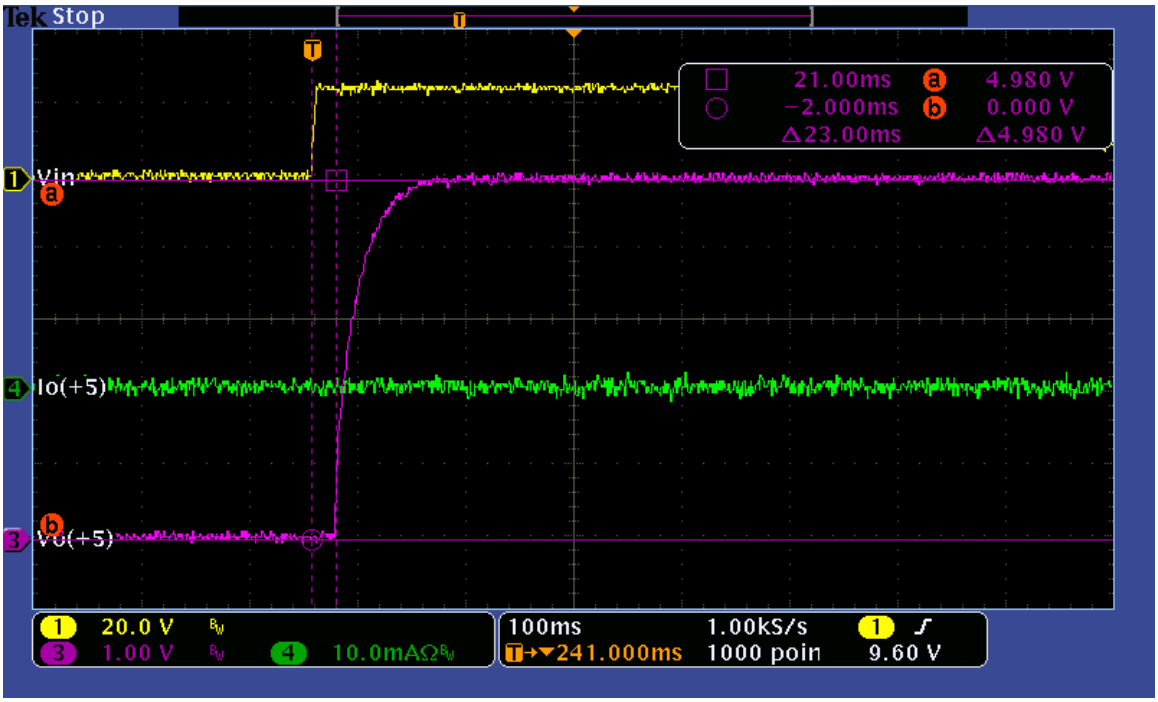


Fig. Start-up

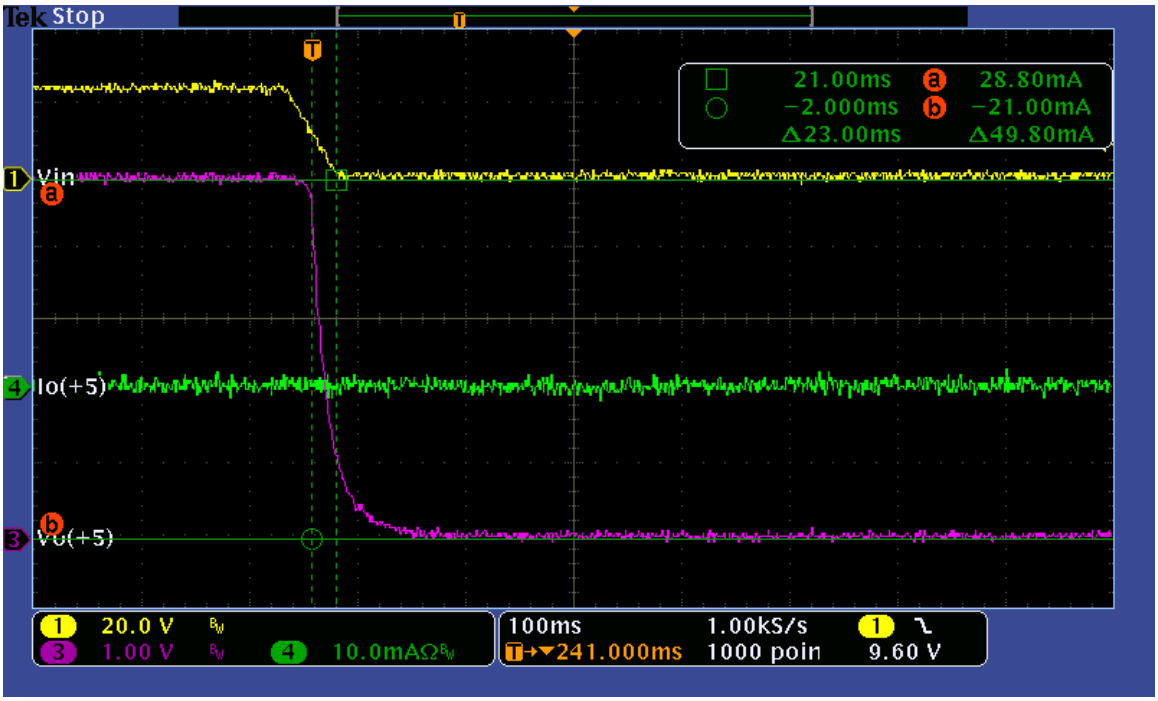
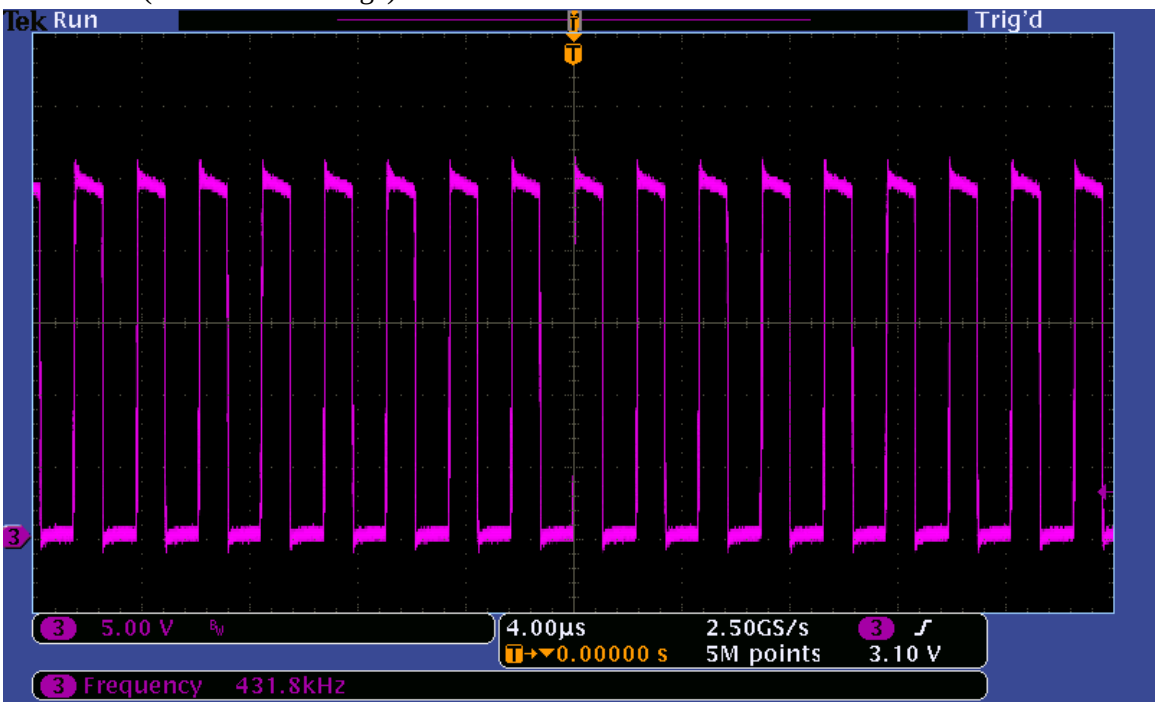


Fig. Shut-down

Note that Vo(+5V) range is 4.5V – 5V, as we can see from the waveform, the Vo(+5V) doesn't exceed its maximum allowed voltage, which is 5V, but as a matter of fact, oscilloscope doesn't present 100% accuracy of what the voltage level really is. The actual voltage of Vo(5V) for this case is 4.75V.

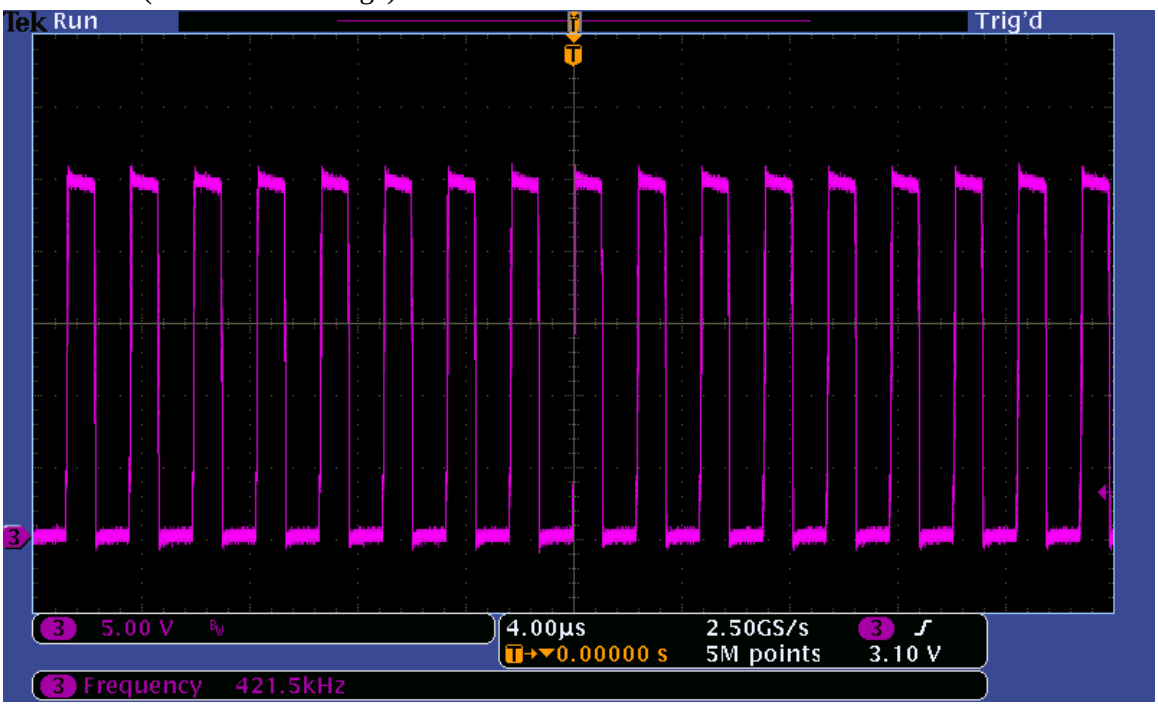
Switching Waveforms

1. Test condition: The input voltage was set at 24V, and all three outputs were set at full load.
   Ch3 – Vsw (switch node voltage)



2. Test condition: The input voltage was set at 24V, and all three outputs were set at no load.

Ch3 – Vsw (switch node voltage)



Load Transients

Vosec(+15V) Output Load Step

Test condition: Vin = 24V, Vosec(+15V) load from53mA to 107mA, full load on other Vosec outputs.

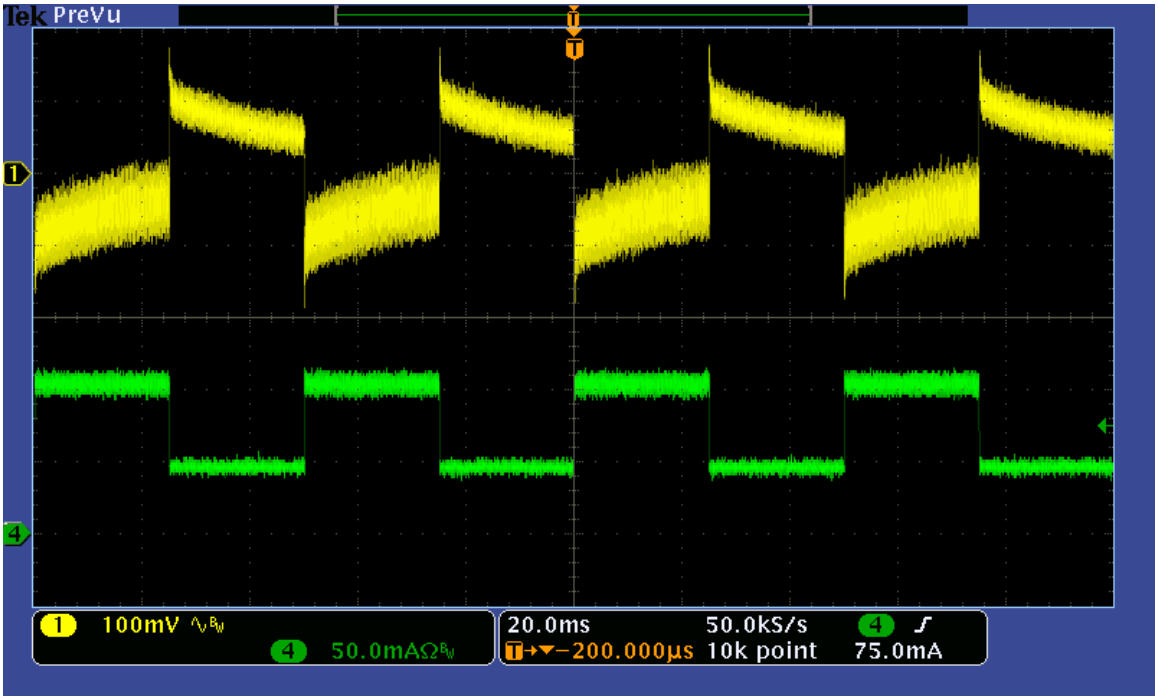


Fig Vosec(+15V)(AC)(yellow, channel1) and Iosec(+15V)(green, channel4)

Vosec(-16V) Output Load Step

Test condition: Vin = 24V, Vosec(-16V) load from 15mA to 30mA, full load on other Vosec outputs.

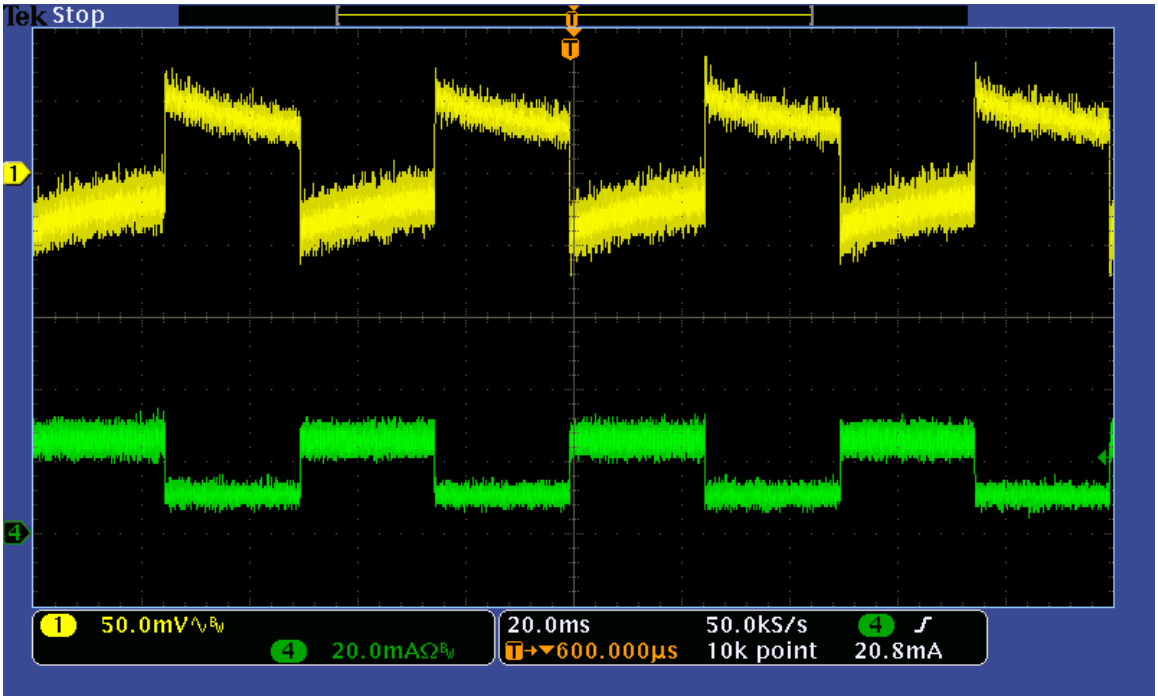


Fig Vosec(-16V)(AC)(yellow, channel1) and Iosec(-16V)(green, channel4)

Vosec(+5V) Output Load Step

Test condition: Vin = 24V, Vosec(+5V) load from 17mA to 0mA, full load on other Vosec outputs.

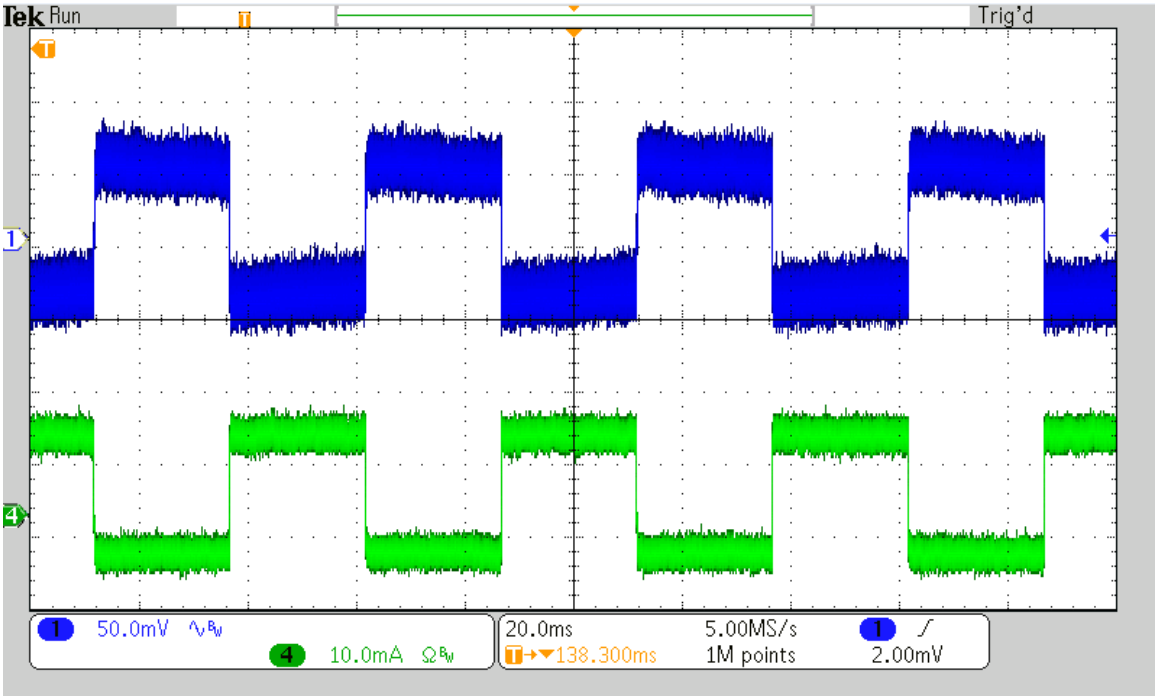


Fig Vosec(+5V)(AC)(blue, channel1) and Iosec(+5V)(green, channel4)

Output Voltage Ripples

Test condition: The input voltage was set at 24V, and all outputs were set at full load.

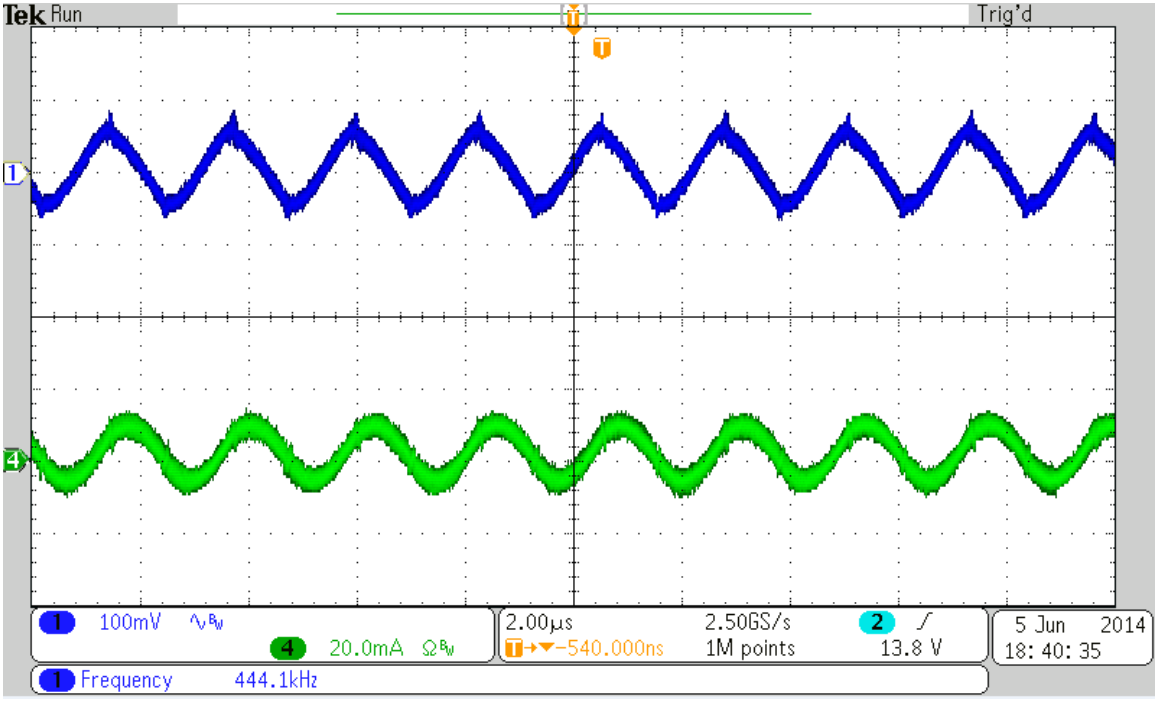


Fig Vosec(15V)(AC)(blue, channel1) and Iosec(15V)(green, channel4)

Test condition: The input voltage was set at 24V, and all outputs were set at full load.

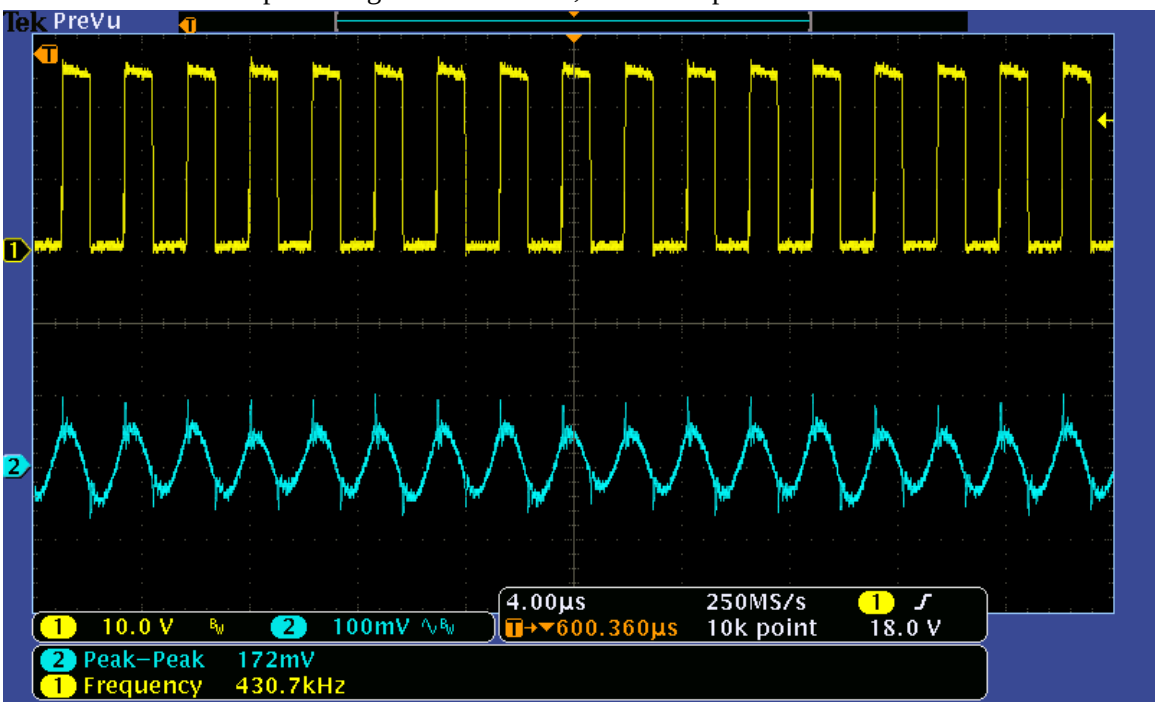


Fig Vosec(-16V)(AC)(blue, channel2) and Vsw(-16V)(yellow, channel1)

Test condition: The input voltage was set at 24V, and all outputs were set at full load.

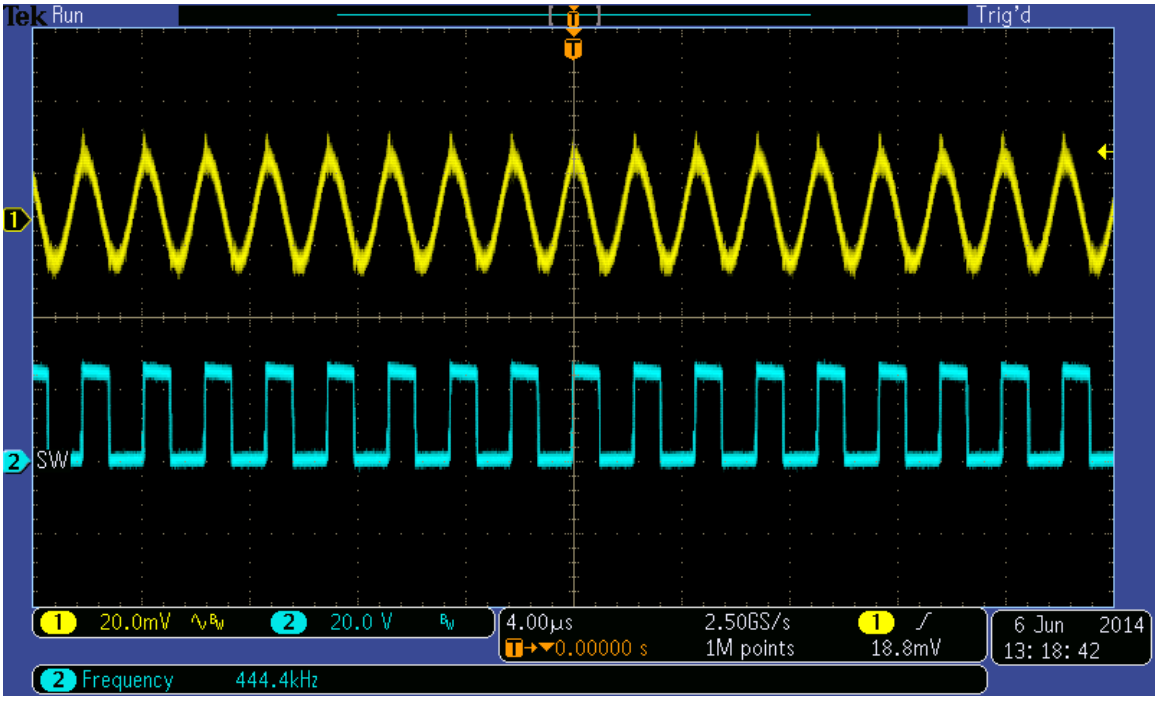


Fig Vosec(5V)(AC)(yellow, channel1) and switch node waveform(blue, channel2)

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