

WVGA digital video SerDes for automotive TFT LCD Displays w/ DVP interface



System Description

The design is a high speed serial video interface to connect a remote automotive WVGA TFT LCD display with DVP (LVCMOS) Interface to a video processing system. It uses TI's FPD-Link II SerDes technology to transmit uncompressed video data over shielded twisted pair cable. Application examples are rear seat entertainment systems, automotive clusters, Head Unit Display.

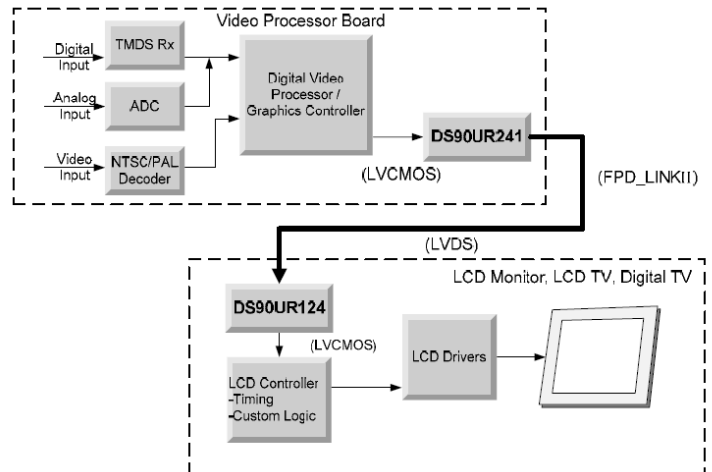
Featured Applications

- Rear Seat Entertainment systems
- Automotive Clusters
- HUD Display
- Navigation Display r

Design Photo



Block Diagram



Design Resources

[DS90UR241-Q1](#)

Product Folder

[EVM User's Guide](#)

Document

[DS90UR124-Q1](#)

Product Folder

Design Features

- Support s WVGA x 60 data rates
- Support DVP (LVCMOS) Interface
- Built In Self-Test (BIST) ASIL B Applications



Jump start system design and speed time to market

Comprehensive designs include schematics or block diagrams, BOMs, design files and test reports by experts with deep system and product knowledge. Designs span TI's portfolio of analog, embedded processor and connectivity products and supports a board range of applications including industrial, automotive, medical, consumer, and more. To explore the designs, go to <http://www.ti.com/tidesigns>

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Associated Part Numbers

<u>Part Number</u>	<u>Part Description</u>	<u>EVM Link</u>
DS90UR241-Q1	5-43MHz DC-Balanced 24-Bit FPD-Link II Serializer	EVM User's Guide
DS90UR124-Q1	5-43MHz DC-Balanced 24-Bit FPD-Link II Deserializer	N/A

Design Considerations:

Connecting a remote display to e.g. an infotainment system requires data lines with sufficient bandwidth and the capability to drive multiple meters of cable in some cases. With fewer wires between the physical interface of the host and the display, FPD-Link II technology is an ideal, cost optimized solution for high speed, low power and low EMI (spread spectrum generation and low voltage differential signal) The serial bus scheme greatly eases system design by eliminating skew problems between clock and data.

Quick Start Guide

What's Needed:

1. One Serializer board with the DS90UR241
2. One De-serializer board with the DS90UR124
3. One 2-meter USB 2.0 Hi-SPEED cable assembly
4. Evaluation Kit Documentation (this manual)
5. DS90UR241/124 Datasheet

Before the system is powered up, please make sure all hardware is configured properly. Check that all jumpers and headers are connected appropriately. For a detailed description of configurations, see EVM user's guide.

1. A two (2) meter USB connector/cable assembly has been included in the kit. Connect 4-pin USB A side of cable harness to the serializer board and the other side 5-pin mini USB jack to the de-serializer board. This completes the LVDS interface connection.
NOTE: The DS90C241 and DS90C124 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.
2. Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the chipset.
3. From the Video Decoder board, connect a flat cable (not supplied) to the Serializer board and connect another flat cable (not supplied) from the De-serializer board to the panel.
Caution: The LVCMOS input levels should be within the specified range for optimal performance, not to exceed the absolute maximum rating of -0.3V to (VCC +0.3V).
Note: For 50 ohm LVCMOS input signal sources, add 50 ohm parallel termination resistors R1-R25 on the DS90UR241 Serializer board and provide appropriate 3.3V LVCMOS input signal levels into DIN[23:0] and TCLK.
4. Power for the Tx and Rx boards must be supplied externally through Power Jack (VDD). Grounds for both boards are connected through Power Jack (VSS) .



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