

The Stackup Legend below this is static.
If you change the stackup, update the Legend.

Layer Name	Material	Copper Thickness	Dielectric
Top Solder Mask	(.GTS)		Solder Resist
Top Layer	(.GTL)	1.4mil	FR-4
Bottom Layer	(.GBL)	1.4mil	FR-4
Bottom Solder Mask	(.GBS)		Solder Resist

DESIGN INFORMATION

MIN. TRACK WIDTH: 8_MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24_MIL
 MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5_MIL, HOLES +/- 3_MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

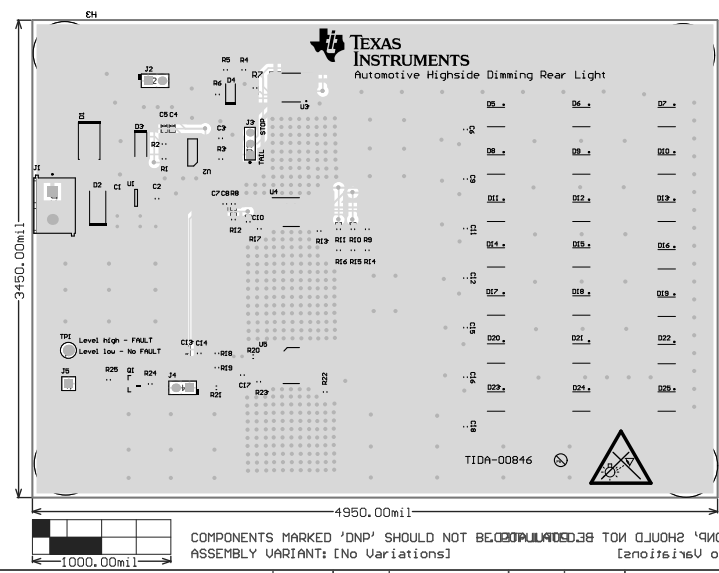
BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR:
 GREEN BLUE OTHER _____

SURFACE FINISH: IMMERSION GOLD (ENG) ENERP
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRIM PER MECH LAYER 1
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



ADDITIONAL COMMENTS: BOARD TOP/SIDE	BOARD #: 001 100 :#	DATE: 01/11/2011	DESIGNER: ANDA ZHANG
LAYER NAME = Top Layer	GENERATED BY: ANDA ZHANG	DATE: 01/11/2011	TIME: 5:38:32 AM
PLOTTING: Top Layer	COMPOSITE: No	GENERATED BY: ANDA ZHANG	DATE: 01/11/2011

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ENGINEER: Anda Zhang	LAYOUT BY: Anda Zhang
SCALE: 1.00	ALTIUM DESIGNER VERSION: 14.3.14.34663

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