

# User's Guide

## CC33xx Hardware Integration



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### ABSTRACT

This document provides necessary information on the WLAN and *Bluetooth*® Low Energy hardware operation to aid engineers in system design. The document reviews the integration process of TI's CC33xx devices into PCBs of final products. When designing a system around the TI chipset, TI recommends following the guidelines outlined in this user guide.

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### Trademarks

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# 1 Introduction

## 1.1 Overview

The SimpleLink™ Wi-Fi™ CC33xx family of devices is where potential cost savings meet reliability, enabling engineers to connect more applications with confidence. CC33xx devices are available in a single-chip, or pre-certified module, integrating both Wi-Fi 6 and Bluetooth Low Energy (BLE) 5.4. The following devices are also pin-to-pin compatible within the relevant packaging family (for example, IC to IC or module to module):

**Table 1-1. CC33xx Companion IC Device Comparison**

| Device | Feature     |                          |           |
|--------|-------------|--------------------------|-----------|
|        | WLAN 2.4GHz | Bluetooth Low Energy 5.4 | WLAN 5GHz |
| CC3300 | ✓           |                          |           |
| CC3301 | ✓           | ✓                        |           |
| CC3350 | ✓           |                          | ✓         |
| CC3351 | ✓           | ✓                        | ✓         |

**Table 1-2. CC33xx Companion Module Comparison**

| Device    | Feature     |                          |           |
|-----------|-------------|--------------------------|-----------|
|           | WLAN 2.4GHz | Bluetooth Low Energy 5.4 | WLAN 5GHz |
| CC3300MOD | ✓           |                          |           |
| CC3301MOD | ✓           | ✓                        |           |
| CC3350MOD | ✓           |                          | ✓         |
| CC3351MOD | ✓           | ✓                        | ✓         |

This guide explains the hardware requirements and recommendations for integrating the CC33xx devices.

## 2 Schematic Considerations – CC33xx Devices

The CC33xx devices are designed to integrate easily with any system and require few external components. The digital interface to the host processor (MPU or MCU) is highly flexible based on the end application. Users can decide to use any combination of secure digital input output (SDIO), serial peripheral interface (SPI), or universal asynchronous receiver-transmitter (UART) for shared Wi-Fi and Bluetooth Low Energy communication.

This section explains the minimum requirements for optimizing an engine area schematic.

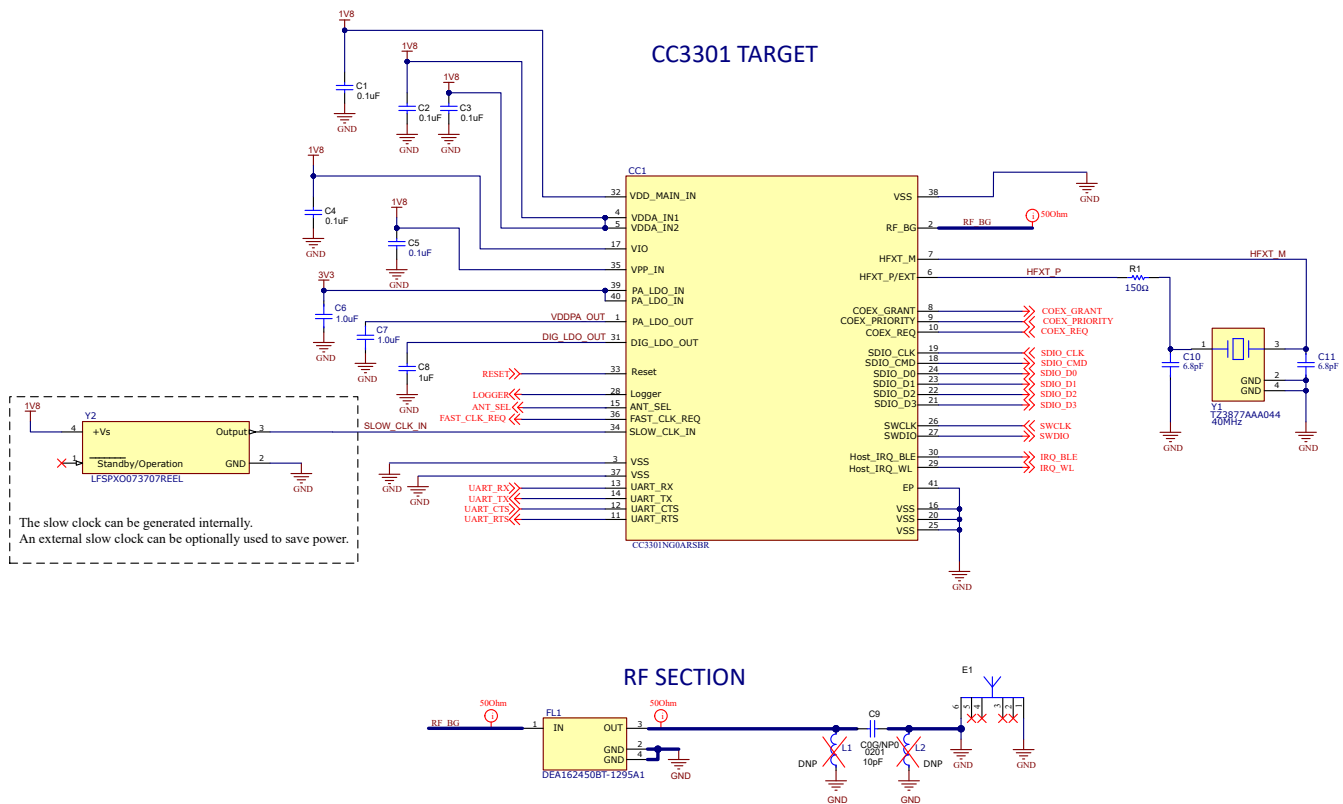
### 2.1 Schematic Reference Design

TI recommends following the reference design and guidelines for the CC33xx devices as closely as possible to achieve the full capabilities of the CC33xx devices (as listed in the device-specific data sheet) and to pass certification. The schematic designs recommended for the CC33xx and CC335x devices are accessed here:

[CC330x Reference Design Files](#)

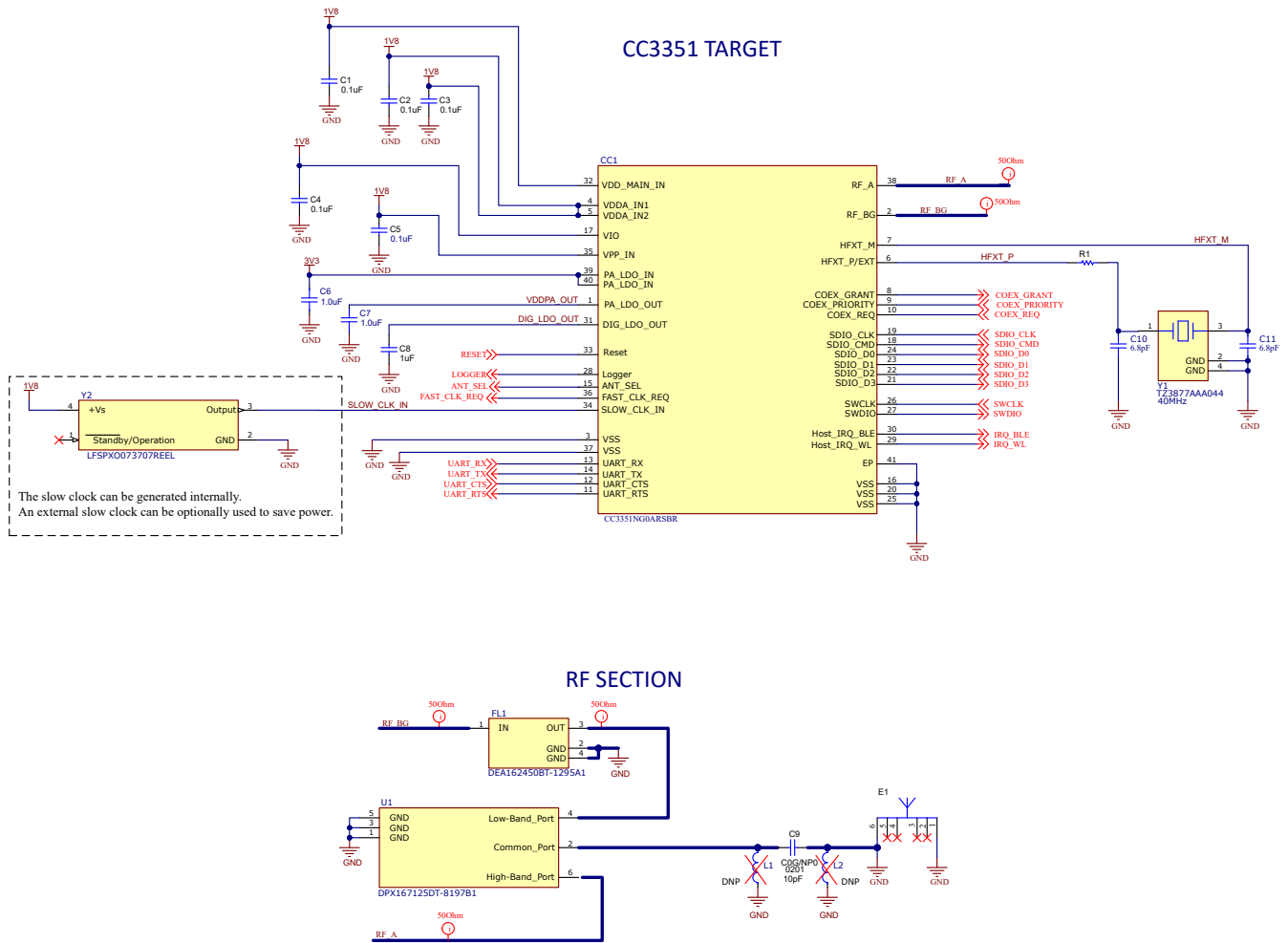
[CC335x Reference Design Files](#)

Figure 2-1 and Figure 2-2 show the reference schematics for the CC330x and CC335x devices.



A. TI recommends RF Shield for optimal regulatory compliance.

**Figure 2-1. CC33xx Reference Schematic**



A. TI recommends RF Shield for optimal regulatory compliance.

**Figure 2-2. CC335x Reference Schematic**

The only difference between the schematics for the CC33xx and CC335x devices is the added diplexer U1 for 5GHz support in the CC335x devices. For more information on the RF section of the schematic, see [Section 2.4](#).

**Table 2-1. Bill of Materials**

| Item | Designator of Reference  | Quantity | Value | Part Number        | Manufacturer           | Description   | Package Reference      |
|------|--|----------|-------|--------------------|------------------------|---|------------------------|
| 1    | C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> | 5        | 0.1µF | GRM033C71A104KE14D | Murata                 | CAP, CERM, 0.1µF, 10V, ±10%, X7S, 0201<br>Matching component:<br>CAP, CERM, 10pF, 50V, ±5%, C0G/NP0, 0201 | 0201                   |
| 2    | C <sub>6</sub> , C <sub>7</sub>  | 2        | 1µF   | GRM033D70J105ME01D | Murata                 | Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 1.0µF, X7T, +22%/-33%, 20%, 6.3V            | 0201                   |
| 3    | C <sub>8</sub>   | 1        | 1µF   | GRM155R70J105MA12D | Murata                 | CAP, CERM, 1µF, 6.3V, ±20%, X7R, 0402   | 0402                   |
| 4    | C <sub>9</sub>   | 1        | 10pF  | GJM0335C1E100JB01D | Murata                 | CAP, CERM, 10pF, 25V, ±5%, C0G/NP0, 0201  | 0201                   |
| 5    | C <sub>10</sub> , C <sub>11</sub>  | 2        | 6.8pF | GJM0335C1H6R8BB01  | Murata                 | Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 6.8pF, COG, 30ppm/°C, 0.25pF, 50V           | 0201                   |
| 6    | R1   | 1        | 150Ω  | RC0201FR-7D150RL   | YAGEO                  | RES, 150, 1%, 0.05W, 0201   | 0201                   |
| 7    | CC1  | 1        |       | CC33x1NG0ARSBR     | Texas Instruments      | CC33x1NG0ARSBR – Wi-Fi 6 and Bluetooth Low Energy 5.2 Combo Transceiver                                   | WQFN40                 |
| 8    | Y2   | 1        |       | TZ3877AAAO44       | Tia-Saw Technology     | Crystal Unit SMD 2.0 x 1.6 40.0MHz  | SMT4_2MM05_1MM65       |
| 9    | FL1  | 1        |       | DEA162450BT-1295A1 | TDK                    | 2.45GHz Center Frequency Band Pass RF Filter, 100MHz Bandwidth, 1.8dB 0603, 3 PC Pad                      | SMT_FILTER_1MM60_0MM80 |
| 10   | <b>Only for CC335x:</b> U1   | 1        |       | DPX167125DT-8197B1 | TDK                    | Multilayer Diplexer for 2.4-2.5GHz W-LAN and Bluetooth / 5-7GHz W-LAN                                     | SMD6                   |
| 11   | <b>Optional:</b> Y1 <sup>(1)</sup>   | 1        |       | LFSPX0073707REEL   | IQD Frequency Products | <b>Optional:</b> 32.768kHz XO (Standard) CMOS Oscillator 1.8V Enable/Disable 4-SMD, No Lead               | SMT4_2MM0_1MM6         |

- (1) The slow clock can be generated internally. An external slow clock can be optionally used to consume less power than sourcing the slow clock internally.

## 2.2 Power Supply

There are two power rails that must be routed to the CC33xx devices:

- 1.8V: VDD\_MAIN\_IN, VDDA\_IN1, VDDA\_IN2, VIO, and VPP\_IN
- 3.3V: PA\_LDO\_IN

The CC33xx devices have internal LDOs for regulating the digital core, memory, and power amplifier supplies. The output of the LDO can be measured from the DIG\_LDO\_OUT and PA\_LDO\_OUT signals.

### Note

The output of the PA\_LDO\_OUT signal is not enabled until firmware is loaded onto the device.

For further information on the operating conditions for the supply pins, see [Table 2-2](#).

**Table 2-2. Required Device Power**

| Pin | Signal      | Direction (I/O) | Required Voltage (Typical) |
|-----|-------------|-----------------|----------------------------|
| 1   | PA_LDO_OUT  | O               | N/A                        |
| 31  | DIG_LDO_OUT | O               | N/A                        |
| 17  | VIO         | I               | 1.8V                       |
| 32  | VDD_MAIN_IN | I               | 1.8V                       |
| 4   | VDDA_IN1    | I               | 1.8V                       |
| 5   | VDDA_IN2    | I               | 1.8V                       |
| 35  | VPP_IN      | I               | 1.8V                       |

**Table 2-2. Required Device Power (continued)**

| Pin | Signal    | Direction (I/O) | Required Voltage (Typical) |
|-----|-----------|-----------------|----------------------------|
| 39  | PA_LDO_IN | I               | 3.3V                       |
| 40  |           |                 |                            |

**2.2.1 Power Input/Output Requirements**

The following lists the supply connections in descending order of criticality:

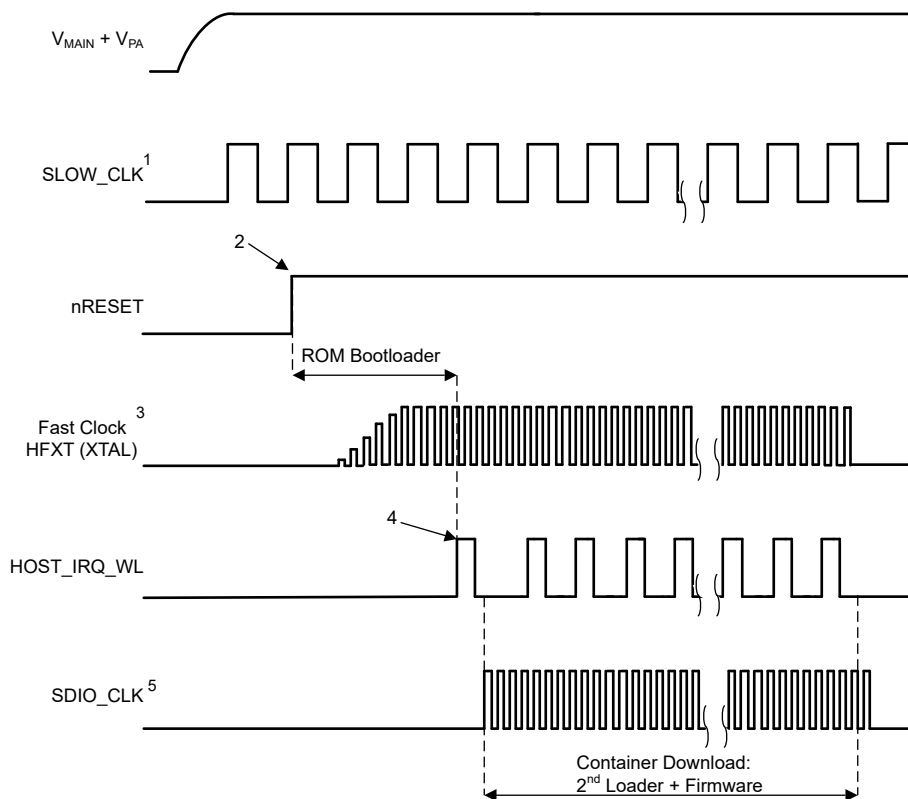
- PA\_LDO\_OUT (pin 1): Provide decoupling capacitor (1.0µF)
- VDDA\_IN1 (pin 4): Provide decoupling capacitor (0.1µF)
- VDDA\_IN2 (pin 5): Provide decoupling capacitor (0.1µF)
- DIG\_LDO\_OUT (pin 31): Provide decoupling capacitor (1.0µF)
- VPP\_IN (pin 35): Provide decoupling capacitor (0.1µF).
- VIO (pin 17): Provide decoupling capacitor (0.1µF)
- VDD\_MAIN\_IN (pin 32): Provide decoupling capacitor (0.1µF)

Prioritize the placements of the bypass capacitor in order of criticality to maximize RF performance.

**2.2.2 Boot Sequence**

For the CC33xx devices to function correctly, the proper boot-up sequence must be followed. Normally, this boot sequence is managed by the host driver, in regard to the interfaces between the CC33xx devices and the host.

Figure 2-3 shows the top-level boot-up sequence for the CC33xx devices when using an SDIO (secure digital input output) for the default setup of the host processor communication.



**Figure 2-3. CC33xx Boot-Up Sequence**

### Note

1. For an external slow clock, verify that the clock is stable before the nReset pin is deasserted (high).
2. All power supplies (VDD\_MAIN\_IN, VDDA, V<sub>IO</sub>, and V<sub>PA</sub>) must be stable for at least 10μs before the nReset pin is deasserted.
  - a. VDD\_MAIN\_IN and V<sub>IO</sub> power supplies must be supplied from the same source to prevent glitches on the I/O during power up.
  - b. VDDA\_IN1/IN2 and PA\_LDO\_IN power supplies can be supplied independent of all other supplies.
3. The external fast clock (HFXT) stabilizes during the ROM bootloader. The clock is active until the CC33xx devices go into sleep mode after boot is finished.
4. The ROM bootloader is the first stage of boot for the CC33xx devices, boot begins when the nReset pin deasserts (device enable) and ends when the HOST\_IRQ\_WL line indicates *output high* from the device, signaling to the host that the boot stage is complete.
5. After the ROM bootloader is finished, the CC33xx devices are ready to receive two binary containers (secondary bootloader + firmware) from the host processor through the SDIO or SPI lines. These containers are downloaded in memory chunks. At the end of every chunk, the CC33xx devices send an acknowledge to the host by raising the HOST\_IRQ\_WL line *high*, signaling to the host that the memory chunk was successfully received and the device is now ready for the next chunk. The SDIO\_CLK is driven by the host and is only active when the SDIO bus is active.
6. After the containers are downloaded to the CC33xx devices, the device completes initialization and goes to sleep.

#### 2.2.2.1 SOP Modes

The logger (pin 28) and Host\_IRQ\_WL (pin 29) signals are considered *sense on power* (SOP) pins. When connecting these pins to a host, verify the Host\_IRQ\_WL (pin 29) pin stays at the *low* logic level during power-up, and the logger (pin 28) pin stays at the *high* logic level during power-up.

If these SOP pins are connected to a host that potentially affects the logic level of these lines, consider adding an optional pulldown and pullup resistor (or resistors).

#### 2.2.3 Power Down Sequence

To improve reliability and proper boot up following the power-down sequence, follow the correct power-down sequence for the CC33xx devices.

To perform the correct shutdown sequence:

1. Deassert (low) the nRESET pin while the slow clock (if sourced externally) and all supplies to the device (VDD\_MAIN\_IN, VDDA, V<sub>IO</sub>, and V<sub>PA</sub>) are still stable and available.
2. Only deassert the power supplies to the chip *after* the nRESET signal is deasserted (low).

A successful shutdown sequence takes 1μs to complete after the nRESET pin is low. If the power supplies remain stable, the minimum time between two successive device enables is 1μs.

### 2.3 Clock Source

The CC33xx devices use two clocks for operation:

- A fast clock running at 40MHz for WLAN/BLE functions
- A slow clock running at 32.768kHz for low power modes

The fast clock must be generated externally. The slow clock can be generated internally by the devices or externally by an oscillator.

**Note**

A deviation in clock frequency is reflected as a deviation in radio frequency.

See [Simplelink Frequency Tuning](#) for more information on how to carefully select external loading capacitors ( $C_L$ ) to complete frequency tuning according to specific board layouts.

**2.3.1 Fast Clock**

The CC33xx devices support a crystal-based fast clock (XTAL). The crystal is fed directly between the HFXT\_P and HFXT\_M pins with the appropriate loading capacitors and a 150Ω resistor. The following lists the design requirements:

1. Provide a 150Ω resistor on the HFXT\_P (pin 6), close to the device and before the XTAL.
2. Connect the XTAL across the HFXT\_P (pin 6) and HFXT\_M (pin 7) pins.
3. Provide load capacitors (6.8pF) at both pins of the XTAL.

**Note**

The recommended load capacitor of 6.8pF is based on a TI board layout.

4. Tune the load capacitance, if required.

**Note**

The requirement of this step is based on the board layout implemented by the customer. This step is not always necessary for the board. See [Simplelink Frequency Tuning](#) for further guidance on this topic.

The fast clock component must meet the requirements shown in [Table 2-3](#).

**Table 2-3. External Fast Clock XTAL Specifications**

| Parameter                              | Test Conditions               | MIN | TYP | MAX                      | Unit |
|--|-------------------------------|-----|-----|--------------------------|------|
| Supported frequencies                  |                               |     | 40  |                          | MHz  |
| Frequency accuracy                     | Initial + temperature + aging |     |     | ±25   ±20 <sup>(2)</sup> | ppm  |
| Load Capacitance, $C_L$ <sup>(1)</sup> |                               | 5   |     | 13                       | pF   |
| Equivalent series resistance, ESR      |                               |     |     | 40                       | Ω    |
| Drive level                            |                               |     | 100 |                          | μW   |

- (1) Load capacitance,  $C_L = [C1 \times C2] / [C1 + C2] + C_p$ , where C1 and C2 are the capacitors connected on the HFXT\_P and HFXT\_M pins, respectively, and  $C_p$  is the parasitic capacitance (typically 1pF to 2pF). For example, for C1 = C2 = 6.2pF and  $C_p = 2pF$ , then  $C_L = 5pF$ .
- (2) When selecting an XTAL for a design implementing the CC330x devices, the accuracy requirement for frequency is ±25ppm. When selecting an XTAL for a design implementing the CC335x devices, the accuracy requirement for frequency is ±20ppm.

**2.3.2 Slow Clock**

The slow clock is generated by the internal oscillator of the device, but an external oscillator can also be used.

**2.3.2.1 Slow Clock Generated Internally**

To minimize external components, the slow clock can be generated by an internal oscillator. However, this clock is less accurate and consumes more power than sourcing the slow clock externally. For this scenario, the SLOW\_CLK\_IN pin must be left not connected.

**2.3.2.2 Slow Clock Using an External Oscillator**

For excellent power consumption, the slow clock can be generated externally by an oscillator or sourced elsewhere in the system. The external source must meet the requirements shown in [Table 2-4](#). This clock can be fed into the SLOW\_CLK\_IN pin of the CC335xMOD and must be stable before the nReset pin is deasserted and the device is enabled.

**Table 2-4. External Slow Clock Requirements**

| Parameter                  | Description | MIN | TYP   | MAX | Unit |
|----------------------------|-------------|-----|-------|-----|------|
| Input slow clock frequency | Square wave |     | 32768 |     | Hz   |

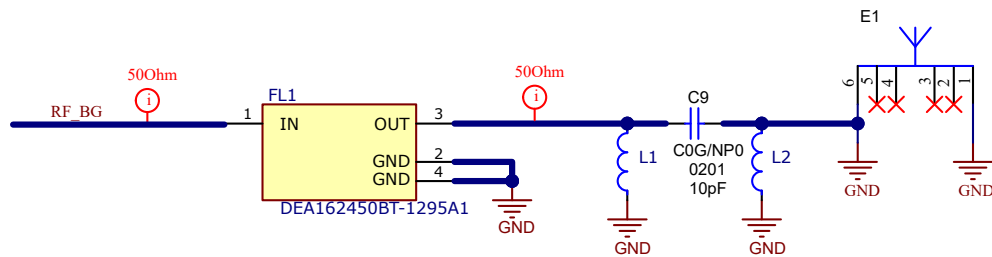
**Table 2-4. External Slow Clock Requirements (continued)**

| Parameter          | Description                   | MIN   | TYP | MAX                  | Unit |
|--------------------|-------------------------------|---|-----|----------------------|------|
| Frequency accuracy | Initial + temperature + aging |   |     | ±250                 | ppm  |
| Input duty cycle   |                               | 30%   | 50% | 70%                  |      |
| $T_r/T_f$          | Rise and fall time            | 10% to 90% (rise) and 90% to 10% (fall) of digital signal level |     | 100                  | ns   |
| $V_{IL}$           | Input low level               | 0   |     | $0.35 \times V_{IO}$ | V    |
| $V_{IH}$           | Input high level              | $0.65 \times V_{IO}$  |     | 1.95                 | V    |
|                    | Input impedance               | 1   |     |                      | MΩ   |
|                    | Input capacitance             |   |     | 5                    | pF   |

## 2.4 Radio Frequency (RF)

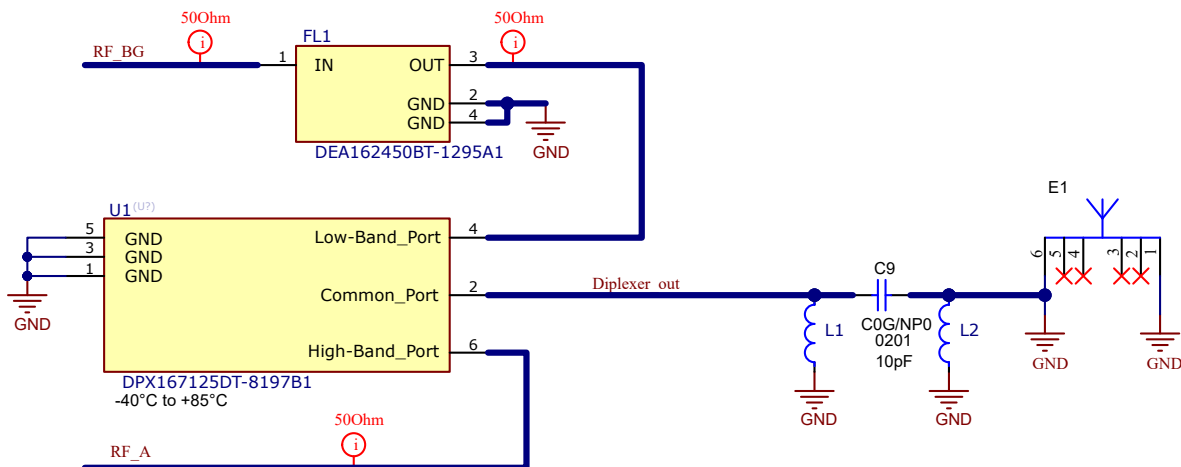
Routing out the RF\_BG (pin 2) pin is required for radio frequency (RF) functionality when implementing the CC330x devices in a single band 2.4GHz configuration. Routing out the RF\_A (pin 38) pin is an additional requirement for radio frequency (RF) functionality when implementing the CC335x devices in a dual band 5GHz configuration.

On the RF\_BG trace, a band pass filter (BPF) is required along this path before reaching any radiative or conductive component. See Table 2-1 for the recommended BPF. TI also recommends implementing an impedance matching network (such as a PI or L network) before the antenna for better RF performance. Figure 2-4 is an example of a schematic design for the RF path when designing for a single band 2.4GHz configuration (CC330x). In this single band 2.4GHz use-case, ground the RF\_A (pin 38) pin for better noise reduction.



**Figure 2-4. BG Band Reference Schematic**

Additional routing is required for the RF\_A (pin 38) pin when designing with the CC335x devices to enable a 5GHz RF with a 2.4GHz RF band. To use both RF bands, a diplexer is required. The RF\_A pin must be connected directly to the high-band port of the diplexer, while the RF\_BG pin must be routed through a BPF (as described previously) and then be connected to the Low\_Band port of the diplexer. See Table 2-1 for the recommended diplexer. Figure 2-5 is an example of a schematic design for the RF path when designing for a dual band 2.4GHz + 5GHz configuration (CC335x).



**Figure 2-5. Dual Band RF Reference Schematic**

Any deviation from these recommendations can cause performance to diverge from the specifications in the datasheet.

If implementing an RF switch (for utilizing antenna diversity), make the input of the RF switch the final filtered signal from the CC33xx devices. Specifically, when designing a dual band RF device that implements a CC335x device, route the input of the RF switch to the common port of the diplexer. When designing a single band RF device that implements a CC330x device, the input of the RF switch must be routed to the output of the BPF. The ANT\_SEL (pin 15) pin can be routed and used as the switching signal. The RF\_IN signal must be connected to the output of the BPF when designing a single band device (with CC330x), and the RF\_IN signal must be connected to the common port of the diplexer when designing a dual band device (with CC335x), as seen in Figure 2-6.

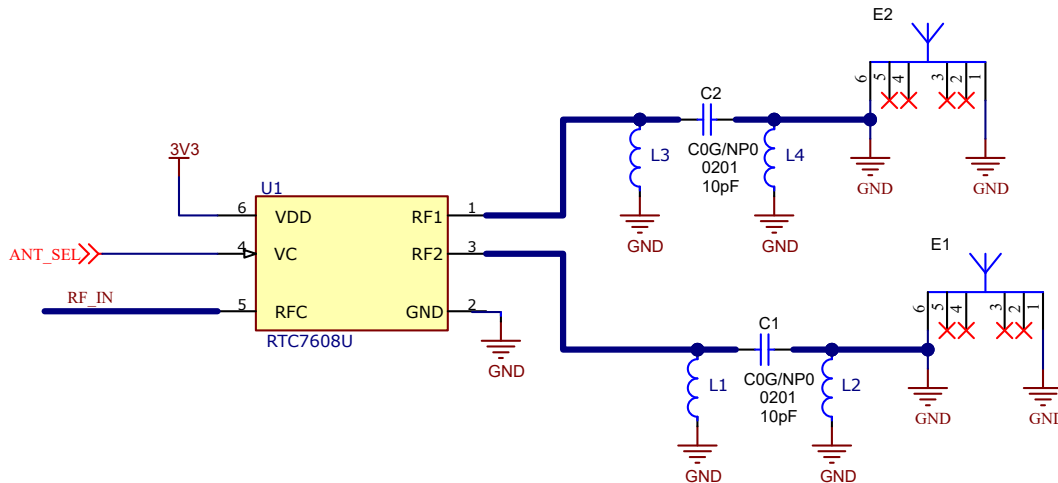


Figure 2-6. Antenna Diversity Reference Schematic

## 2.5 Digital Interfaces

All I/O signals on the CC33xx devices operate at 1.8V (typical). Designs must take in consideration the use of level shifters if utilized at a higher voltage in a system.

### 2.5.1 Reset

The nReset (pin 33) pin, an *active low* signal, must be connected and controlled by the host. If using a setup without a host, reset must be pulled high after power supplies are stable.

When reset is low, the device enters an active shutdown mode. After the device is re-enabled, firmware must be re-downloaded for proper operation.

### 2.5.2 Secure Digital Input Output (SDIO)

An SDIO is the main host interface for wireless communication. The CC33xx devices support a shared SDIO interface for both Wi-Fi and Bluetooth Low Energy protocols.

As per the SDIO specification, the host expects these data lines to be pulled up (SDIO\_D0, SDIO\_D1, SDIO\_D2, SDIO\_03, and SDIO\_CMD). Take care that components (for example, level shifters) on the SDIO data lines do not change the state of these data lines to a low logic level.

2.5.2.1 SDIO Timing Diagram: Default Speed

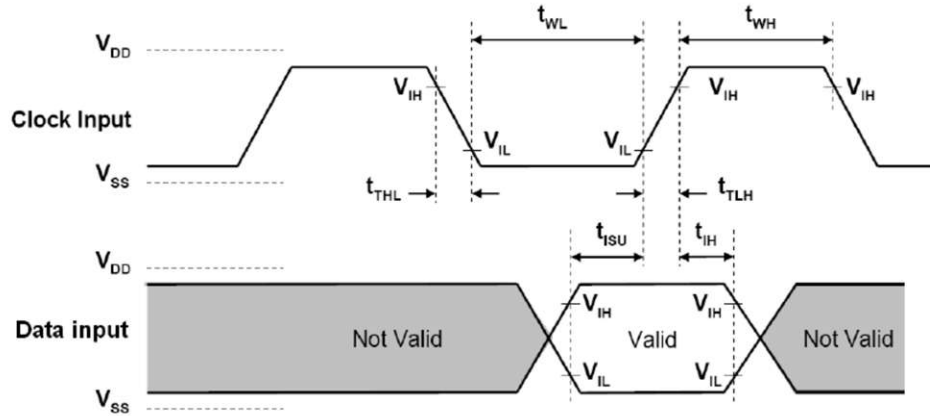


Figure 2-7. SDIO Default Input Timing

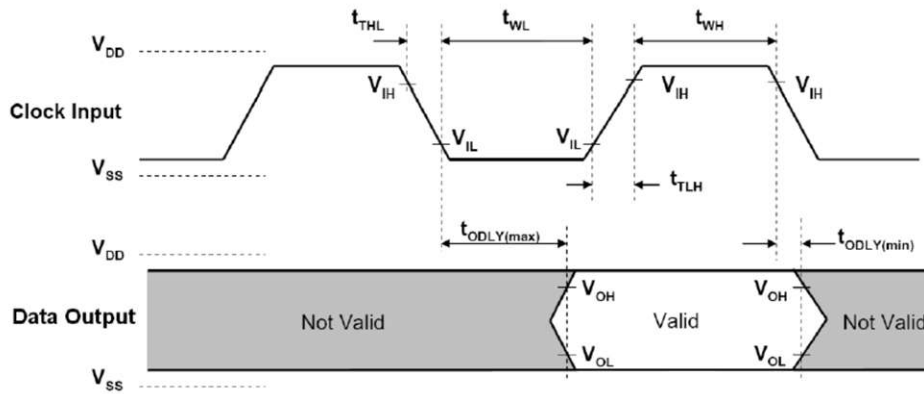
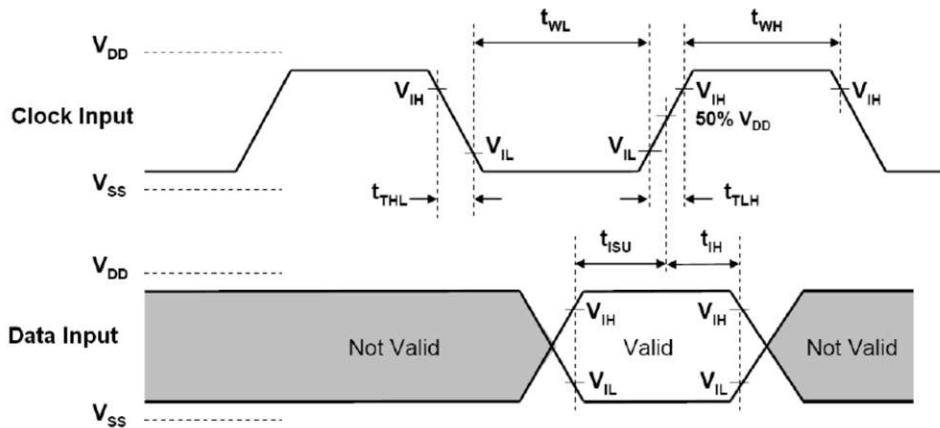


Figure 2-8. SDIO Default Output Timing

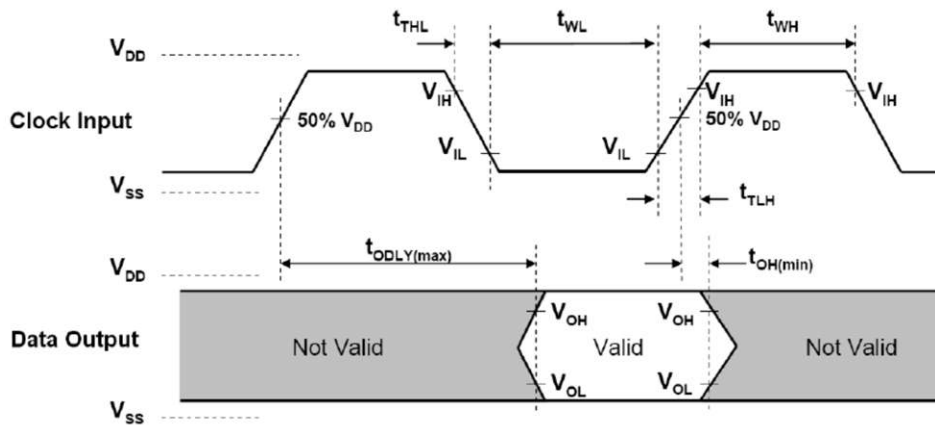
**Table 2-5. SDIO Timing Parameters: Default Speed**

| Parameter          | Description                                   | MIN | MAX | Unit |
|--------------------|---|-----|-----|------|
| $f_{\text{clock}}$ | Clock frequency, CLK                          |     | 26  | MHz  |
| $t_{\text{High}}$  | High period                                   | 10  |     | ns   |
| $t_{\text{Low}}$   | Low period                                    | 10  |     |      |
| $t_{\text{TLH}}$   | Rise time, CLK                                |     | 10  |      |
| $t_{\text{THL}}$   | Fall time, CLK                                |     | 10  |      |
| $t_{\text{ISU}}$   | Setup time, input valid before CLK $\uparrow$ | 5   |     |      |
| $t_{\text{IH}}$    | Hold time, input valid after CLK $\uparrow$   | 5   |     |      |
| $t_{\text{ODLY}}$  | Delay time, CLK $\downarrow$ to output valid  | 2   | 14  |      |
| $C_L$              | Capacitive load on outputs                    | 15  | 40  | pF   |

**2.5.2.2 SDIO Timing Diagram: High Speed**



**Figure 2-9. SDIO HS Input Timing**



**Figure 2-10. SDIO HS Output Timing**

**Table 2-6. SDIO Timing Parameters: High Speed**

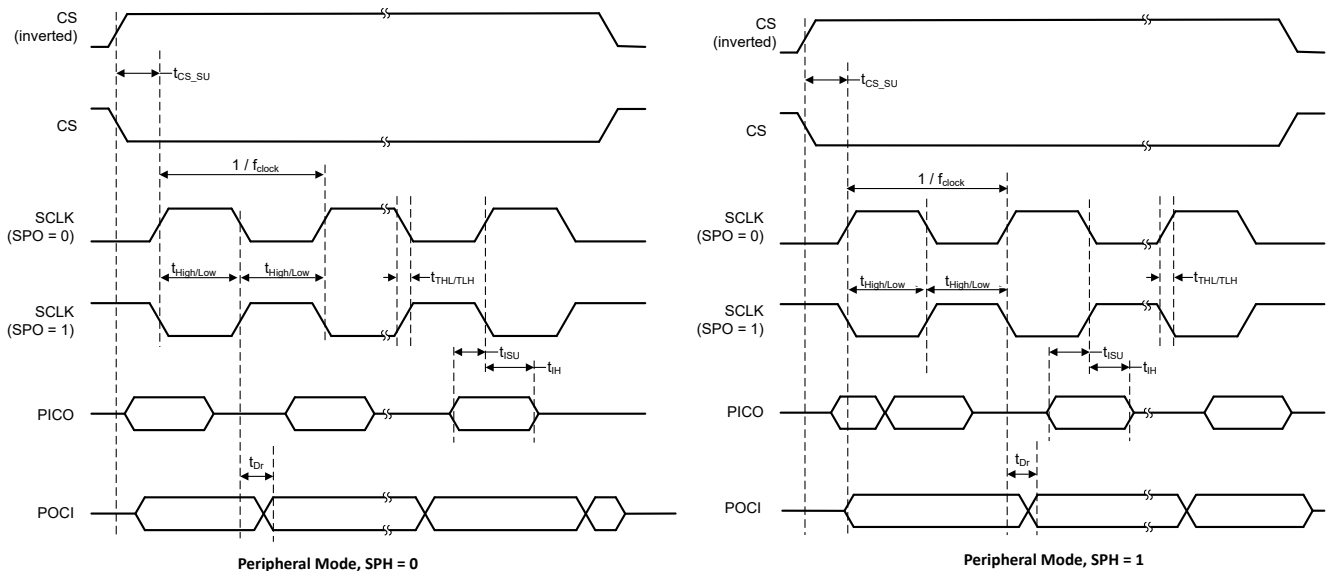
| Parameter          | Description                                   | MIN | MAX | Unit |
|--------------------|---|-----|-----|------|
| $f_{\text{clock}}$ | Clock frequency, CLK                          |     | 52  | MHz  |
| $t_{\text{High}}$  | High period                                   | 7   |     | ns   |
| $t_{\text{Low}}$   | Low period                                    | 7   |     |      |
| $t_{\text{TLH}}$   | Rise time, CLK                                |     | 3   |      |
| $t_{\text{THL}}$   | Fall time, CLK                                |     | 3   |      |
| $t_{\text{ISU}}$   | Setup time, input valid before CLK $\uparrow$ | 6   |     |      |
| $t_{\text{IH}}$    | Hold time, input valid after CLK $\uparrow$   | 2   |     |      |
| $t_{\text{ODLY}}$  | Delay time, CLK $\uparrow$ to output valid    | 2   | 14  |      |
| $C_L$              | Capacitive load on outputs                    | 15  | 40  | pF   |

### 2.5.3 Serial Peripheral Interface (SPI)

The SPI signal lines can be used as a host interface for wireless communication. The CC33xx devices also support a shared SPI for both BLE and WLAN. The SPI lines on CC33xx include:

- SDIO\_CMD (SPI PICO)
- SDIO\_CLK (SPI clock)
- SDIO\_D3 (SPI CS)
- SDIO\_D0 (SPI POCI)

#### 2.5.3.1 SPI Timing Diagram


**Figure 2-11. SPI Timing Diagram**

**Table 2-7. SPI Timing Parameters**

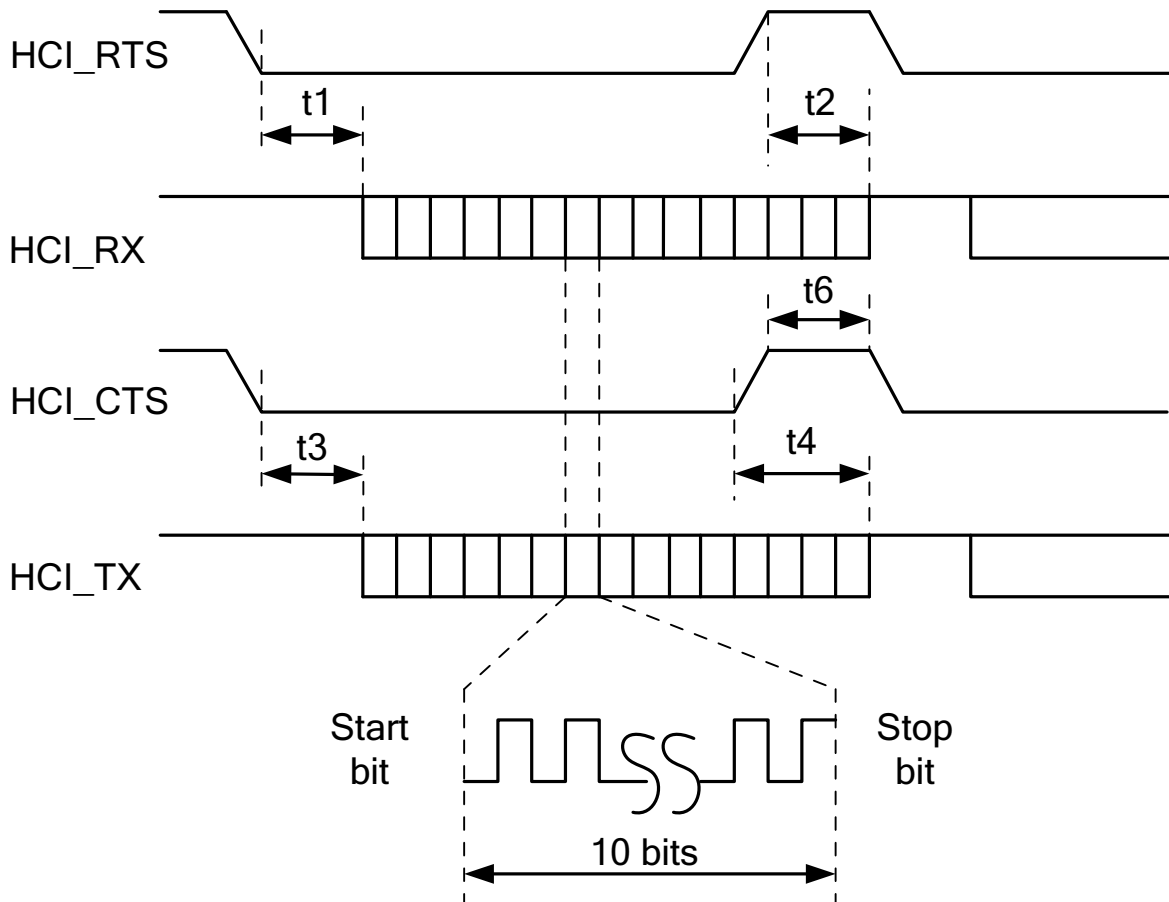
| Parameter                                      | Description   | MIN | MAX | Unit |
|--|---|-----|-----|------|
| $f_{\text{clock}}$                             | Clock frequency, CLK                                  |     | 26  | MHz  |
| $t_{\text{High}}$                              | High period   | 10  |     | ns   |
| $t_{\text{Low}}$                               | Low period  | 10  |     |      |
| $t_{\text{TLH}}$                               | Rise time, CLK  |     | 3   |      |
| $t_{\text{THL}}$                               | Fall time, CLK  |     | 3   |      |
| $t_{\text{CSsu}}$                              | CS setup time, CS valid before CLK $\uparrow$         | 3   |     |      |
| $t_{\text{ISU}}$                               | PICO, input valid before CLK $\uparrow$               | 3   |     |      |
| $t_{\text{IH}}$                                | PICO hold time, input valid after CLK $\uparrow$      | 3   |     |      |
| $t_{\text{Dr}}, t_{\text{Df}} - \text{Active}$ | Delay time, CLK $\uparrow/\downarrow$ to output valid | 2   | 10  |      |
| $t_{\text{Dr}}, t_{\text{Df}} - \text{Sleep}$  | Delay time, CLK $\uparrow/\downarrow$ to output valid |     | 12  |      |
| $C_L$  | Capacitive load on outputs                            | 15  | 40  | pF   |

### 2.5.4 Universal Asynchronous Receiver-Transmitter (UART)

UART is the main host interface for BLE, which supports a host controller interface (HCI) transport layer. When a UART is used with a host, take care to connect the UART correctly:

- Pin 14 is the UART\_TX of the device and must be connected to the host side of the RX.
- Pin 13 is the UART\_RX of the device and must be connected to the host side of the TX.
- Pin 12 is the UART\_CTS of the device and must be connected to the host side of the RTS.
- Pin 13 is the UART\_RTS of the device and must be connected to the host side of the CTS.

#### 2.5.4.1 UART Timing Diagram



**Figure 2-12. UART Timing Diagram**

**Table 2-8. UART Timing Parameters**

| Parameter                   | Condition                 | MIN   | TYP | MAX   | Unit |
|-----------------------------|---------------------------|-------|-----|-------|------|
| Baud rate                   |                           | 37.5  |     | 4364  | kbps |
| Baud rate accuracy per byte | Receive   Transmit        | -2.5  |     | +1.5  | %    |
| Baud rate accuracy per bit  | Receive   Transmit        | -12.5 |     | +12.5 | %    |
| CTS low to TX_DATA on       |                           | 0     | 2   |       | ms   |
| CTS high to TX_DATA off     | Hardware flow control     |       |     | 1     | Byte |
| CTS high pulse width        |                           | 1     |     |       | bit  |
| RTS low to RX_DATA on       |                           | 0     | 2   |       | ms   |
| RTS high to RX_DATA off     | Interrupt set to 1/4 FIFO |       |     | 16    | Byte |

### 2.5.5 Serial Wire Debug (SWD)

The two serial wire debug pins on the CC33xx devices include the SWCLK (pin 26) and SWDIO (pin 27) pins. These signals are used for various types of debug (such as RF testing) and must be routed to test points for troubleshooting.

### 2.5.6 WLAN Interrupt Request (HOST\_IRQ\_WL)

The CC33xx devices require an interrupt request (IRQ) line between the individual device and the host, in addition to the serial host interface (SDIO, SPI, or UART). This IRQ line is important for the proper function of the host driver; where the host receives the signal from the CC33xx device any time the device tries to send something on the host interface, and the CC33xx signals an acknowledgment to the host when a message is received from the host.

By default, this IRQ line is a separate dedicated GPIO between the host and the CC33xx device. The option to use an SDIO in-band interrupt also exists; where the interrupt is enabled over the SDIO bus, reducing the total number of pins necessary to interface with the host.

### 2.5.7 Logger

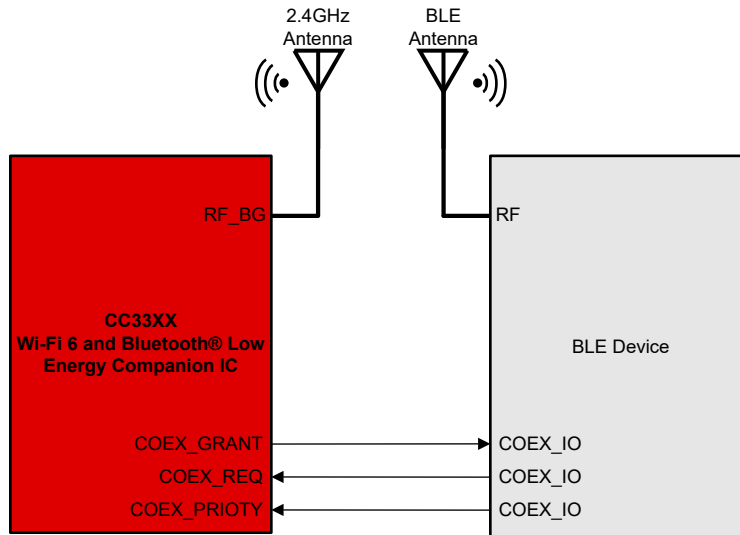
The logger pin (pin 28) of the CC33xx devices is an output tracer for firmware logs. This pin is useful for an in-depth debug of the firmware running on the CC33xx devices. TI provides parsers and documentation for how to read these logs in the CC33xx driver release. The firmware logs are normally not necessary unless undergoing deep debugging with TI, as other debugging tools exist as part of the driver. In the event that these logs are necessary, connecting the logger pin routed to a test point is a good option for access.

### 2.5.8 Coexistence

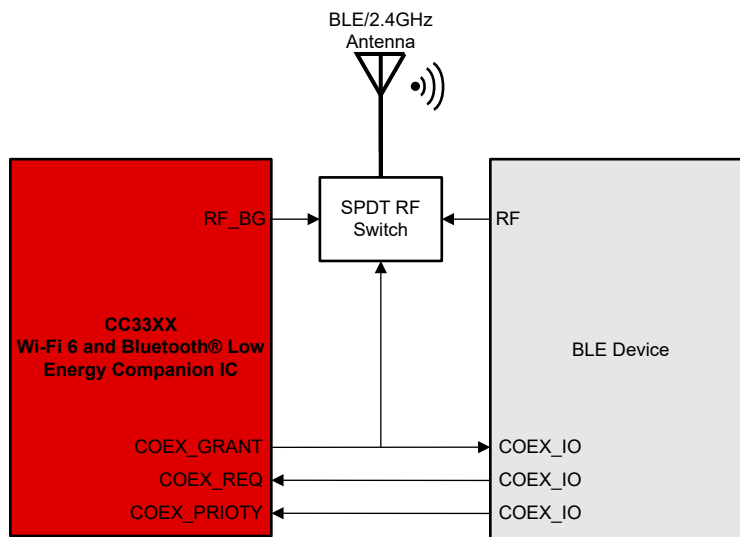
The coexistence feature is a means to organize wireless packet traffic for communication protocols operating in the same frequency band. The CC33xx devices behave as the coexistence primary device and communicate to the coexistence secondary device. The CC33xx devices support a three-wire packet traffic arbitration (PTA) interface for coexistence. The coexistence signals on the CC33xx devices include:

- COEX\_GRANT (pin 8) – an input signal, controlled by the coexistence primary device. Indicates the response of the PTA decision.
- COEX\_PRIORITY (pin 9) – an output signal, controlled by the coexistence secondary device. Indicates the priority of a request signal.
- COEX\_REQ (pin 10) – an output signal, controlled by the coexistence secondary device. Indicates a request to use the shared frequency band.

These three signals on the CC33xx devices must be routed to the matching coexistence pins on the coexistence secondary device. Coexistence is enabled by default and can be configured between internal and external in the INI file. Coexistence can be implemented with either one antenna (for both the primary and secondary device) or two antennas for each device. Figure 2-13 and Figure 2-14 provide visual examples of utilizing the coexistence feature with a Bluetooth Low Energy device.



**Figure 2-13. CC33xx Coexistence With Dual Antennas**



**Figure 2-14. CC33xx Coexistence With Single Antenna**

## 3 Layout Considerations – CC33xx Devices

The CC33xx devices are designed to integrate easily with any system and require few external components. The digital interface to the host processor (MPU or MCU) is highly flexible based on the end application. Users can decide to use any combination of SDIO, SPI, or UART for shared Wi-Fi and Bluetooth Low Energy communication.

This section explains the minimum requirements for optimizing an engine area layout.

### 3.1 Layout Reference Design

TI recommends following the reference design and guidelines for the CC33xx devices as closely as possible to achieve the full capabilities of the CC33xx devices (as listed in the device-specific data sheet) and to pass certification. These layout guidelines are especially important in the engine area, which includes the sensitive RF components and traces.

The following list of designs incorporate the layout guidelines given throughout this document. Refer to these as reference sources:

- [CC330x Reference Design Files](#)
- [CC335x Reference Design Files](#)
- [BP-CC3351](#)
- [M2-CC3351](#)

The figures below include the engine area of the CC33xx devices on the top layer (layer 1) and ground layer (layer 2) for all three designs.

---

#### Note

Before proceeding with any hardware build involving the CC33xx devices, TI recommends reviewing the [CC33x1 Design Checklist](#) before submitting the design for [review](#).

Additionally, the engine area (as shown in the reference design) can be rotated according to the design requirements.

---

### 3.1.1 Reference Design – CC330x Single Band Layout

Figure 3-1 is sampled from the CC330x reference design files.

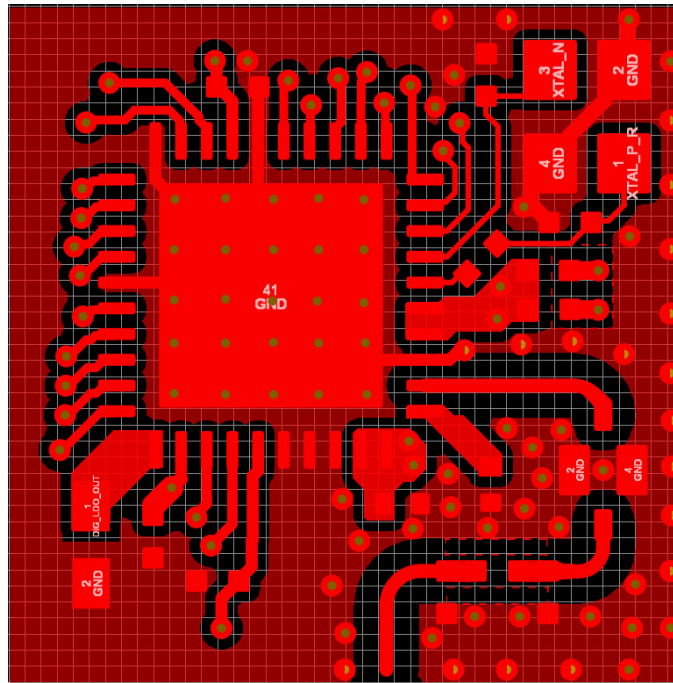


Figure 3-1. CC330x Reference Design, Top (Layer 1)

Figure 3-2 is sampled from the CC330x reference design files.

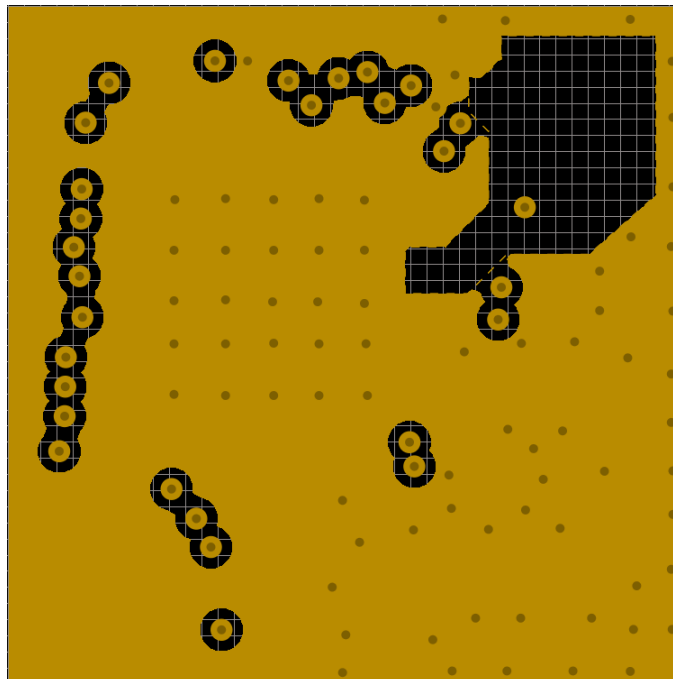


Figure 3-2. CC330x Reference Design, Ground (Layer 2)

### 3.1.2 Reference Design – CC335x Dual Band Layout

Figure 3-3 is sampled from the CC335x reference design files.

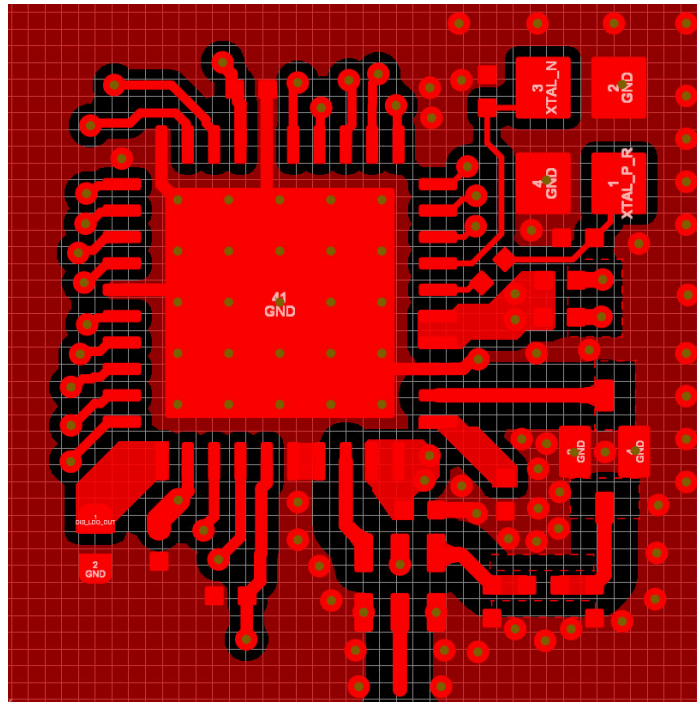


Figure 3-3. CC335x Reference Design, Top (Layer 1)

Figure 3-4 is sampled from the CC335x reference design files.

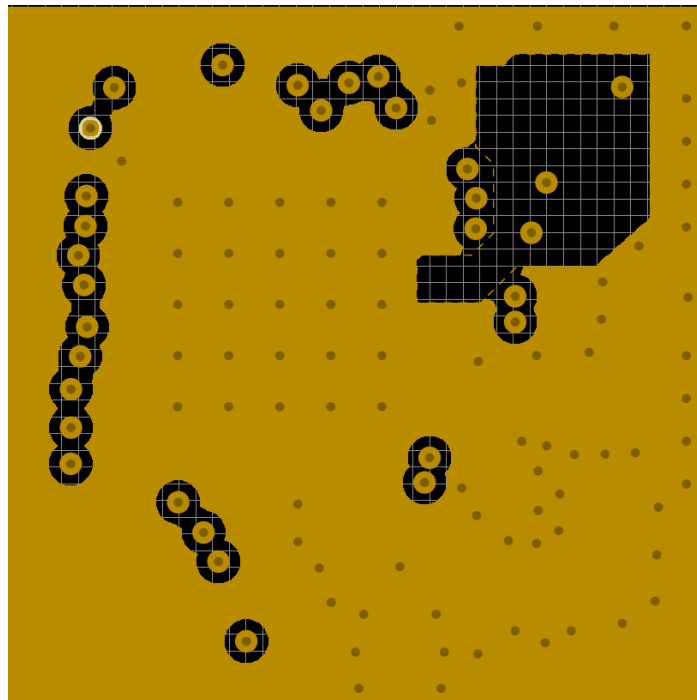


Figure 3-4. CC335x Reference Design, Ground (Layer 2)

### 3.1.3 BP-CC3351 Design Layout

Figure 3-5 is sampled from the BP-CC3351 design files.

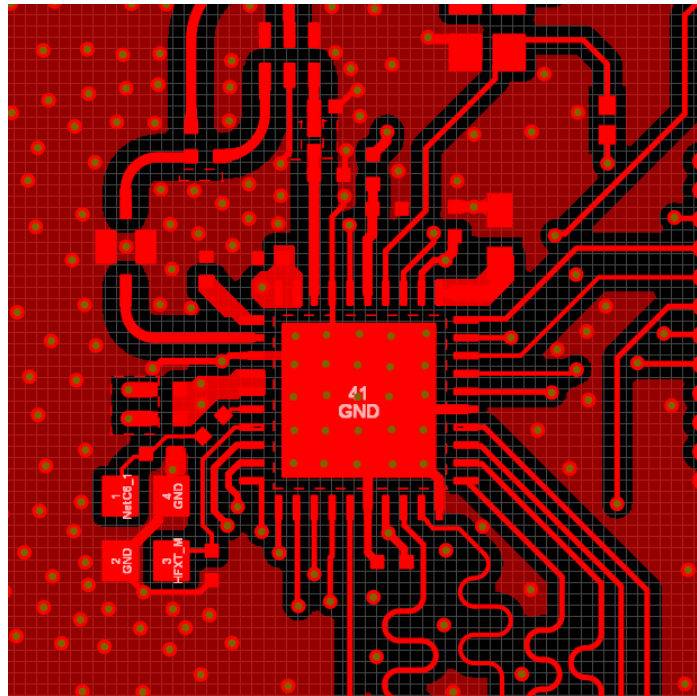


Figure 3-5. BP-CC3351 Layout, Top (Layer 1)

Figure 3-6 is sampled from the BP-CC3351 design files.

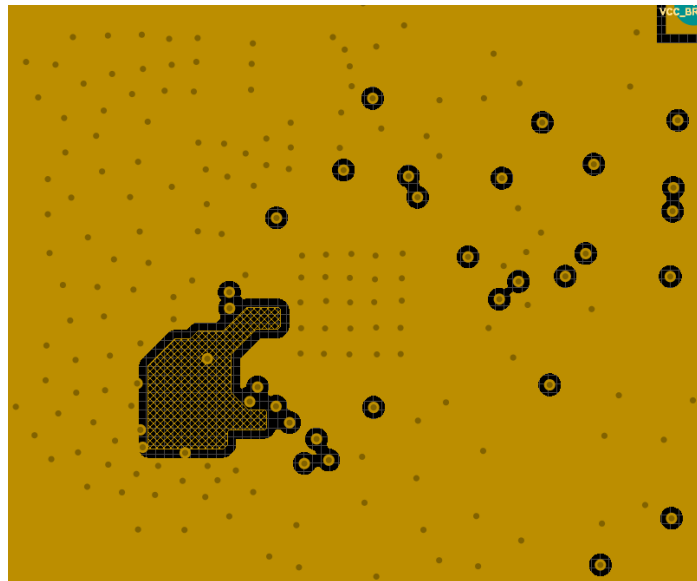


Figure 3-6. BP-CC3351 Layout, Ground (Layer 2)

### 3.1.4 M2-CC3351 Design Layout

Figure 3-7 is sampled from the M2-CC3351 design files.

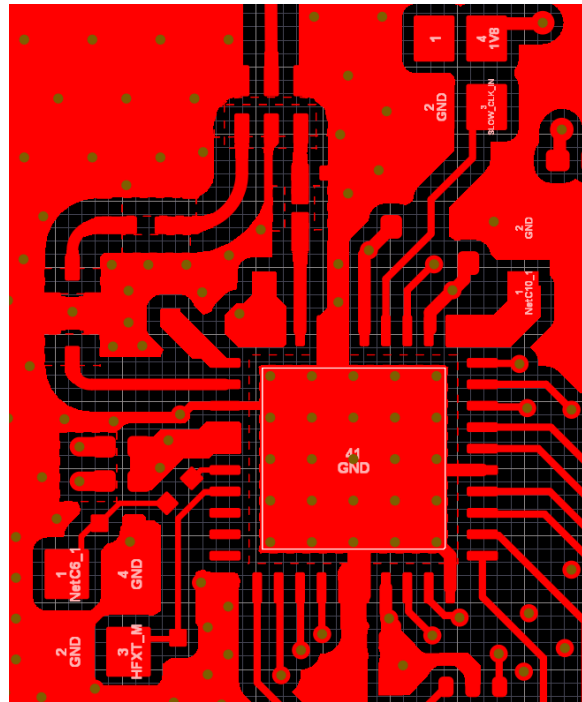


Figure 3-7. M2-CC3351 Layout, Top (Layer 1)

Figure 3-8 is sampled from the M2-CC3351 design files.

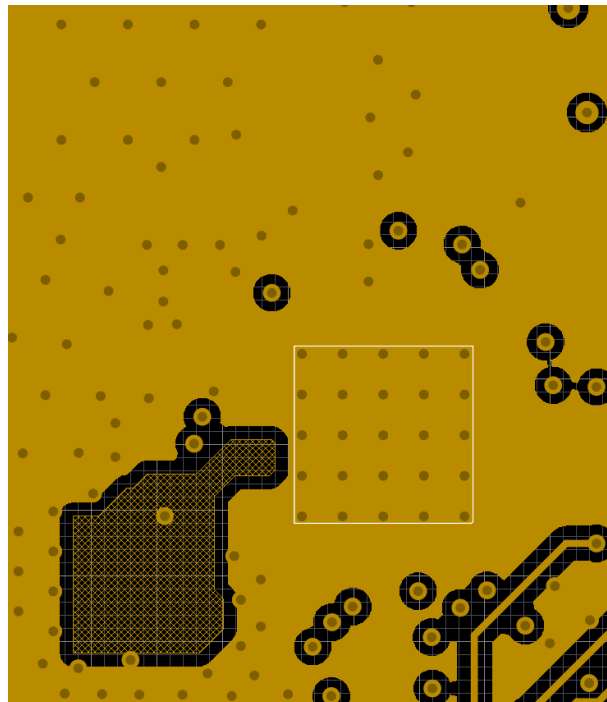
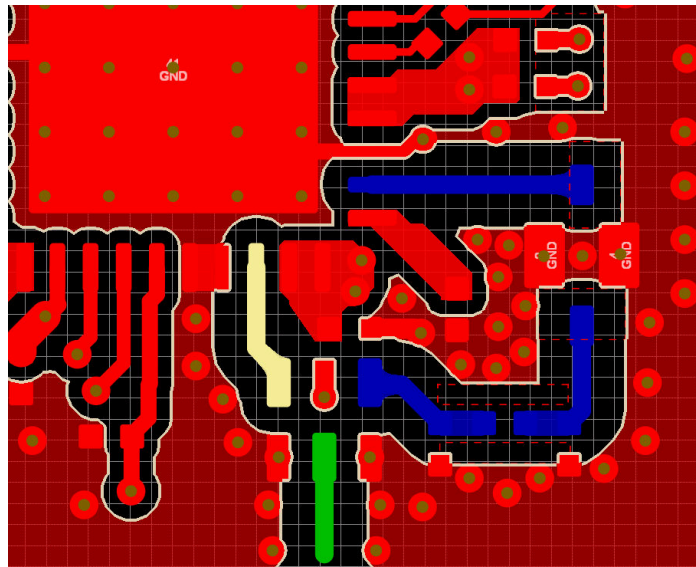


Figure 3-8. M2-CC3351 Layout, Ground (Layer 2)



Figure 3-11 is sampled from the CC335x reference design files.

In Figure 3-11, the blue traces are the RF\_BG trace (2.4GHz), the beige trace is the RF\_A trace (5GHz), and the green trace is the combined RF trace connected to the common port of the diplexer, which is routed to an antenna.



**Figure 3-11. CC335x Reference Design RF Path**

Follow the reference design as closely as possible and comply with the following list of guidelines:

#### Note

The guidelines for RF layout listed below are relevant for designs with the CC330x and CC335x devices, unless otherwise noted.

- The RF trace has a constant  $50\Omega$  characteristic impedance. This value is achieved by matching the CPWG based on the dielectric, layer stackup, ground plane spacing, and trace thickness. These parameters must remain consistent throughout the length of the trace.
- The entire RF trace is only on the top layer of the PCB, and the layer immediately underneath is one constant ground plane (with the exception of the XTAL cutout) for the trace reference.
- The RF trace is as clean and straight as possible with no components before the antenna, beside the band pass filter and matching filter. This action avoids unwanted component-to-component coupling. If a straight RF trace is not possible, rounded curves are acceptable.
- The RF trace is as isolated as possible from other components to decrease noise. Ground planes surround the RF trace, and the distance between ground through stitching is less than  $1/8$ th of the minimum wavelength.
- The band pass filter is as far as possible (within design space limits) from the RF\_BG (pin 2) pin and the VDDA decoupling capacitors on pins 4 and 5.
- A ground via is placed between the two ground pads for the band pass filter (BPF). The ground plane on both sides of the BPF is connected to enable one common ground plane for the entire area. There is increased ground through stitching in the ground plane between the BPF and the PA\_LDO\_OUT decoupling capacitor (pin 1).
- There is no high frequency signal traces or test points close to the RF trace.
- **CC335x only:** The diplexer is placed in such a way that the RF\_A trace is as short as possible (the trace connecting the RF\_A (pin 38) pin to the high port of the diplexer). The RF\_A trace takes layout priority over the RF\_BG trace when routing.
- **CC335x only:** The diplexer layout must follow the manufacturer reference design (found in the product datasheet) as close as possible, including ground vias between ground pads, for optimal diplexer performance.

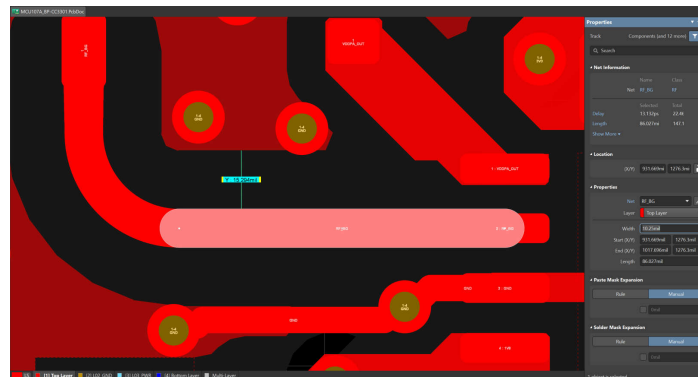
Another factor of impact in RF performance is the stackup. As an example, [Table 3-1](#) contains the stackup (from top to bottom) used in the BP-CC3351 design.

**Table 3-1. Stackup (From Top to Bottom) Used in All CC33xx EVMs**

| Layer | Name              | Thickness | $\epsilon_r$ |
|-------|-------------------|-----------|--------------|
|       | Top Soldermask    |           |              |
|       | Top Solder        | 1.00mil   | 3.5          |
| 1     | Top Layer         | 1.85mil   |              |
|       | Dielectric 1      | 5.48mil   | 4.2          |
| 2     | L02_GND           | 1.26mil   |              |
|       | Dielectric 2      | 42.82mil  | 4.2          |
| 3     | L03_PWR           | 1.26mil   |              |
|       | Dielectric 3      | 5.48mil   | 4.2          |
| 4     | Bottom Layer      | 1.85mil   |              |
|       | Bottom Solder     | 1.00mil   | 3.5          |
|       | Bottom Soldermask |           |              |

The RF signal from the device is routed to the antenna using a coplanar waveguide (CPW-G) structure. This structure offers maximum isolation across the filter gap and shielding to the RF lines. Taking into account the stackup and trace measurements is imperative for achieving a 50Ω impedance. [Figure 3-12](#) and [Figure 3-13](#) illustrate examples of calculating trace impedance using the BP-CC3351 EVM as an example.

This image is sampled from the BP-CC3351 design files.



**Figure 3-12. Example of Taking RF Trace Measurements**

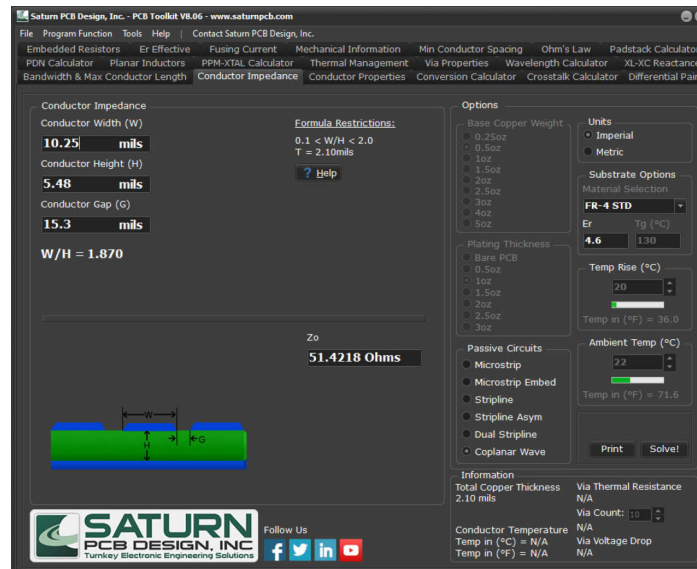


Figure 3-13. Example of Calculating Trace Impedance

### 3.4 XTAL

Figure 3-14 shows the placement and layout around the 40MHz XTAL and the connections to the CC33xx devices.

Figure 3-14 is sampled from the BP-CC3351 design files.



Figure 3-14. 40MHz XTAL From BP-CC3351

Follow the list of guidelines when integrating the XTAL:

- The traces connecting the XTAL to the CC3351 devices (XTAL\_P and XTAL\_M) is as short as possible with matching trace length.
- Place a 150Ω resistor on the XTAL\_P pin as close as possible to the CC33xx devices.
- The two loading capacitors must be parallel to the edge of the XTAL.
- On the layer below the crystal (layer 2), place a cutout underneath the area of the XTAL and the loading capacitors. Verify that the layer below layer 2 (layer 3) has good ground underneath the same area. See Figure 3-15 for a visual representation.

- Wherever possible, increase ground through stitching around the XTAL for better isolation.

Figure 3-15 is sampled from layer 3 of the M2-CC3351 design files.



**Figure 3-15. Reference Layout for Layer Under XTAL Cutout**

### 3.5 Power Supplies

The power supplies, ground traces, and decoupling capacitors are important for improving layout. Since the decoupling capacitors can be close to the RF pins and traces of the device and power supplies, traces must be thick enough to support the necessary current to the device.

- PA\_LDO\_OUT (pin 1): TI suggests placing the decoupling capacitor close to the device pin and having a thick enough trace to have a low impedance path to the capacitor. See Figure 3-16 for a visual representation.
- VDDA\_IN1 and VDDA\_IN2 (pins 4 and 5): The supply side of the decoupling capacitors must be shorted together with a polygon region with two power vias (one for each decoupling capacitor). The ground side of each capacitor must go directly to ground by separate vias (not shorted together) and be isolated from the rest of the ground plane on the top layer.
- For the 1.8V power delivery, a thick trace or power plane must be used to carry the required amount of current consumption in the VDD\_MAIN\_IN, VIO, VDDA\_IN1, VDDA\_IN2, and VPP\_IN pins combined. See Table 2-2 for maximum current consumption.
- The 1.8V path must be located around the device on a layer that is not the top layer or ground layer (place the path on layer 3 or 4). This way, the power path cannot interrupt the RF trace on the top layer (layer 1) or the continuous ground layer (layer 2). Only one via is used for each 1.8V power supply. The 1.8V supply currents must not flow under the device.
- For the 3.3V power delivery, a thick trace or a power plane must be used to carry the required amount of current consumption of the PA\_LDO\_IN pins. See Table 2-2 for more information. The power delivery must also be placed on a layer that is not the top layer or ground layer (layer 3 or 4).
- PA\_LDO\_IN (pins 39 and 40): These two pins must be shorted together with a solid region. The decoupling capacitor must be placed close to the device. Use two vias (if possible) to deliver the 3.3V rail.
- The ground for pins 37 and 38 must be shorted together with a solid region. This solid region must be connected to the thermal ground pad of the device.
- The ground for pin 3 must be shorted to the thermal pad under the device and to the ground plane that is adjacent to the RF trace.





## 4 Schematic Considerations – CC33xxMOD

The CC33xxMOD devices are designed to integrate easily with any system and require few external components. The digital interface to the host processor (MPU or MCU) is highly flexible based on the end application. Users can decide to use any combination of SDIO, SPI, or UART for shared Wi-Fi and Bluetooth Low Energy communication.

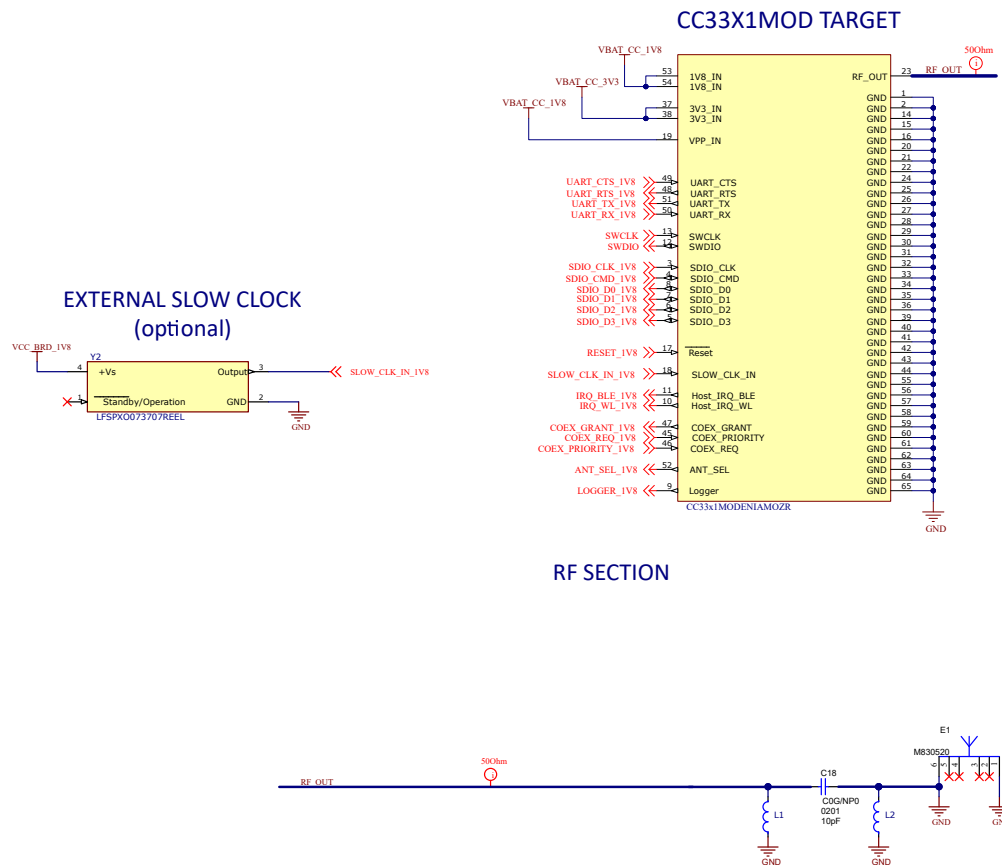
This section explains the differences between the schematic requirements for the CC33xx single chip and the CC33xxMOD pre-certified modules. All other guidance for the CC33xxMOD schematic is similar to the CC33xx devices and can be followed accordingly.

### 4.1 Schematic Reference Design – CC33xxMOD

TI recommends following the reference design and guidelines for the CC33xxMOD devices as closely as possible to achieve the full capabilities of the CC33xxMOD devices (as listed in the device-specific datasheet) and to pass certification. The schematic designs recommended for the CC33xxMOD devices are accessed here:

[CC33xxMOD Reference Design Files](#)

Figure 4-1 shows the reference schematic for the CC33xxMOD devices.



A. The slow clock can be generated internally. An external slow clock can be optionally used to consume less power than sourcing the slow clock internally.

**Figure 4-1. CC33xxMOD Reference Schematic**

### 4.2 Power Supply

There are two power rails that must be routed to the CC33xxMOD devices:

- 1.8V: 1V8\_IN, VPP\_IN
- 3.3V: 3V3\_IN

See [Section 4.2](#) for further information on the operating conditions for the supply pins.

**Table 4-1. Required Device Power**

| Pin | Signal | Direction (I/O) | Required Voltage (Typical) |
|-----|--------|-----------------|----------------------------|
| 19  | VPP_IN | I               | 1.8V                       |
| 53  | 1V8_IN | I               | 1.8V                       |
| 54  | 1V8_IN | I               | 1.8V                       |
| 37  | 3V3_IN | I               | 3.3V                       |
| 38  | 3V3_IN | I               | 3.3V                       |

## 5 Layout Considerations – CC33xxMOD

The CC33xxMOD devices are designed to integrate easily with any system and require few external components. The digital interface to the host processor (MPU or MCU) is highly flexible based on the end application. Users can decide to use any combination of SDIO, SPI, or UART for shared Wi-Fi and Bluetooth Low Energy communication.

This section explains the differences between the schematic requirements for the CC33xx single chip and the CC33xxMOD pre-certified modules. All other guidance for the CC33xxMOD layout is similar to the CC33xx devices and can be followed accordingly.

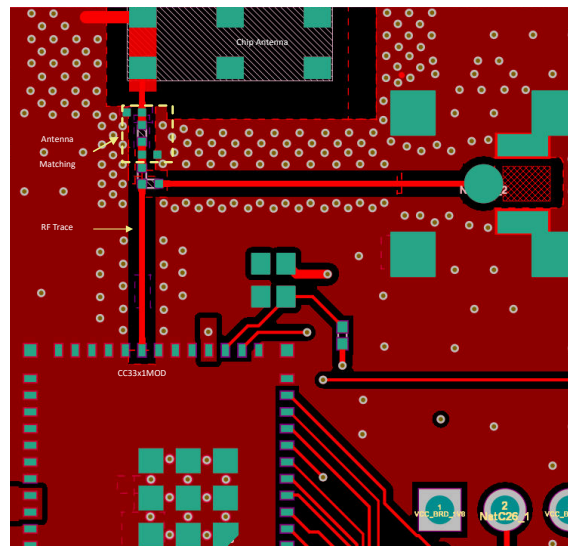
### Note

Before proceeding with any hardware build involving the CC33xxMOD devices, TI recommends reviewing the [CC33x1 Design Checklist](#) before submitting the design for [review](#).

### 5.1 CC33xxMOD RF Layout Recommendations

The RF section of this wireless module gets top priority in terms of layout. Importantly, the RF section must be laid out correctly to maintain optimum performance from the module. A poor layout can cause low-output power, EVM degradation, sensitivity degradation, and mask violations.

[Figure 5-1](#) shows the RF placement and the routing of the CC33xxMOD module with an external antenna.



**Figure 5-1. RF Section Layout**

Follow these RF layout recommendations for the CC33xxMOD devices:

- RF traces must have 50Ω impedance and must be no shorter than 9.24mm.
- RF trace bends must be made with gradual curves, and 90° bends must be avoided.
- RF traces must not have sharp corners.

- There must be no traces or ground under the antenna section.
- RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- RF traces must be as short as possible. The antenna, RF traces, and the module must be on the edge of the PCB product in consideration of the product enclosure material and proximity.

Follow the list of general layout recommendations:

- Have a solid ground plane and ground vias under the module for a stable system and thermal dissipation.
- Do not place signal traces underneath the module on a layer where the module is mounted.

## 6 CC33xxMOD Regulatory Compliance

The CC33xxMOD family of devices are designed to be easy to use and enhance the time to market for customers.

Follow these high-level steps to complete integration:

1. Design your carrier PCB following:
  - The design guidelines listed in the [Important Notice to OEM integrators](#) .
  - Using an antenna from our [Antenna Installation Guidelines](#).
2. Evaluate the regions where you plan to ship your product and determine the appropriate regulatory bodies:
  - For regions with a pre-existing TI certification:
    - a. TI modules are designed to enable easy reuse of certification.
    - b. Full integration steps depend on the region, but in most use-cases, integration is limited to paperwork or spot checking for compliance.
  - a. For other regions:
    - Work with the appropriate regulatory body to determine the steps for compliance.

Reports for the CC33xxMOD can be found on the [SIMPLELINK-CC33XX-REPORTS](#) page.

IDs are listed in [Table 6-1](#) and [Table 6-2](#):

**Table 6-1. CC330xMOD Certification**

| Model Name | Regulatory Body | ID                                     |
|------------|-----------------|--|
| CC33MOD    | FCC             | Z64-CC33SBMOD                          |
|            | ISED            | 4511-CC33SBMOD                         |
|            | CE / ETSI       | N/A                                    |
|            | Japan / TELEC   | 201-250389 (Test Grade: 01, CC3301MOD) |
|            | Japan / TELEC   | 201-250390 (Test Grade: 00, CC3300MOD) |

**Table 6-2. CC335xMOD Certification**

| Model Name | Regulatory Body | ID                                     |
|------------|-----------------|--|
| CC33MOD-DB | FCC             | Z64-CC33DBMOD                          |
|            | ISED            | 4511-CC33DBMOD                         |
|            | CE / ETSI       | N/A                                    |
|            | Japan / TELEC   | 201-250530 (Test Grade: 51, CC3351MOD) |
|            | Japan / TELEC   | 201-250531 (Test Grade: 50, CC3350MOD) |

To leverage the IDs in [Table 6-1](#) and [Table 6-2](#) at a regulatory test facility, TI recommends submitting a [Module Certification Request](#) form and obtaining a letter of authorization from TI for FCC and ISED.

### 6.1 CC33xxMOD OEM Integration Manual

#### Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).

3. Refer to the datasheet for the device for trace design instruction. As a module using trace design, this module relies on the manufacturers of the host product to prepare the antenna connector. A unique antenna connector must be used on the Part 15 authorized transmitters used in the host product. The module manufacturer provides a list of acceptable unique connectors (see [Table 6-4](#)).
4. Separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations.
5. For FCC Part 15.31 (h) and (k): The manufacturer of the host product is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the manufacturer of the host product is required to show compliance with Part 15 Subpart B while the transmitter module (or modules) are installed and operating. The modules must be transmitting, and the evaluation must confirm that the intentional emissions of the module are compliant (for example, fundamental and out of band emissions). The manufacturer of the host product must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are compliant with the rules of the transmitter (or transmitters).

### Antenna Installation

- (1) The antenna must be installed such that 20cm is maintained between the antenna and users.
- (2) The transmitter module cannot be co-located with any other transmitter or antenna.
- (3) Only antennas of the same type and with equal or less gains (see [Table 6-4](#)) can be used with this module. Other types of antennas and higher gain antennas possibly require additional authorization for operation.

**Table 6-3. CC330xMOD Certified Antenna List**

| Brand       | Part Number | Antenna Type |
|-------------|-------------|--------------|
| Kyocera AVX | M830520     | Chip antenna |

**Table 6-4. CC335xMOD Certified Antenna List**

| Brand          | Part Number          | Antenna Type                |
|----------------|----------------------|-----------------------------|
| Kyocera AVX    | M830520              | Chip antenna                |
| Kyocera AVX    | W4P42X8W04-U100D3B0A | External PCB antenna        |
| TDK            | ANT162442DT-2001A2   | Chip antenna                |
| Yageo/Pulse    | ANT3216A063R2455A    | Chip antenna                |
| Yageo/Pulse    | W5028T               | Dipole(stick) antenna       |
| Yageo/Pulse    | W3078T               | Monopole(ceramic) antenna   |
| Yageo/Pulse    | W3917B0100T          | Dipole(flexible PC) antenna |
| Molex          | 204281-1100          | External PCB antenna        |
| Molex          | 146153-1100          | External PCB antenna        |
| Molex          | 204281-0100          | External PCB antenna        |
| Molex          | 146153-0100          | FPC                         |
| Unictron       | H2B1PD1A1C385L       | External PCB antenna        |
| Unictron       | H2B1PC1A1C095L       | External PCB antenna        |
| Laird          | WTS2450              | Whip antenna                |
| TEConnectivity | 001-0012             | Whip antenna                |
| Chang Hong     | DA-2458-02           | Whip antenna                |
| Ezurio         | 001-0016             | Flex PIFA                   |

#### Note

**CC330xMOD is only certified with the M830520 antenna. CC335xMOD does support all of the antennas in [Table 6-4](#).**

## End Product Labeling

To comply with the CC330xMOD or CC335xMOD modular approval for use in Canada and the United States, OEM/Host manufacturers must include the following example label as shown in [Figure 6-1](#) and [Figure 6-2](#) on end-product and user manual:

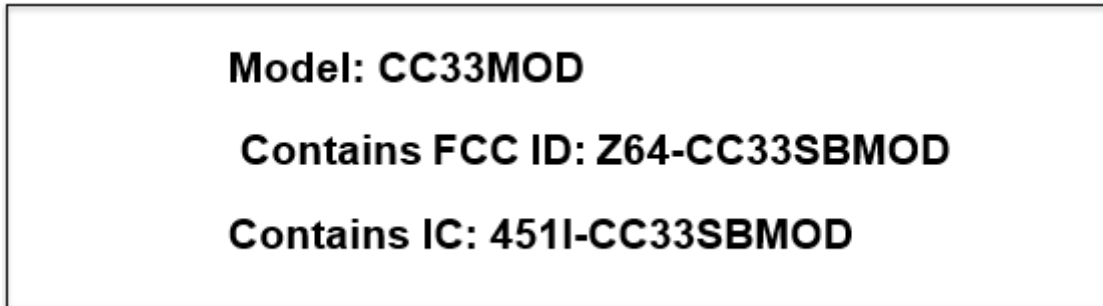


Figure 6-1. CC330xMOD End Product Labeling

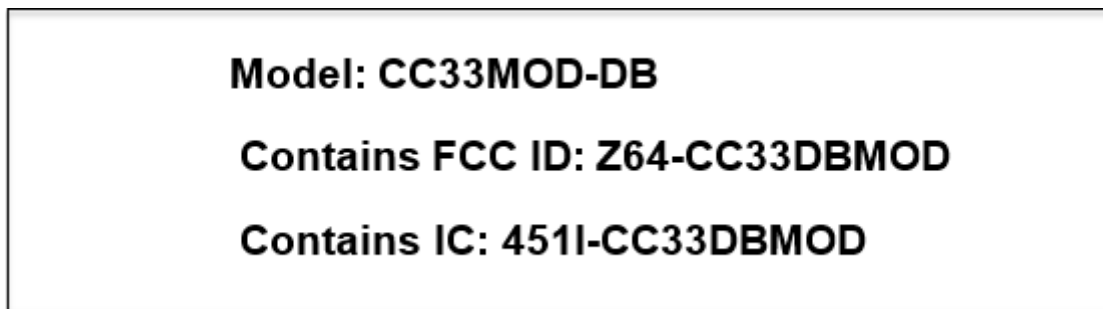


Figure 6-2. CC335xMOD End Product Labeling

## EMI Considerations

Refer to KDB 996369 D04 and D02 for guidance regarding compliance of the host device.

## Information to Make Changes

Only Grantees are permitted to make permissive changes. Please contact TI if the host integrator expects the module to be used differently than as granted: [connectivity-wifi-cert@list.ti.com](mailto:connectivity-wifi-cert@list.ti.com)

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from January 9, 2026 to June 17, 2026 (from Revision A (January 2026) to Revision B (June 2026))

|   | Page |
|---|------|
| • Added schematic figure note.....  | 4    |
| • Updated Layout Considerations.....  | 18   |
| • Added additional CC335x only bullet.....  | 23   |
| • Updated Layout Considerations.....  | 31   |
| • Changed the ISED ID from 461I-CC33DBMOD to 451I-CC33DBMOD. Updated Regulatory Compliance section..... | 32   |
| • Added OEM Integration Guidance.....   | 32   |

### Changes from December 14, 2023 to January 8, 2026 (from Revision \* (December 2023) to Revision A (January 2026))

|  | Page |
|--|------|
| • Updated with module information.....   | 3    |
| • Removed links and added tables.....  | 3    |
| • Added additional schematic information.....  | 4    |
| • Removed the <i>Power-Up Sequence</i> section.....                                  | 7    |
| • Added the <i>Boot Sequence</i> section.....  | 7    |
| • Added additional content for a dual band configuration.....                        | 10   |
| • Added the <i>WLAN Interrupt Request (HOST_IRQ_WL)</i> section.....                 | 16   |
| • Added the <i>Logger</i> section.....   | 16   |
| • Added the <i>Schematic Considerations – CC33xxMOD</i> section and subsections..... | 30   |
| • Added the <i>Layout Considerations – CC33xxMOD</i> section and subsections.....    | 31   |
| • Added the <i>CC33xxMOD Regulatory Compliance</i> section and subsections.....      | 32   |
| • Added module information.....  | 32   |

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