TPS659112 Netra User Guide

This document is a user guide for integrating the TPS659112 power-management integrated circuit (PMIC) with the DM816x, C6A816x, and AM389x application processors.

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1 Introduction

This document describes connectivity between the DM816x, C6A816x, and AM389x processors and PMIC. It also describes TPS659112 EEPROM bit configuration that is programmed to support power-up sequence requirements of DM816x, C6A816x, and AM389x processors. For details of the PMIC features and performance, refer to the full specification document, *TPS65911 Data Manual*.

2 Platform Connection

Figure 1 shows the connection between the DM8168 application processor and the TPS659112.

The following notes to the connection diagram shown in Figure 1:

- TPS659112 starts the power-up sequence upon insertion of a 5-V input to VCC7.
- VCCS must be > 3 V for the power-up sequence to proceed.
- The voltage level of the TPS659112 I/O control signals (I2C, INT1, EN1, EN2, NRESPWRON) is defined by the VDDIO input, which is connected to the 3.3-V VIO.
- The VDD1 connections are shown based on the assumption that the CVDDC load current is > 1.5 A and VDD1 is not used. VDD1 is still included in the TPS659112 power-up sequence for potential future use. To minimize power consumption, VDD1 should be set to off by software (300 µA of extra consumption if VDD1 is left on).
- The LDO connection for peripheral a I/O is an example. Depending on the system requirements, each peripheral I/O can be connected to an LDO at the required level. Only LDO1 and LDO2 are powered-up during the initial power-up sequence; the other LDOs are enabled by software I^2C™ access.
- INT1 is an optional interrupt output from the TPS659112 to the processor. An interrupt is generated for example from

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  - PMIC die temperature increase (prewarning before thermal shutdown)
  - GPIO events
  - Button press event to the PWRON pin
-
- Voltage scaling for CVDD is supported through the main I^2C (SDA_SDI and SCL_SCK). EN1 and EN2 (dedicated SmartReflex™ I^2C interface) is not connected.
- PWRHOLD is programmed as a general-purpose input in the TPS659112. If PWRHOLD is not used, it can be left floating.
- CLK32KOUT is generated from the TPS659112 internal RC oscillator.
- If a backup battery is not used, VBACKUP should be connected to VCC7.
- GPIO0 is a push-pull output. The output high level is defined by VCC7.
- GPIO7 was not available on TPS659112 samples delivered before July 1st 2011 and should be left floating in this case.
- GPIO2 and GPIO7 are open-drain outputs and need an external pull-up. These GPIOs can to actively pull the output low after 4 ms from the VCC7 input supply insertion.

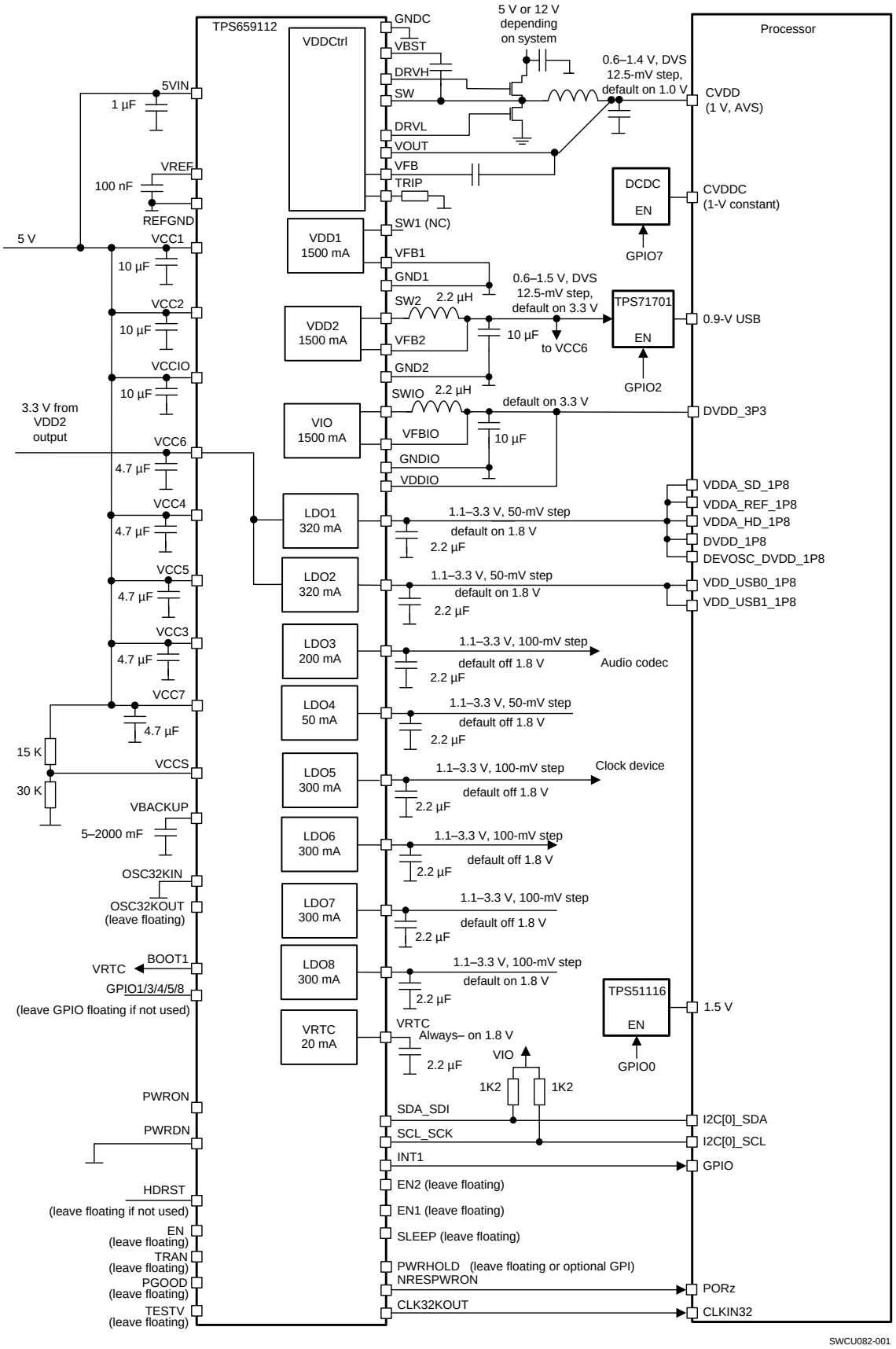

Figure 1. Processor Power Supply Connections With TPS659112

3 Power-Up Sequencing

Power-up sequence matching processor is programmed on TPS659112 EEPROM. Figure 2 shows the power-up sequence.

NOTE: GPIO7 was not available on TPS659112 samples delivered before July 1, 2011.

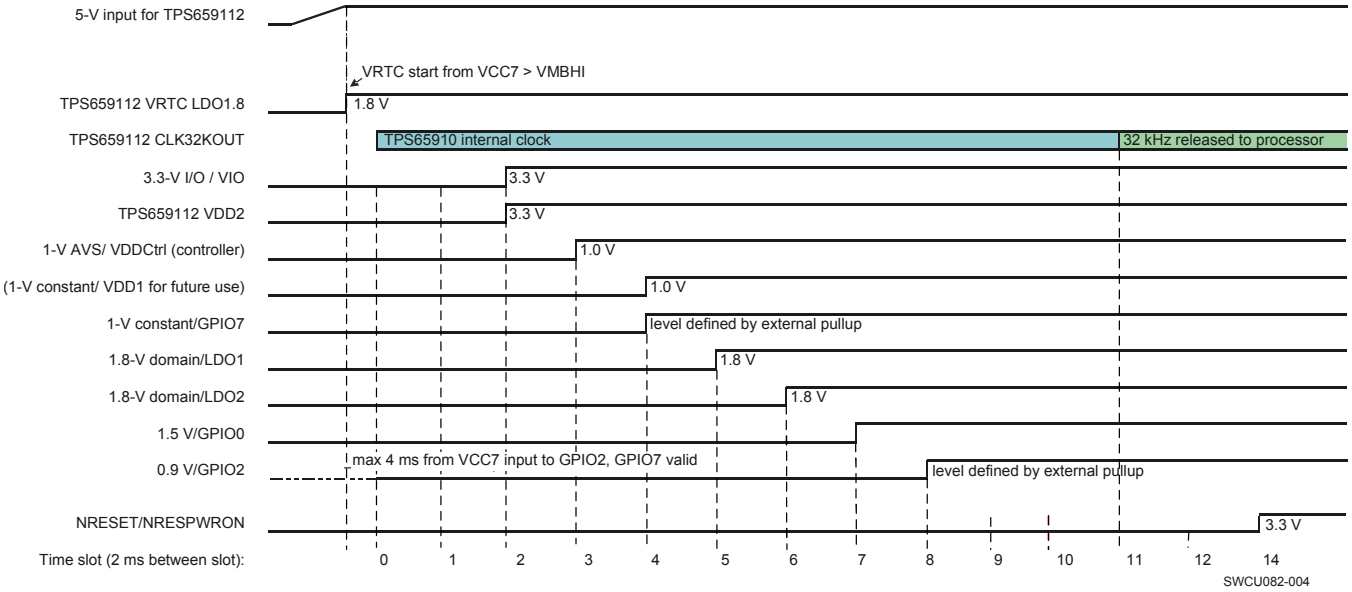

Figure 2. Power-Up Sequence Timing Diagram

Table 1 lists the EEPROM values for the TPS659112.

Table 1. EEPROM Configuration for TPS659112 Power-Up Sequence

Register	Bit	Description	Option Selected
VDD1_OP_REG/VDD1_SR_REG	SEL	VDD1 voltage level selection for boot	1.0 V
VDD1_REG	VGAIN_SEL	VDD1 gain selection, x1 or x2	x1
EEPROM		VDD1 time slot selection	4
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG / VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.1 V
VDD2_REG	VGAIN_SEL	VDD2 gain selection, x1 or x3	x3
EEPROM		VDD2 time slot selection	2
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	3.3 V
EEPROM		VIO time slot selection	2
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled
VDDCtrl_OP_REG / VDDCtrl_SR_REG		VDDCtrl voltage level selection for boot	1.0 V
EEPROM		VDDCtrl time slot selection	3
LDO1_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	5
LDO2_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	6
LDO3_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
LDO4_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
LDO5_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
LDO6_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
LDO7_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
LDO8_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
CLK32KOUT pin		CLK32KOUT time slot	11
NRESPWRON, NRESPWRON2 pin		NRESPWRON time slot	14
GPIO0 pin		GPIO0 time slot	7
GPIO2 pin		GPIO2 time slot	8
GPIO6 pin		GPIO6 time slot	OFF
GPIO7 pin		GPIO7 time slot	4

Table 2. EEPROM Configuration for TPS659112, Control Bits

Register	Bit	Description	Option Selected
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO will be in low-power mode during OFF state. 1 = VRC LDO will be in full-power mode during OFF state.	Low-power mode
DEVCTRL_REG	DEV_ON	0 = No impact 1 = Will maintain device on, in ACTIVE and SLEEP state	1
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is crystal/external clock. 1 = Clock source is internal RC oscillator.	RC
DEVCTRL2_REG	TSLOTD	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	2 ms
DEVCTRL2_REG	PWON_LP_OFF	0 = Turn off device after PWRON long press not allowed 1 = Turn off device after PWRON long press	0
DEVCTRL2_REG	PWON_LP_RST	0 = No impact 1 = Reset digital core when device is off	0
DEVCTRL2_REG	IT_POL	0 = INT1 signal will be active low. 1 = INT1 signal will be active high.	Active low
INT_MSK_REG	VMBHI_IT_MSK	0 = Device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = Start-up is reason required before switch-on.	0 = Automatic switch-on from supply insertion
INT_MSK3_REG	GPIO5_F_IT_MSK	0 = GPIO5 falling edge detection interrupt not masked 1 = GPIO5 falling edge detection interrupt masked	1
INT_MSK3_REG	GPIO5_R_IT_MSK	0 = GPIO5 rising edge detection interrupt not masked 1 = GPIO5 rising edge detection interrupt masked	0
INT_MSK3_REG	GPIO4_F_IT_MSK	0 = GPIO4 falling edge detection interrupt not masked 1 = GPIO4 falling edge detection interrupt masked	1
INT_MSK3_REG	GPIO4_R_IT_MSK	0 = GPIO4 rising edge detection interrupt not masked 1 = GPIO4 rising edge detection interrupt masked	0
GPIO0_REG	GPIO_ODEN	0 = GPIO0 configured as push-pull output 1 = GPIO0 configured as open drain-output	Push-pull
WATCHDOG_REG	WATCHDOG_EN	0 = Watchdog disabled 1 = Watchdog enabled	0
VMBCH_REG	VMBBUF_BYPASSS	0 = Enable input buffer for external resistive divider 1 = In single-cell system, disable buffer for low power	Enable buffer
VMBCH_REG	VMBCH_SEL[5:1]	Select threshold for boot gating comparator COMP1	3 V
EEPROM	AUTODEV_ON	0 = PWRHOLD pin is used as PWRHOLD feature. 1 = PWRHOLD pin is a GPI. After power on, DEV_ON set high internally, no processor action needed to maintain supplies	1
EEPROM	PWRDN_POL	0 = PWRDN signal is active low 1 = PWRDN signal is active high	Active high

4 Getting Started with TPS659112

4.1 First Initialization

4.1.1 Power-Down Sequence Configuration

To meet processor power-down sequence requirements, select the reverse sequence by setting the PWR_OFF_SEQ bit to 1 in the DEVCTRL_REG register.

4.1.2 I/O Polarity/Muxing Configuration

Voltage scaling for VDD1, VDD2, and VDDCtrl can be done either through the main I^2C interface or through dedicated interface EN1/EN2. Refer to the processor documentation for information on which one is supported. To enable the dedicated voltage scaling interface, set the SR_CTL_I2C_SEL bit to 0 in the DEVCTRL_REG register.

If sleep mode is supported, program the SLEEPSIG_POL bit in the DEVCTRL2_REG register according to the GPIO from the processor. This can be set to active-low or active-high for SLEEP transitions. Software can configure specific power resources to enter the LOW-POWER or OFF state in sleep mode.

In the DEVCTRL_REG register, set the DEV_SLP bit to 1 to allow the SLEEP transition when requested through the SLEEP pin.

Update the GPIOx configuration (GPIOx_REG) based on the specification needs.

4.1.3 Define Wake Up/Interrupt Event (SLEEP or OFF)

Select the appropriate bits in the INT_MSK_REG, INT_MSK2_REG, and INT_MSK3_REG registers to activate an interrupt to the processor on the INT1 line.

4.1.4 Backup Battery Configuration

If the system has backup battery, set the BBCHEN bit to 1 in the BBCH_REG register to enable backup battery charging. The maximum voltage can be set based on backup battery specifications by using the BBSEL bits in the BBCH_REG register.

4.1.5 DCDC Maximum Current Capablity

In VIO_REG, VDD1_REG and VDD2_REG, set the ILMAX bit according to the required maximum current.

4.1.6 Sleep Platform Configuration

Configure the state of the DC-DCs and LDOs when the SLEEP signal is used. By default, in sleep mode all resources maintain their output voltage and load capability, but response to transients (load change) is reduced.

Resources that must provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG and SLEEP_KEEP_RES_ON_REG registers.

Resources that can be set to off in the SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG and SLEEP_SET_RES_OFF_REG registers.

4.2 Event Management Through Interrupts

This section describes the TPS659112 interrupts.

4.2.1 INT_STS_REG.VMBHI_IT

The VMBHI_IT interrupt bit indicates that a supply (VBAT) is connected (PMIC leaving the BACKUP or NO SUPPLY state) and the system must be initialized (see Section 4.1, *First Initialization*).

4.2.2 INT_STS_REG.PWRON_IT

The PWRON_IT interrupt bitis triggered by pressing the PWRON button. If the device is in the OFF or SLEEP state, then this acts as a wake-up event and resources are reinitialized.

4.2.3 INT_STS_REG.PWRON_LP_IT

The PWRON_LP_IT interrupt bit is the PWRON long-press interrupt. This interrupt is generated when the PWRON button is pressed for 4 seconds. The application processor can make a decision to acknowledge the interrupt. If this interrupt is not acknowledged within the next second, the device interprets this as a power-down event.

4.2.4 INT_STS_REG.HOTDIE_IT

The HOTDIE_IT interrupt bit indicates that the temperature of the die is reaching the limit. The software must take action to decrease the power consumption before automatic shutdown.

4.2.5 INT_STS_REG.PWRHOLD_R/F_IT

The PWRHOLD_R/F_IT interrupt bit indicates a GPI interrupt event.

4.2.6 INT_STS_REG.RTC_ALARM_IT

The RTC_ALARM_IT interrupt bit is triggered when the RTC alarm set time is reached.

4.2.7 INT_STS2(3)_REG.GPIO_R/F_IT

The GPIOx_R/F_IT interrupt bit indicates a GPIO1, GPIO2 or GPIO3 interrupt event. It can be used to wake up the device from SLEEP state. This can be an interrupt coming from any peripheral device or alike.

4.2.8 INT_STS3_REG.PWRDN_IT

The PWRDN_IT interrupt bit is triggered when PWRDN reset is detected.

4.2.9 INT_STS3_REG.VMBDCH2_H/L_IT

The VMBDCH2_H_IT or VMBDCH2_L_IT interrupt bit is triggered when comparator 2 input (VCCS) is above or below the threshold, respectively.

4.2.10 INT_STS3_REG.WATCHDOG_IT

The WATCHDOG_IT interrupt bit is triggered from the watchdog (periodic or interrupt mode).

5 Revision History

The following table summarizes the TPS659112 Netra User Guide versions.

Note: Numbering may vary from previous versions.

Version	Literature Number	Date	Notes
*	SWCU082	August 2011	See (1)
A	SWCU082A	October 2012	See (2)

(1) SWCU082 – Initial release

(2) SWCU082A –
- Update Figure 1

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