EVM User's Guide: SK-AM69

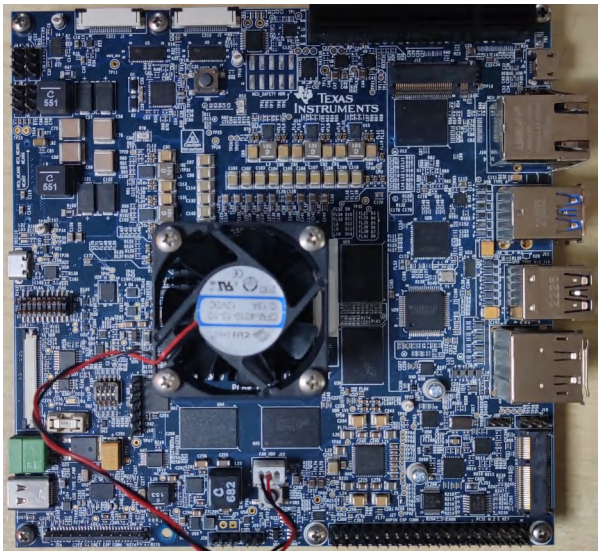
AM69 Processor Starter Kit Evaluation Module

Description

The SK-AM69 starter kit evaluation module (EVM) is based on the AM69x artificial intelligence (AI) vision processor, which includes an image signal processor (ISP) supporting up to 1440MP/s, 32 tera-operations-per-second (TOPS) AI accelerator, eight 64-bit Arm® Cortex® A72 microprocessor, and H.264/H.265 video encode/decode. The SK-AM69x is a practical choice for machine vision, traffic monitoring, retail automation, and factory automation.

Get Started

1. Order EVM at SK-AM69.
2. Download the EVM Design Files.
3. Download the software.
4. Read this user's guide.



Features

- Performance: AM69 processor enables 32 TOPS deep-learning performance and hardware-accelerated edge AI at low power
- Camera interfaces: three CSI-2 ports compatible with Raspberry Pi or a high-speed 40-pin Samtec® camera connector allowing up to twelve cameras (requires multi-camera hub)
- Connectivity: three SuperSpeed® USB Type-A ports, one SuperSpeed USB Type-C™ port, one Ethernet port, one M.2 key E connector and one M.2 key M connector, four CAN-FD interfaces, four UART terminals over one USB bridge
- Memory: four DRAM, LPDDR4-4266, 32 gigabytes total memory, support for inline ECC
- Display: DisplayPort with up to 4K resolution with MST support and 1080 HDMI

This design incorporates HDMI® technology.

1 Evaluation Module Overview

1.1 Introduction

The starter kit (SK) includes two RPI 22-Pin CSI connectors and two MIPI CSI-2 40-Pin expansion connectors for up to 12 cameras, making the kit practical for a variety of embedded vision and AI applications on the edge. Our ISP can handle different lighting conditions in video streams by using HDR encoding for camera support. Our deep-learning accelerator enables classification and object detection at low latency and high frame rate.

Processor SDK AM69A software development kit (SDK) supports Linux application development. On-chip emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ (CCS).

1.2 Kit Contents

The SK-AM69 Processor Starter Kit includes:

- AM69 Starter Kit EVM
- Micro-SD card
- USB cable (Type-A to Micro-B) for serial terminal and logging
- Paper card with start-up link and support information

The EVM is powered from a Type-C power supply, but the power supply is *not included*. For more information on the types of supplies recommended with the EVM, see Table 2-1.

The orderable part number of the EVM is: SK-AM69.

1.3 Specification

- Processor
  - Texas Instruments AM69 Super-Set device
- Optimized Power Management Design
  - Dynamic Voltage Scaling
  - Multiple Clock and Power Domains
- Memory
  - 4x 8GByte LPDDR4 DRAM (2133MHz)
  - 512Mb Non-Volatile Flash, Octal-SPI NOR
  - 32GB eMMC, version 5.1 compliant
  - Multimedia Card (MMC)/Secure Digital Card (Micro SD) Cage, UHS-I
- USB
  - USB3.1 (Gen1) Hub to 3x Type A (Host)
  - USB3.1 (Gen1) Type C (DFP modes)
  - USB2.0 Micro B (for Quad UART-over-USB Transceiver)
- Display
  - VESA Display Port (v1.4), supports 4K UHD with MST support
  - DVI (v1.0) through HDMI Type A, supports 1080p
- Wired Network
  - Gigabit Ethernet (RJ45 Connector)
  - 4x CAN-FD Headers (1x3)
- Camera Interfaces
  - 2x 22-Pin Flex Cable Interface (CSI-4L)
  - 2x 40-pin High Speed Connector (dual CSI-4L, I2C, General-Purpose Input/Output (GPIO), and so forth)
- Expansion/Add-on
  - M.2 Key M Interface (PCIe/Gen3x 2 Lane)
  - M.2 Key E Interface (PCIe/Gen3x 1 Lane)
  - Standard x8 PCIe Interface (Gen3x 4 Lane)
  - 60-pin ENET expansion header SGMII Interface
  - 40-pin Header (2x20) (Inter-Integrated Circuit (I2C), Serial Peripheral Interface (SPI), Universal Asynchronous Receiver/Transmitter (UART), Inter-IC Sound (I2S), GPIO, Pulse Width Modulator (PWM), and so forth)

  - Fan Header (12V)
- User Control/Indication
  - Pushbuttons (Reset, Power/User Defined)
  - LEDs (Power, User Defined, Serial Port)
  - User Configuration (Boot Mode)
  - On board Emulator Support (XDS110) with optional external support (20-pin header)
- REACH and RoHS Compliant
- EMI/EMC Radiation Compliant

1.4 Device Information

Function: Define Info

Processor, SoC: AM69A

Power Management, SoC: TPS6594133A

Power Regulator, SoC: TPS62873-Q1

CAN-FD Bus transciver: TCAN1462V-Q1

Emulator (XDS110): TM4C1294NCPDT

Ethernet PHY, 1Gb: DP83867E

Power Monitor: INA226-Q1

Power Regulator: LM5143-Q1

Power Regulator: LM61460-Q1

USB Hub Controller: TUSB8041-Q1

USB Power Controller: TPS25750

USB Type-C Controller: TUSB321

2 Hardware

2.1 User Interfaces

Figure 2-1 and Figure 2-2 identify the key user interfaces on the AM69 Processor SK (top and bottom view).

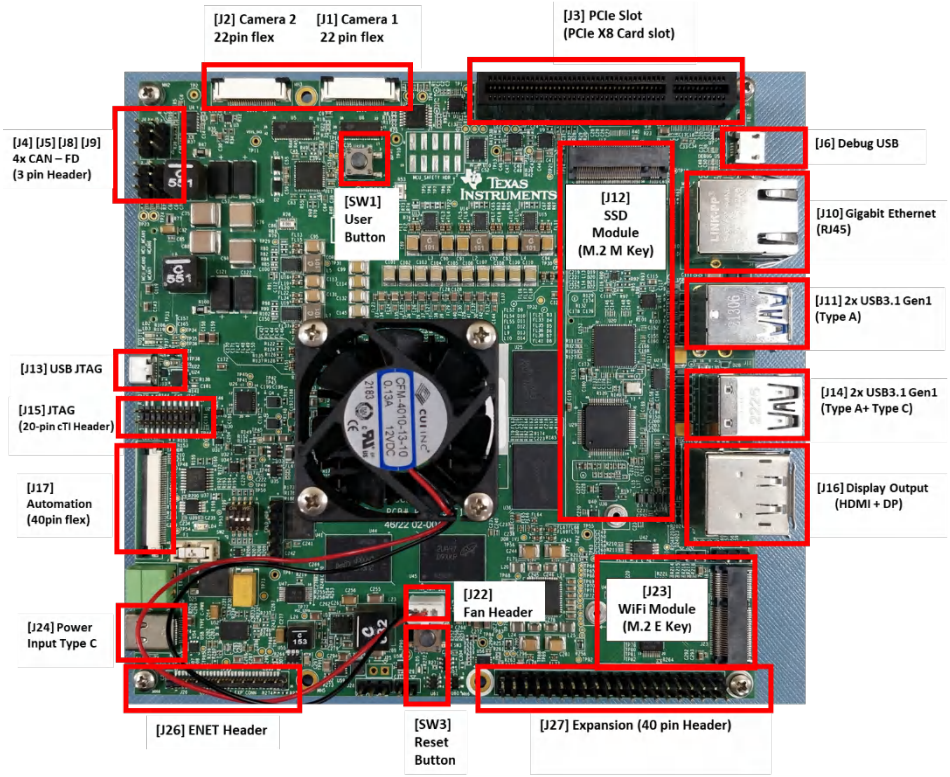


Figure 2-1. User Interfaces (Top)

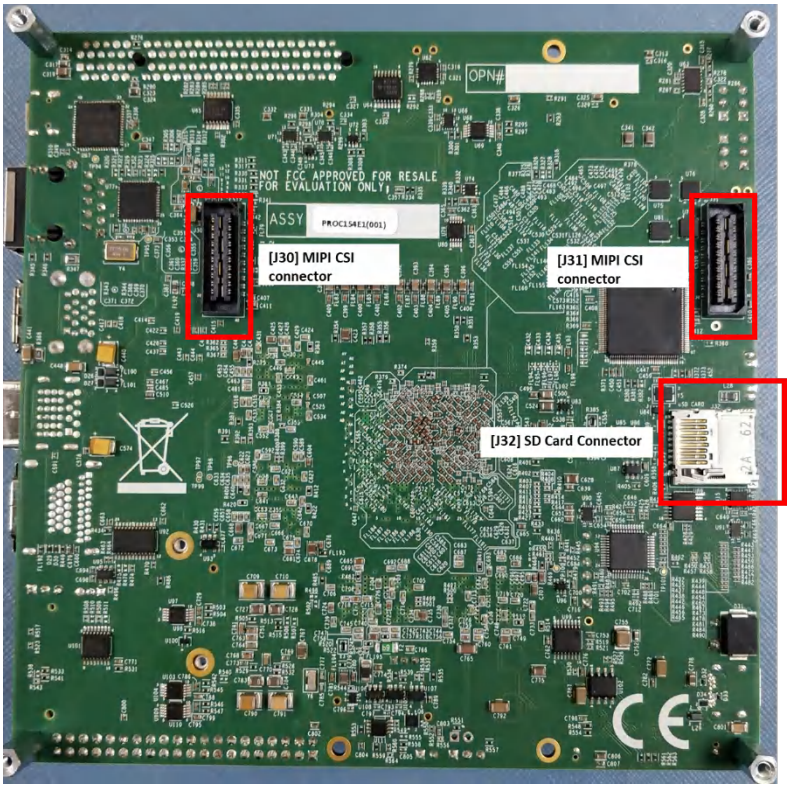


Figure 2-2. User Interfaces (Bottom)

2.1.1 Power Input

A power supply is not included with the SK and must be purchased separately.

External Power Supply or Power Accessory Requirements:

- Nominal Output Voltage: 5-20VDC
- Maximum Output Current: 5000mA
- Efficiency Level V

Note

TI recommends using an external power supply or power accessory that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, and so forth.

2.1.1.1 Power Input [J24] With LED for Status [LD4]

The dedicated power input connector is a USB Type C connector [J24] with Power Delivery 3.0 support. The input can accept wide range of input voltages (5V to 20V). The exact power required for the SK is largely dependent on the application and the connected peripherals. The recommended supplies are listed in Table 2-1. These supplies are 20V Type C supplies capable of supplying up to 100W of power (20VDC at 5A). The minimum supply required is 60W supply (20VDC at 3A). However, a 60W supply can limit available processing with processor as well as limit some of the available peripherals. USB and PCIe peripherals can require significant power and this is a reason higher wattage supply is recommended.

There are many USB Type C power supply manufactures and models available in the market, and testing the SK with every combination is not possible.

Table 2-1 lists a few recommended supplies the SK has tested.

Table 2-1. Recommended External Power Supply

Manufacturer	Part # / Model #	Description	Ordering Information
Dell	450-AJWU	Dell USB-C 90W AC Adapter	Link
Asus	AC100-00(A20-100P1A)	ROG 100W USB-C Adapter	Link

Table 2-1. Recommended External Power Supply (continued)

Manufacturer	Part # / Model #	Description	Ordering Information
GlobTek, Inc.	TR9CZ3000USBCG2R6BF2	AC/DC DESKTOP ADAPTER 5V-20V 60W	1939-1794-ND [Digikey part #]
Qualtek	QADC-65-20-08CB	AC/DC DESKTOP ADAPTER 20V 65W	Q1251-ND [Digikey part #]

2.1.1.2 Power Budget Considerations

The exact power required for the SK is largely dependent on the application, usage of the on-board peripherals, and power needs of add-on devices. Table 2-2 shows the power allocations of the design. (Again, the input supply must be capable of supplying the power needs for your application).

Table 2-2. Power Supply Allocation

Function	Power	Description
Processor Core	Up to 50W	Processor, Memory
On-board Peripherals	Up to 3W	SD card, Ethernet, Logic, and so forth
USB Ports	Up to 19W	USB Hub Type A Ports (2.8A at 5V) Type C Port (1.5A at 5V)
Camera Ports	Up to 2W	Cam Ports (0.5A at 3.3V)
Expansion Interfaces	Up to 40W	M.2 Type E (1A at 3.3V) M.2 Type M (3A at 3.3V) PCIe Card Slot (2A at 12V, 3A at 3.3V) 40p Expansion(2A at 3.3V,1.5A at 5V)
Displays	Up to 3W	HDMI Transceiver HDMI Panel(55mA at 5V) DP Panel (0.5A at 3.3V)

2.1.2 User Inputs

The EVM supports several mechanisms for the user to configure, control, and provide input to the system.

2.1.2.1 Board Configuration Settings [SW2]

Dip Switch [SW2] is used to configure different options available on the SK, including processor boot mode.

Table 2-3. Processor Bootmode Settings [SW2 Switch 1-3]

Processor Boot Source	SW2.1	SW2.2	SW2.3
MicroSD Card [J32]	OFF	OFF	OFF
Non-Volatile Flash (xSPI)	OFF	OFF	ON
eMMC	OFF	ON	ON
Reserved	OFF	ON	ON
UART (for Flashing)	ON	OFF	ON
No Boot (JTAG/Emulator)	ON	OFF	OFF
Ethernet[J10]	OFF	ON	OFF

2.1.2.2 Reset Pushbutton [SW3]

When pressed [SW3], the SK is issued a Power-On (Cold) Reset, and is held in reset until the button is released.

If the pushbutton is held longer than five seconds, the system powers down. The system can be restarted by either pressing the User Pushbutton [SW1] or by cycling power to the board.

2.1.2.3 User Pushbutton [SW1] With User LED Indication [LD5]

The pushbutton [SW1] can be used for several different functions.

Function 1: System Wake from Shutdown. After software-initiated power down (using WKUP_GPIO0_69), pressing pushbutton [SW1] re-enables and boots the SK.

Function 2: Power Management Enable. The pushbutton [SW1] is connected with Power Management IC (nPWRON/ENABLE), and used for enabling the SOC supplies

Function 3: User Defined Input/Interrupt. The pushbutton [SW1] is connected with the processor (WKUP_GPIO0_82), and can be programmed for variety of user input and interrupt needs.

A red LED [LD5] is available as user indicator, and is controlled through the processor (WKUP_GPIO0_55).

2.1.3 Standard Interfaces

The EVM provides industry standard interfaces and connectors to connect a wide variety of peripherals. Because these interfaces are standard, specific pin information is not provided in this document.

Note

The maximum length for any IO cables are required to be less than three meters.

2.1.3.1 UART-Over-USB [J6] With LED for Status [LD1]

Four UART ports of the processor are interfaced with UART-over-USB transceivers. When the USB micro-B connector (J6) of the EVM is connected to a Host-PC using supplied USB cable (Type-A to Micro-B), the computer can establish Virtual Com Ports which can be used with any terminal emulation application. Virtual Com Port drivers for the transceiver (CP2108B02-GM) can be obtained from here.

Once installed, the Host-PC creates four Virtual Com Ports. Depending on the other Host-PC resources available, the Virtual COM Ports can not be located at COM1-4. However, the ports remain in the same numerical order.

Table 2-4. UART to COM Port Mapping

AM69 UART	Host-PC COM Port
WKUP_UART0	COM 1
MCU_UART0	COM 2
UART8	COM 3
UART2	COM 4

The circuit is powered through BUS power, therefore the COM connection is not lost when the EVM power is removed. An LED [LD1] is used to indicate an active COM connection with Host-PC.

2.1.3.2 Gigabit Ethernet [J10] With Integrated LEDs for Status

A wired Ethernet network is supported on the base board via RJ45 cable interface [J10], and is compatible with IEEE 802.3 10BASETe,100BASE-TX, and 1000BASE-T specifications. The connector includes status indicators for link and activity.

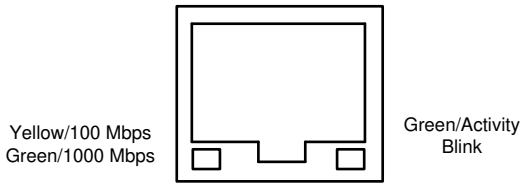


Figure 2-3. RJ45 LED Indicators [J10]

Power-Over-Ethernet (PoE) is not supported.

2.1.3.3 On-Board JTAG/Emulator [J13] with optional External Interface [J15]

The EVM supports an integrated XDS110 emulator for loading and debugging software. The USB micro-B connector [J13] on the EVM is connected to a Host-PC using supplied USB cable (Type-A to Micro-B). The computer can use Texas Instruments' Code Composer Studio (CCS) to establish a connection with the

processor and download and debug software on the various processor cores. The circuit is powered through BUS power. LEDs [LD12] [LD3] are used to indicate an active connection with Host-PC or processor.

Optionally, an external JTAG emulation or debugger can connect using a dedicated emulation connector [J15]. The connector is aligned with the Texas Instrument 20-pin CTI header standard (2x20, 1.27mm pitch), and is compatible with Texas Instruments modules (XDS110, XDS200, XDS560v2) and third party modules.

Table 2-5. Expansion Header Pin Definition [J15]

Pin #	Pin Name	Description	Dir
1	TMS	Test Mode Select	Input
2	TRSTn	Test Reset	Input
3	TDI	Test Data Input	Input
4	TDIS	Target Disconnect	Output
5	Vref	Target Voltage Detect, 3.3V	Output
6	<No pin>	No pin/Key	
7	TDO	Test Data Output	Output
8	GND	Ground	
9	RTCK	Test Clock Return	Output
10	GND	Ground	
11	TCK	Test Clock	Input
12	GND	Ground	
13	EMU0	Emulation Pin 0	Bi-Dir
14	EMU1	Emulation Pin 1	Bi-Dir
15	RESETz	Target Reset	Input
16	GND	Ground	
17		Open	
18		Open	
19		Open	
20	GND	Ground	

Note

In the DIR column, output is to the JTAG module, input is from the JTAG module. Bi-Dir signals can be configured as either input or output.

2.1.3.4 USB3.1 Gen1 Interfaces [J11] [J14]

The EVM supports three USB3.1 Gen1 Type A ports [J11][J14], which operate in Host mode. The combined VBUS output for these ports is limited to 2.8A.

Also supported is one USB3.1 Gen1 Type C interface [J14], which can function as a DFP. The VBUS output for this port is limited to 1.5A. The EVM cannot be powered from this port.

2.1.3.5 Stacked DisplayPort and HDMI Type A [J16]

The EVM supports DisplayPort panel via standard DP cable interface [J16]. The interface supports resolutions to 4K UHD (3840x2160) including MST (Mutli-Stream Transport) for supporting multiple panels. A second display interface is supported via HDMI connector [J13], and supports resolutions up to 1080p (1920x1080). The interface is DVI, and therefore does not support the integrated audio. Both DisplayPort and HDMI interfaces can be used simultaneously.

2.1.3.6 PCIe Connector [J3] for PCIe Card Modules

The EVM supports a PCIe card slot for supporting full size PCIe cards. The slot accepts up to 8-Lane cards, but only 4-Lanes are supported. This expansion interface is used for a wide variety of peripherals, and supports the following interfaces: PCIe (4x) and I2C.

2.1.3.7 M.2 Key M Connector [J12] for SSD Modules

The EVM supports a Mini-PCIe M.2, Key M slot (2280) for expansion modules [J12]. This expansion interface is primarily used for Solid State Drives (SSD), and supports the following interfaces: PCIe (2x) and I2C.

2.1.3.8 M.2 Key E Connector [J23] for Wi-Fi Networking Modules

The EVM supports a Mini-PCIe M.2, Key E slot (2230) for expansion modules [J23]. This expansion interface is primarily used for BT/Wi-Fi modules, and supports the following interfaces: PCI Express (PCIe) (1x) and inter-integrated circuit (I2C).

Note

An example optional add-on Wireless Network module for this interface is the Intel M.2 Type E Wi-Fi/ 9260NGW.

2.1.3.9 MicroSD Card Cage [J32]

The EVM supports a micro-SD card cage. The EVM supports UHS-1 class memory cards, including SDHC and SXDC. The connector is a PUSH-PUSH connector, meaning you push to insert the card and push again to remove the card.

A MicroSD Card is included with the EVM.

2.1.4 Expansion Interfaces

The EVM supports expansion interfaces that have non-standard/custom pinouts. Each of those interfaces are introduced and specific pin information is provided.

2.1.4.1 Heat Sink [ACC] With [J22] Fan Header

The heat sink supports cooling of the device at ambient temperatures and is mounted on the processor. If your environment or use case requires additional cooling, a fan can be added to the heat sink.

The fan connector is a 3-pin header (TE CONNECTIVITY, Part number 440054-3).

Table 2-6. Fan Header Pin Definition [J22]

Pin #	Pin Name	Description	Direction
1	<open>	Unconnected	N/A
2	12V	Main 12V supply	Output
3	GND	Ground	

2.1.4.2 CAN-FD Connector(s) [J4] [J5] [J8] [J9]

The EVM supports four (4x) CAN Bus interfaces.

Table 2-7. CAN-FD Interface Assignment

Connector Ref	Processor Resource
J4	MCU_CAN1
J5	CAN6
J8	MCU_CAN0
J6	CAN7

Each Controller Area Network (CAN) Bus interface is supported on a 3-pin, 2.54mm pitch header. The interface meets ISO 11898-2 and ISO 11898-5 physical standards, and supports CAN and optimized CAN-FD performance up to 8Mbps. Each includes CAN Bus end-point termination. If the SK is included in a network with more than two nodes, the termination my need to be adjusted.

Table 2-8. CAN-FD Header Pin Definition [J4][J5][J8][J9]

Pin #	Pin Name	Description	Direction
1	CAN-H	High-Level CAN Bus Line	Bi-Dir
2	GND	Ground	
3	CAN-L	Low-Level CAN Bus Line	Bi-Dir

2.1.4.3 Expansion Header [J27]

The EVM includes a 40-pin (2x20, 2.54mm pitch) expansion interface [J27]. The expansion connector supports variety of interfaces including: I2C, serial peripheral interface (SPI), I2S with Audio clock, UART, pulse width modulator (PWM), and GPIO. All signals on the interfaces are 3.3V levels.

Table 2-9. Expansion Header Pin Definition [J27]

Pin #	Pin Name	Description (AM69 Pin #)	Dir
1	Power	Power,3.3V	Output
2	Power	Power,5.0V	Output
3	I2C_SDA	MCU I2CBus #0, Data (G34)	Bi-Dir
4	Power	Power,5.0V	Output
5	I2C_SCL	MCU I2CBus #0, Clock (M35)	Bi-Dir
6	GND	Ground	
7	GP_CLK/GPIO	REFCLK0/WKUP_GPIO0_66 (N34)	Bi-Dir
8	UART_TXD	UART#5 Transmit (AG36)	Output
9	GND	Ground	
10	UART_RXD	UART#5 Receive (AJ33)	Input
11	GPIO	GPIO0_42 (AF34)	Bi-Dir
12	I2S_SCLK	McASP#1 ACLKX (AC34)	Bi-Dir
13	GPIO	GPIO0#36 (AC35)	Bi-Dir
14	GND	Ground	
15	GPIO	WKUP_GPIO0_49 (M33)	Bi-Dir
16	GPIO	GPIO0#3 (AF33)	Bi-Dir
17	Power	Power,3.3V	Output
18	GPIO	AUDIO_EXT_REFCLK0(AJ34)	Bi-Dir
19	SPI_PICO	MCU SPI#1 Data 0 (J34)	Bi-Dir
20	GND	Ground	
21	SPI_POCI	MCU SPI#1 Data 1 (J35)	Bi-Dir
22	GPIO	WKUP_GPIO0_67 (M34)	Bi-Dir

Table 2-9. Expansion Header Pin Definition [J27] (continued)

Pin #	Pin Name	Description (AM69 Pin #)	Dir
23	SPI_SCLK	MCU SPI#1 Clock (H38)	Bi-Dir
24	SPI_CS0	MCU SPI #1 Chip Select 0 (J36)	Bi-Dir
25	GND	Ground	
26	SPI_CS1	MCU SPI #1 Chip Select 2 (K37)	Bi-Dir
27	ID_SDA	WKUP I2C #0 Data (N35)	Bi-Dir
28	ID_SCL	WKUP I2C #0 Clock (N33)	Bi-Dir
29	GPIO	WKUP_GPIO0_56 (M37)	Bi-Dir
30	GND	Ground	
31	GPIO	WKUP_GPIO0_57(M36)	Bi-Dir
32	PWM0	PWM3_A (AE35)	Output
33	PWM1	PWM0_A (AM37)	Output
34	GND	Ground	
35	I2S_FS	McASP #1 AFSX (AD33)	Bi-Dir
36	GPIO	GPIO0_41 (AJ36)	Bi-Dir
37	GPIO	GPIO0_27 (AJ37)	Bi-Dir
38	I2S_DIN	McASP #1 AXR0 (AD38)	Bi-Dir
39	GND	Ground	
40	I2S_DOUT	McASP #1 AXR4 (AL34)	Bi-Dir

2.1.4.4 Camera Interface, 22-Pin Flex Connectors [J1] [J2]

The EVM supports two (2) 22-pin flex (0.5mm pitch) connectors [J1][J2] for interfacing with camera modules. Each camera interface provides MIPI CSI-2interface (4Lane), Clock/Control signals, and power (3.3V) to the camera.

To enable camera modules with same addressing to be used simultaneously, I2C mux is used to select each camera. The voltage level for Clock/Control signals is selectable between 1.8V/3.3V.

Table 2-10. Camera 0 Flex Pin Definition [J1]

Pin #	Pin Name	Description	Dir
1	GND	Ground	Output
2	CSI0_D0_N	CSIPort 0 Data Lane 0	Input
3	CSI0_D0_P	CSIPort 0 Data Lane 0	Input
4	GND	Ground	
5	CSI0_D1_N	CSIPort 0 Data Lane 1	Input
6	CSI0_D1_P	CSIPort 0 Data Lane 1	Input
7	GND	Ground	
8	CSI0_CLK_N	CSIPort 0 CLK	Input
9	CSI0_CLK_P	CSIPort 0 CLK	Input
10	GND	Ground	
11	CSI0_D2_N	CSIPort 0 Data Lane 2	Input
12	CSI0_D2_P	CSIPort 0 Data Lane 2	Input
13	GND	Ground	
14	CSI0_D3_N	CSIPort 0 Data Lane 3	Input
15	CSI0_D3_P	CSIPort 0 Data Lane 3	Input
16	GND	Ground	
17	CAM0_PWDN	Pwr-Dwn(IO expander)	Output
18	CAM0_AUX	AUX (WKUP_GPIO0_88)	Bi-Dir
19	GND	Ground	

Table 2-10. Camera 0 Flex Pin Definition [J1] (continued)

Pin #	Pin Name	Description	Dir
20	I2C_SCL	I2C Clock #1, Mux 0	Output
21	I2C_SDA	I2C Data # 1, Mux 0	Bi-Dir
22	Power	Power, 3.3V	Output

Table 2-11. Camera 1 Flex Pin Definition [J29]

Pin #	Pin Name	Description	Dir
1	GND	Ground	Output
2	CSI1_D0_N	CSIPort 1 Data Lane 0	Input
3	CSI1_D0_P	CSIPort 1 Data Lane 0	Input
4	GND	Ground	
5	CSI1_D1_N	CSIPort 1 Data Lane 1	Input
6	CSI1_D1_P	CSIPort 1 Data Lane 1	Input
7	GND	Ground	
8	CSI1_CLK_N	CSIPort 1 CLK	Input
9	CSI1_CLK_P	CSIPort 1 CLK	Input
10	GND	Ground	
11	CSI1_D2_N	CSIPort 1 Data Lane 2	Input
12	CSI1_D2_P	CSIPort 1 Data Lane 2	Input
13	GND	Ground	
14	CSI1_D3_N	CSIPort 1 Data Lane 3	Input
15	CSI1_D3_P	CSIPort 1 Data Lane 3	Input
16	GND	Ground	
17	CAM1_PWDN	Pwr-Dwn(IO expander)	Output
18	CAM1_AUX	AUX (WKUP_GPIO0_70)	Bi-Dir
19	GND	Ground	
20	I2C_SCL	I2C Clock #1, Mux 1	Output
21	I2C_SDA	I2C Data # 1, Mux 1	Bi-Dir
22	Power	Power, 3.3V	Output

2.1.4.5 Camera Interface, 40-Pin High Speed [J31] [J30]

The EVM includes a 40-pin (2x20, 2.54mm pitch,) high-speed camera interface [J31][J30]. Each expansion connector [J31][J30] supports two CSI-2 (4 Lanes each), power, and control signals (I2C, GPIO, and so forth). All control signals are configurable for 3.3V or 1.8V voltage levels.

Table 2-12. Camera IO Voltage Control

I2C IO Expander (P0)	Camera IO Level
Low or ‘0’	1.8V (Default)
High or ‘1’	3.3V

Table 2-13. 40-Pin High-Speed Camera Expansion Pin Definition [J31]

Pin #	Pin Name	Description (Processor Pin #)	Dir
1	Power		Output
2	I2C_SCL	I2CBus #1, Clock (AE34)	Bi-Dir
3	Power		Output
4	I2C_SDA	I2CBus #1, Data (AL33)	Bi-Dir
5	CSI0_CLK_P	CSIPort 0 Clock	Input
6	GPIO/PWMA	WKUP_GPIO0_32(C31)	Bi-Dir
7	CSI0_CLK_N	CSIPort 0 Clock	Input
8	GPIO/PWMB	WKUP_GPIO0_36 (G31)	Bi-Dir

Table 2-13. 40-Pin High-Speed Camera Expansion Pin Definition [J31] (continued)

Pin #	Pin Name	Description (Processor Pin #)	Dir
9	CSI0_D0_P	CSIPort 0 Data Lane 0	Input
10	REFCLK	MCU CLKOUT0(M38)	Bi-Dir
11	CSI0_D0_N	CSI Port 0 Data Lane 0	Input
12	GND	Ground	
13	CSI0_D1_P	CSI Port 0 Data Lane 1	Input
14	RESETz	FROM IO EXPANDER	Output
15	CSI0_D1_N	CSI Port 0 Data Lane 1	Input
16	GND	Ground	
17	CSI0_D2_P	CSI Port 0 Data Lane 2	Input
18	GPIO	WKUP_GPIO0_37 (F33)	Bi-Dir
19	CSI0_D2_N	CSI Port 0 Data Lane 2	Input
20	GPIO	WKUP_GPIO0_38 (G32)	Bi-Dir
21	CSI0_D3_P	CSI Port 0 Data Lane 3	Input
22	GPIO	WKUP_GPIO0_35 (D31)	Bi-Dir
23	CSI0_D3_N	CSI Port 0 Data Lane 3	Input
24	GND	Ground	
25	CSI1_CLK_P	CSI Port 1 Clock	Input
26	CSI1_D3_P	CSI Port 1 Data Lane 3	Input
27	CSI1_CLK_N	CSI Port 1 Clock	Input
28	CSI1_D3_N	CSI Port 1 Data Lane 3	Input
29	CSI1_D0_P	CSI Port 1 Data Lane 0	Input
30	Power	Power, 3.3V	Output
31	CSI1_D0_N	CSI Port 1 Data Lane 0	Input
32	Power	Power, 3.3V	Output
33	CSI1_D1_P	CSI Port 1 Data Lane 1	Input
34	Power	Power, 3.3V	Output
35	CSI1_D1_N	CSI Port 1 Data Lane 1	Input
36	Power	Power, 3.3V	Output
37	CSI1_D2_P	CSI Port 1 Data Lane 2	Input
38	Power	Power, IO Level (1.8 or 3.3V)	Output
39	CSI1_D2_N	CSI Port 1 Data Lane 2	Input
40	Power	Power, IO Level (1.8 or 3.3V)	Output

Table 2-14. 40-Pin High-Speed Camera Expansion Pin Definition [J30]

Pin #	Pin Name	Description (Processor Pin #)	Dir
1	Power		Output
2	I2C_SCL	I2CBus #1, Clock (AE34)	Bi-Dir
3	Power		Output
4	I2C_SDA	I2CBus #1, Data (B34)	Bi-Dir
5	CSI2_CLK_P	CSIPort 0 Clock	Input
6	GPIO/PWMA	WKUP_GPIO0_29(C31)	Bi-Dir
7	CSI2_CLK_N	CSIPort 0 Clock	Input
8	GPIO/PWMB	WKUP_GPIO0_31 (F32)	Bi-Dir
9	CSI2_D0_P	CSIPort 0 Data Lane 0	Input
10	REFCLK	MCU CLKOUT0(M38)	Bi-Dir
11	CSI2_D0_N	CSI Port 0 Data Lane 0	Input
12	GND	Ground	

Table 2-14. 40-Pin High-Speed Camera Expansion Pin Definition [J30] (continued)

Pin #	Pin Name	Description (Processor Pin #)	Dir
13	CSI2_D1_P	CSI Port 0 Data Lane 1	Input
14	RESETz	FROM IO EXPANDER	Output
15	CSI2_D1_N	CSI Port 0 Data Lane 1	Input
16	GND	Ground	
17	CSI2_D2_P	CSI Port 0 Data Lane 2	Input
18	GPIO	WKUP_GPIO0_33 (F31)	Bi-Dir
19	CSI2_D2_N	CSI Port 0 Data Lane 2	Input
20	GPIO	WKUP_GPIO0_34 (E35)	Bi-Dir
21	CSI2_D3_P	CSI Port 0 Data Lane 3	Input
22	GPIO	WKUP_GPIO0_39 (G33)	Bi-Dir
23	CSI2_D3_N	CSI Port 0 Data Lane 3	Input
24	GND	Ground	
25	<open>		N/A
26	<open>		N/A
27	<open>		N/A
28	<open>		N/A
29	<open>		N/A
30	Power	Power, 3.3V	Output
31	<open>		N/A
32	Power	Power, 3.3V	Output
33	<open>		N/A
34	Power	Power, 3.3V	Output
35	<open>		N/A
36	Power	Power, 3.3V	Output
37	<open>		N/A
38	Power	Power, IO Level (1.8 or 3.3V)	Output
39	<open>		N/A
40	Power	Power, IO Level (1.8 or 3.3V)	Output

2.1.4.6 Automation and Control Connector [J17]

The EVM supports an interface to allow for automated control of the system, including functions like on/off, reset, and boot mode settings.

Table 2-15. Test Automation Interface Pin Definition [J25]

Pin	Pin Name	Description (Processor Pin #)	Dir
1	Power	Power,3.3V	Output
2	Power	Power,3.3V	Output
3	Power	Power,3.3V	Output
4-6	<open>		N/A
7	GND	Ground	
8-15	<open>		N/A
16	GND	Ground	
17-24	<open>		N/A
25	GND	Ground	
26	POWERDOWNz	SK Power Down	Input
27	PORz	SK Power-On/Cold Reset	Input
28	RESETz	SK Warm Reset	Input

Table 2-15. Test Automation Interface Pin Definition [J25] (continued)

Pin	Pin Name	Description (Processor Pin #)	Dir
29	<open>		N/A
30	INT1z	MCU_ADC1_AIN0 (Y38)	Input
31	INT2z	MCU_ADC1_AIN1 (Y34)	Bi-Dir
32	BOOTMODE_CNTL#	NA	N/A
33	BOOTMODE_RSTz	Bootmode Buffer Reset	Input
34	GND	Ground	
35	<open>		N/A
36	I2C_SCL	I2C Bus #0, Clock (AN36)	Bi-Dir
37	BOOTMODE_SCL	Bootmode Buffer I2C Clock	Input
38	I2C_SDA	I2C Bus #0, Data (AP37)	Bi-Dir
39	BOOTMODE_SDA	Bootmode Buffer I2C Data	Bi-Dir
40-42	GND	Ground	

3 Hardware Design Files

The hardware design files are combined to a single package and available for download on ti.com. The package file can contain multiple EVM board revisions (directories). The naming convention is as follows for PROCxyzEwq_RP where:

- PROC: Indicates TI's Processor Product.
- xyz: Unique ID for this Evaluation Board (example is '154' for this design).
- E: E indicates Pre-Production, blank for Production.
- wq: Indicates Revision (w - Major, blank/q - Minor).
- _RP: Release Package Notation.

Example (oldest to latest revision):

PRO154E1A: Pre-Production, version '1A'

PROC154E2: Pre-Production, Version '2'.

PROC154A: Production, Version 'A'.

See schematic history/change log for complete list of changes for each revision.

3.1 Schematics

The schematics are available in both design format (Cadence Allegro, *_SCH.DSN) and searchable PDF (*_SCH.PDF). Both are included as part of the design package and available for download on ti.com.

3.2 PCB Layouts

The PCB design and manufacturing information is available in several different file formats. Below is a list of PCB files included in the design package available for download on ti.com.

Table 3-1. PCB Design and Manufacturing Files

File Type	Description
Design file (*_BRD.ZIP)	Allegro PCB design file/zip
Design file (*_ODBGRB.ZIP)	Design file exported to ODB++/Zip
Design file extract (ALG)	For import into other design tools
Fabrication drawing (*_FAB.PDF)	Fabrication info in viewable format
Manufacturing file (_274XGBR.ZIP)	Gerber data, RS-274/ZIP
Manufacturing file (*_STL.ZIP)	Gerber data, STL/Zip
Manufacturing file (*_BRD.IPC)	IPC-D 465 Gerber data supplement
Layers drawing (*_LAYERS.PDF)	Viewable images of each PCB Layer
Stack-up (*_STACKUP.PDF)	PCB Stack-up from PCB manufacturer

3.3 Bill of Materials (BOM)

The Bill Of Materials (BOM) is available in spreadsheet format (Microsoft Excel, *_BOM.XLSX) and is included as part of the design package download on ti.com.

4 Compliance Information

4.1 Compliance and Certifications

There is elevated heat on the processor and heat sink. Use caution particularly at elevated ambient temperatures!

Although the processor and heat sink are not burn hazards, caution must be used when handling the SK due to increased heat in the area of the heat sink.

	Caution	Caution Hot surface. Contact may cause burns. Do not touch!

4.2 Electrostatic Discharge (ESD) Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). It is recommended this product be used in an ESD controlled environment. This may include a temperature and/or humidity-controlled environment to limit the buildup of ESD. It is also recommended to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory condition and the applied standard will be as per ENC IEC 61326-1:2021.

5 Additional Information

5.1 Known Hardware or Software Issues

5.2 Trademarks

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2024) to Revision B (December 2025)	Page
• Added HDMI trademark information	1
• Added Note to Section 2.1.3	7
• Updates were made in Section 2.1.3.4	8
• Updated Hardware Design Files section	16
• Added new Section 4.2	17

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NOTE:

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3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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