User's Guide

SK-AM64B EVM User's Guide

ABSTRACT

This technical User's Guide describes the hardware architecture of the SK-AM64B. The SK-AM64B (henceforth referred as AM64x SKEVM or simply SKEVM). The AM64x processor comprises of a Dual-Core 64-bit Arm-Cortex A53 microprocessor, 2x Dual core Arm® Cortex®-R5F MCUs and an Arm Cortex-M4F MCU. The AM64x starter kit is a stand-alone test and development platform that is ideal for accelerating the prototype phase of your next design. The kit includes: wired and wireless connectivity, three expansion headers, multiple boot options and flexible debug capabilities.

The starter kit is equipped with AM64x processor from TI and an optimized feature-set to allow the user to create commercial and industrial solutions using Ethernet-based, USB, and serial wired interfaces plus 2.4-GHz and 5-GHz wireless communications. Two 1-Gbps Ethernet Ports for wired connectivity are on-board, in addition to three expansion headers (PRU, MCU, User) headers to expand the board's functionality. Using standard serial protocols such as UART, I2C, and SPI, the starter kit can interface with a multitude of other devices, acting as a communications gateway. Receiving 5-V power from a standard USB-C port, the starter kit allows the user to access the R5F cores of the AM64x, making it suitable as a programmable logic controller (PLC) or motor controller, processing sensor inputs and managing peripherals in real-time while running Linux on the A53 cores, making it the central engine in a remote industrial communication network. The embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ from TI.

Note

This document specifically describes the PMIC version of the AM64x Starter Kit EVM. For the discrete version please visit the following link.

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Trademarks

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1 Key Features

Processor:

The core processing unit of the SKEVM is the AM64x Series processor (soldered to the PCB) without socket.

Memory

- 2GB of 16-Bit LPDDR4 memory
- Micro Secure Digital (SD) Card with UHS-1 support
- 512Mbit Octal SPI Flash memory.
- 512Kbit I2C EEPROM for board ID

High Speed Interface:

- Gigabit Ethernet interfaces (RGMII) from CPSW RGMII Port of processor connected to two Ethernet PHY IC's and terminated on two numbers of RJ45 connectors.
- USB3.0 HOST interface terminated on USB Type-A Connector for data transfer

Expansion Header:

- SKEVM board has three expansion connectors using 0.1” spaced 0.025” square post connectors.
- All the three expansion connectors are on the top of the board.
- The three connectors include the 40-pin User expansion connector, the PRU 54-pin connector, and the MCU 28-pin connector.

User Expansion Connector (40 Pin):

- This connector is compatible with the standard expansion connector found on a Raspberry Pi 4B®™ allowing seamless interface with HAT Boards.
- Four mounting holes must be oriented with the connector to allow for connection of these boards.
- Signals are at 3.3-V Logic Level.
- Signals connected from SoC to the Expansion Header include: SPI (0), SPI (1), UART (5), I2C (0), I2C (2), EHRPWM4_A / B, EHRPWM5_A / B along with GPIOs [32, 35, 38, 39, 40, 41, 42] along with 5-V and 3.3-V PWR and GND.
- 5 V and 3.3 V are current limited to 155 mA and 500 mA, respectively.

PRU Header (54 Pin):

- PRU Header offers low speed connection to PRG0 Interface.
- PRG0_PRU0 and PRG0_PRU1 signals are terminated on the PRU Expansion Connector.
- PRG0 signals are connected to a 27x2 standard 0.1” spaced 54-pin connector.
- Connector contains MDIO control Signals (2 Pins), PRG0_PRU0_GPO [0: 19], PRG0_PRU1_GPO [0: 17], +3.3V PWR (2 Pins) and Ground reference (5 Pins), SoC I2C0 signals (2 pins), Reserved (2 pins), DETECT, RESET, INT going to the daughter card.
- 3.3 V are current limited to 500 mA.

Safety Connector or MCU 28pin connector:

- A safety signal connector is 14x2 standard 0.1” spaced header.
- The pin-out should be compatible with the AM64 GPEVM.
- MCU connector will only include signals connected to the MCU.
- 18 Signals include MCU_I2C0, MCI_I2C1, MCU_UART1 (with flow control), MCU_SPI0 and MCU_GPIO (6, 7, 8 and 9), and Test LED signal.
- Additional control signals provided on the connector include CONN_MCU_RESETz, CONN_MCU_PORz, MCU_RESETSTATz, MCU_SAFETY_ERRORn_3.3V IO to MCU and GND.
- MCU Domain warm reset (MCU_RESETz) and MCU Domain cold reset (MCU_PORz) of SoC is achieved by CONN_MCU_RESETz and CONN_MCU_PORz respectively from Safety Connector.
- Allowed current limit is 100 mA on 3.3-V rail.

Serial Interfaces:

- SoC I2C [0] signals are connected to Board ID EEPROM, User Expansion Headers, and TPS6522053xx PMIC.
- SoC I2C [1] signals are connected to 8-Bit LED Driver, 8-Bit GPIO Expander, Temperature Sensors and Test Automation Header.

- SoC I2C [2] signals are connected to User Expansion Headers.
- SPI0 and SPI1 signals are connected to User expansion connector.
- SoC UART [5] signals are connected to User expansion connector.

LEDs, Push Buttons, and Boot Switches:

- LEDs: Main Power(x1), PMIC PGOOD(x1), GPIO from MPU Domain(x1) and MCU domain(x1), Fault Indication LED(x1), Eight Industrial Communication LEDs.
- Push Button Switches: Enable Pin of TPS6522053xx PMIC (x1), and User Interrupt push button on AM64x Main GPIO (x1).
- Boot Switches: Two 8-Bit DIP Switches for the User to select various Boot modes for AM64x.

Sensor Interface:

- 2x Temperature Sensor near SoC and LPDDR4 for thermal monitoring.

JTAG and DEBUG Interfaces:

- Necessary circuit to offer on-board JTAG Support using XDS110 emulation through Micro- B USB connector.
- XDS110 also offers UART-To-USB Interface for one of the Serial Ports of AM64xx (SoC_Main_UART1)
- Additionally one 20-pin cTI connector is also used.
- USB to UART (x2 Ports) for Debug Console access terminated on a single USB Micro-B Connector is provided via CP2105.
- XDS110 controller controls the power cycle, change boot modes, and reset the SoC.

Power Supply:

- The AM64x SKEVM is powered through a USB Type-C Connector
- 5V is bucked down to 3V3 by LM61460AASQRJRRQ1 regulator. VCC3V3SYS_EXT is the input supply to the PMIC.
- TPS6522053RHBR PMIC and other discrete regulators on the starter kit provide all the required power supplies for SoC and other peripherals (LPDDR4, Wi-Fi Module, OSPI, Clock buffers, Level translators, and logic gates).
- Dedicated regulators are also provided for:
  - Powering the always-on circuits of the Test Automation Header section.
  - E-Fuse programming of the SoC.
  - Optional Power to the WL1837MOD WiLink module
  - XDS110 Debugger section
  - 3V3 for SoC and peripherals
  - 1V0 for Ethernet Phys
- Recommended Power Supplies:
  - CUI Inc. 5V 15W AC/DC External Wall Mount Adapter - SWC15-S5-NB
  - GlobalTek Inc. 5V 15W AC/DC External Mount Wall Adapter - WR9QA3000USBC3MNA-CIMR6B
  - Qualtek USB 2.0 Cable C Male to C Male 3.28' Shielded Cable for powering the boards through a laptop Type-C port - 3021091-01M

2 AM64x SKEVM Overview

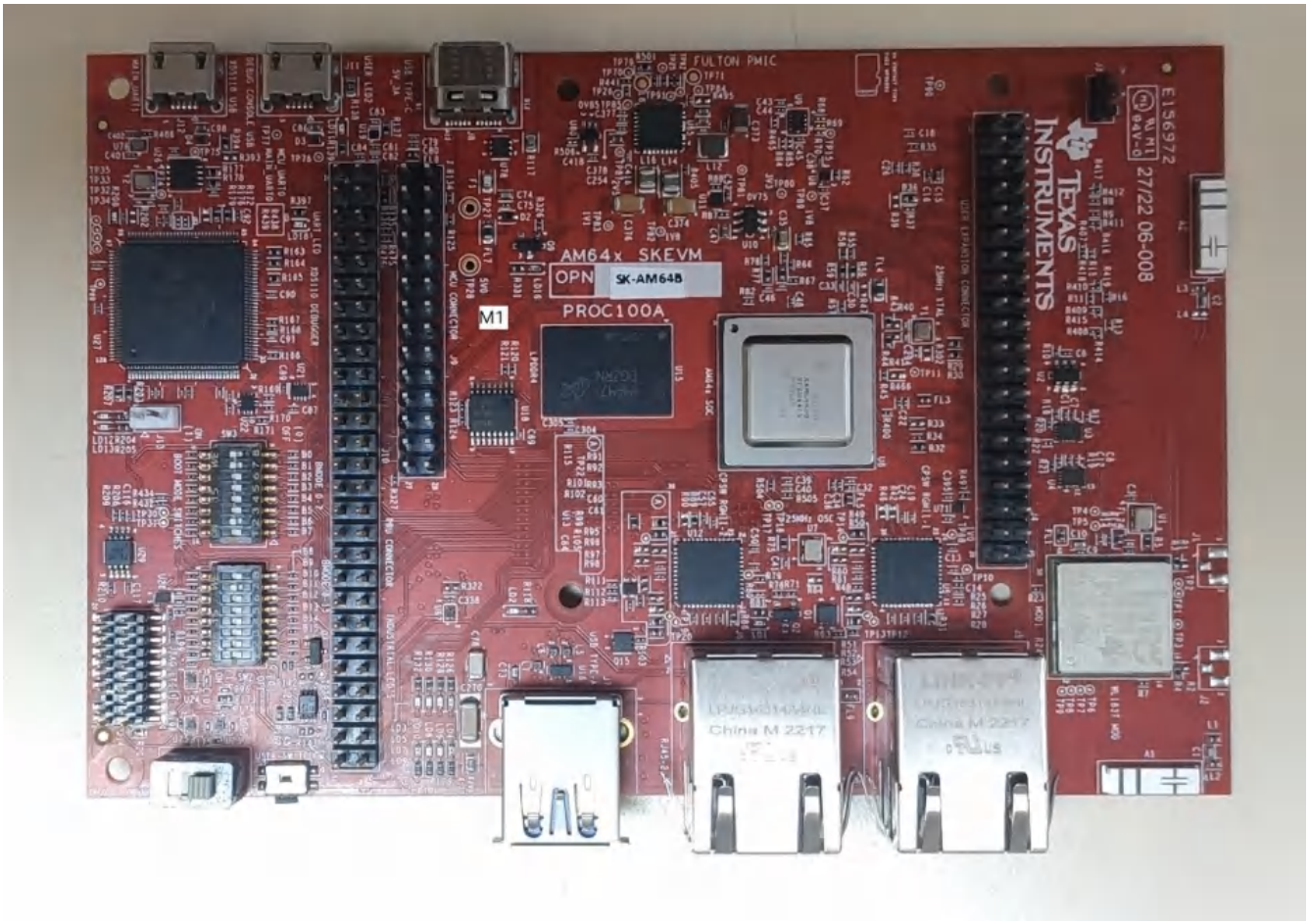


Figure 2-1. System Assembly

2.1 Board Version Identification

To identify the version of the board, an **M1** sticker is pasted on the top side of the board, as shown in Figure 2-2. The M1 sticker on the board signifies that R302 and C294 are not assembled (DNI) on the board.

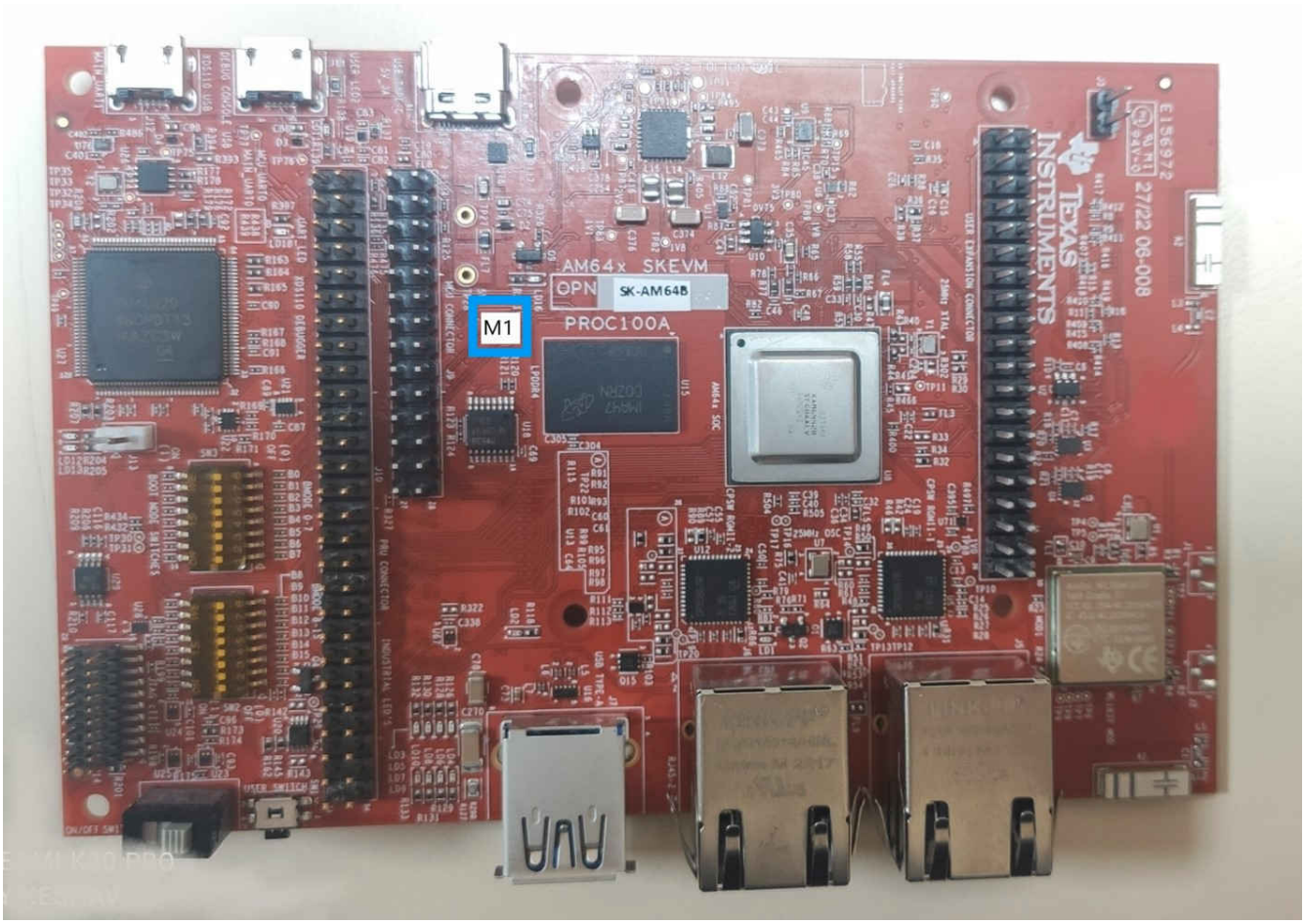


Figure 2-2. M1 Sticker Identification

3 Functional Block Diagram

The functional block diagram of the SKEVM Board is shown in Figure 3-1.

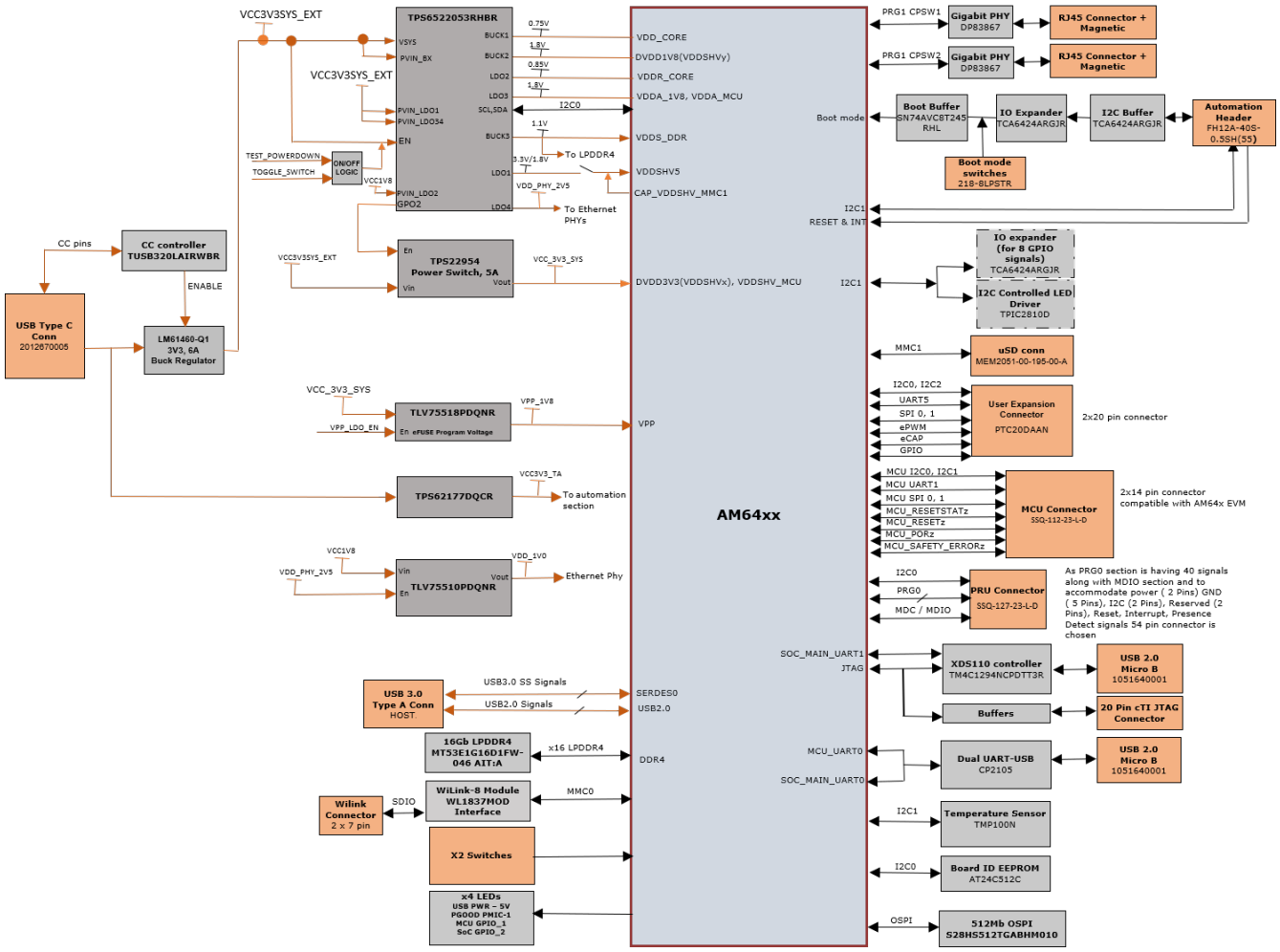


Figure 3-1. SKEVM Board Functional Block Diagram

4 System Description

The following sections provide an overview of the different interfaces and circuits on the SKEVM board.

4.1 Clocking

4.1.1 Ethernet PHY Clock

The clock buffer of part number LMK1C1103PWR is used to drive the 25-MHz clock to the Ethernet PHYs. LMK1C1103PWR is a 1:3 LVCMOS clock buffer, which takes a 25-MHz crystal/LVCMOS reference input and provides three 25-MHz LVCMOS clock outputs. The source for the clock buffer will be either the CLKOUT0 pin from the SoC or a 25-MHz oscillator (ECS-2520MV-250-CN-TR); the selection can be made using a set of resistors. By default, the oscillator is used as input to the clock buffer in AM64x SKEVM. Output Y2 and Y3 of the clock buffer LMK1C1103PWR are used as a reference clock input for two Gigabit Ethernet PHYs in SKEVM.

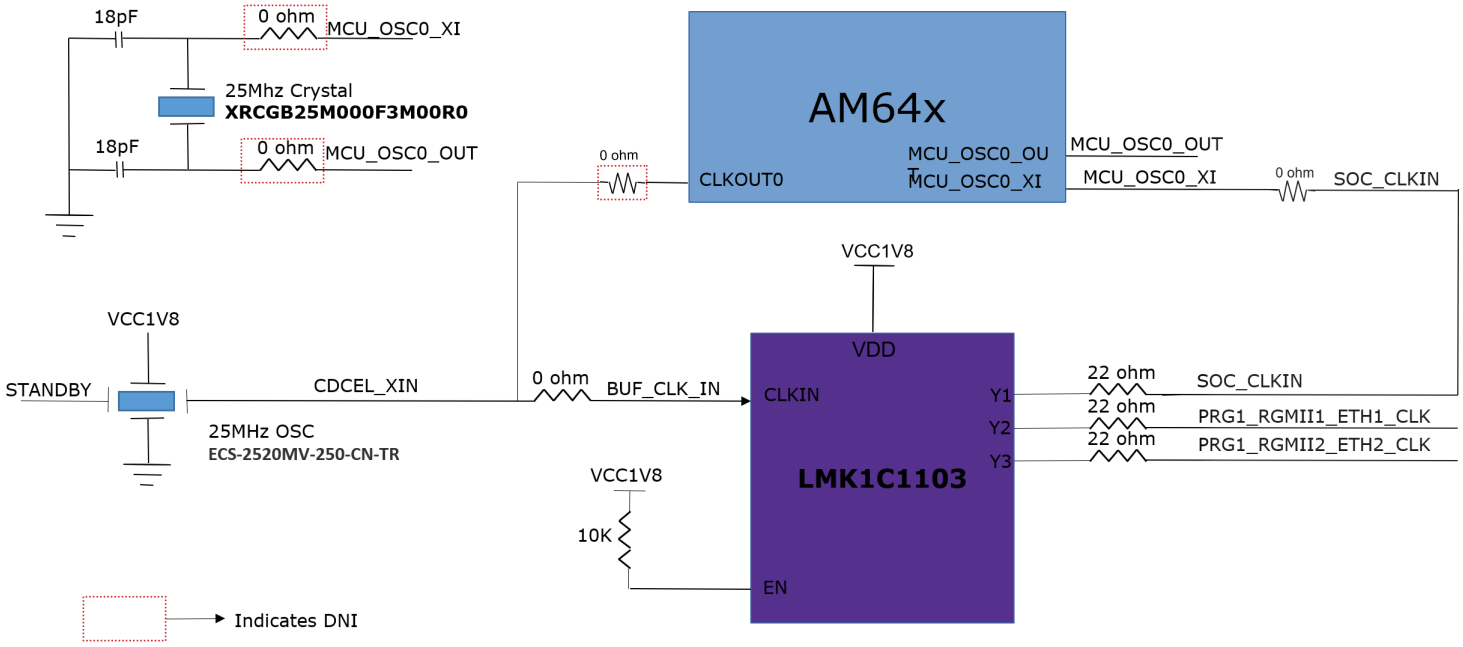


Figure 4-1. AM64x SK EVM Clock Tree

Note

Resistors that are marked with a red color box are DNI.

4.1.2 AM64x SoC Clock

Output Y0 from the clock buffer LMK1C1103PWR is used as a reference clock for the SoC on SKEVM. An optional 25-MHz crystal (XRCGB25M000F3M00R0) is also provided for driving the SoC. Selection of clock for the SoC is done using resistors. By default, an output from the SoC_CLKIN clock buffer is provided to the SoC. For clock source selection, see Table 4-1.

Table 4-1. SoC Clock Source

Clock Source to SoC	Part Number	Mount	Unmount
Clock Buffer	LMK1C1103PWR	R116	R40, R41
25-MHz Crystal	XRCGB25M000F3M00R0	R40, R41	R116

4.2 Reset

The AM64x SoC has the following resets:

- RESETSTATz is the warm reset status output for Main domain.

- PORz_OUT is the power ON reset status output from Main and MCU domain.
- MCU_PORz is the power ON / Cold Reset input for MCU and Main domain.
- MCU_RESETz is the Warm Reset input for MCU domain.
- MCU_RESETSTATz is the Warm Reset status output for MCU domain.

The SoC_PORz signal is provided by ANDing the PGOOD signals of the PMIC and JTAG emulator reset. MCU_PORz is provided by ANDing the CONN_MCU_PORz from the MCU Connector, TEST_PORZn from the Test Automation Connector, and SoC_PORz.

MCU Domain warm reset (MCU_RESETz) and MCU Domain cold reset (MCU_PORz) of the SoC is achieved by CONN_MCU_RESETz and CONN_MCU_PORz, respectively, from the Safety Connector.

Upon Power on Reset, all peripheral devices connected to the main domain are reset by RESETSTATz, along with a GPIO control as shown in Figure 4-2.

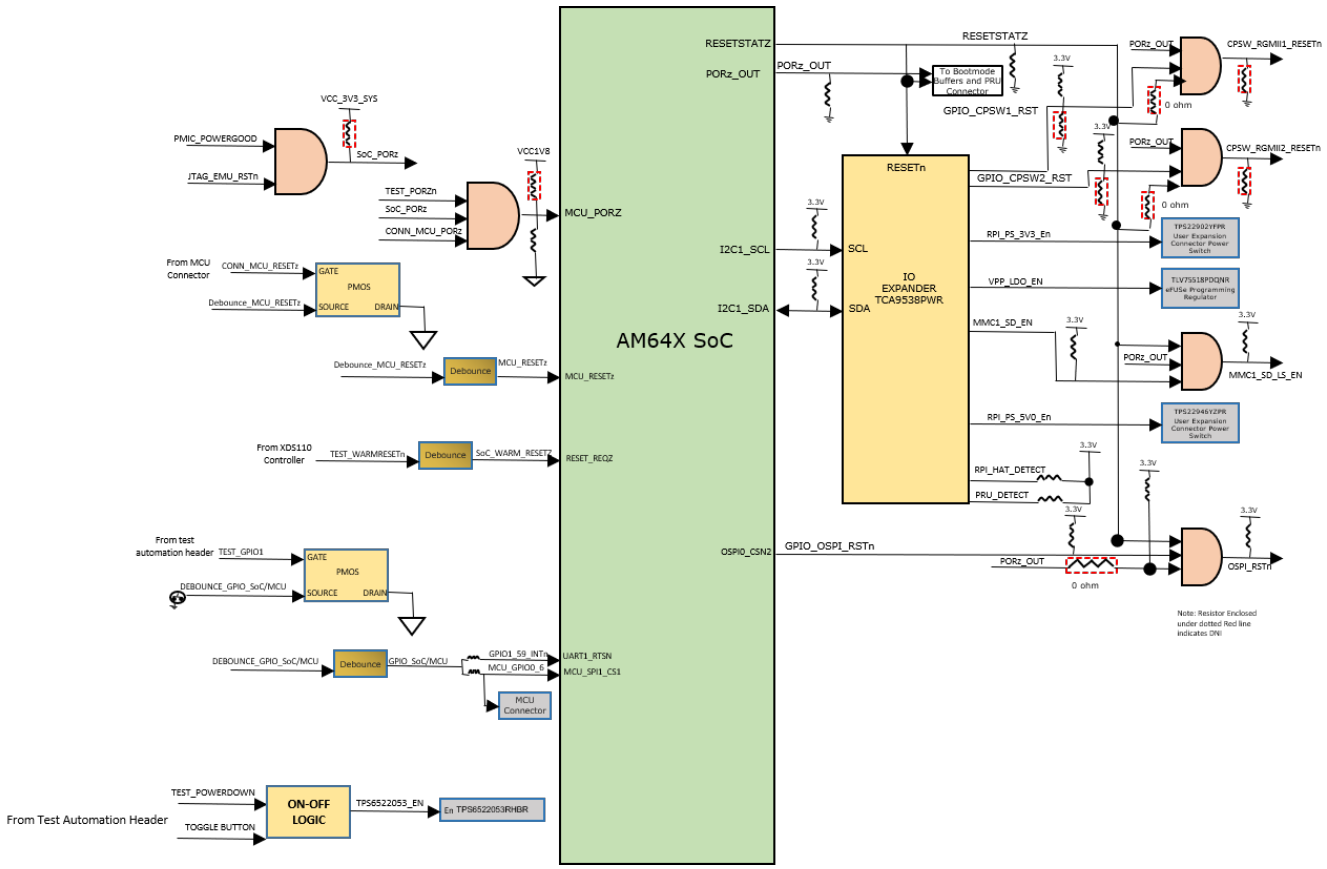


Figure 4-2. Reset Architecture of the AM64x SK Evem

4.3 Power Requirements

4.3.1 Power Input

The SKEVM receives 5-V input from a USB Type-C connector. The following sections describe the power distribution network topology that supply the SKEVM board, supporting components and reference voltages.

The AM64x SKEVM board includes a power solution based on PMIC and a few discrete regulators. The initial stage of the power supply is 5 V from a Type-C USB connector with part No 2012670005 from Molex, which supports a 3A current rating and necessary protection circuits for over current and voltage surge. The 5-V input (VUSB_MAIN) from the USB Connector is used to generate 3.3 V (VCC3V3SYS_EXT) with the help of switching regulator (part No. LM61460AASQRJRRQ1), which is the input supply to the PMIC section. PMIC generates the necessary voltages required for the SKEVM.

A Toggle switch (with part number AS11AP) is provided to initiate the power on and power down sequence of the Board. This switch connects TPS6522053_EN enable signal to ground when switch is in OFF position

and enables PMIC TPS6522053RHBR when the switch is in ON position, thereby initiating the Power – Up Sequence. A low on enable pin of the TPS6522053RHBR PMIC, by sliding the switch to OFF position, initiates the Power-down sequence.

Additionally, TEST_POWERDOWN from the test automation header is also connected to the enable pin of TPS6522053RHBR PMIC to control on/off of the EVM through the test automation board. The test automation connector requires 3.3-V supply, which is provided from power mux (part No: TPS2121RUXT). The inputs to the power mux are 3V3 from two different sources. First 3V3 supply is generated from 5V (XDS_USB_VBUS) using an LDO (Part No: TPS79601DRBR). This will be generated if the Micro B cable is connected to J12. Second 3V3 input is generated from 5V (VUSB_MAIN) using a switching Buck regulator (part No: TPS62177DQCR). This is an Always ON Regulator and supplies the necessary power if the USB Type C Cable is plugged in. When Both Type C cable and Micro B cable at J12 are connected, the mux priority is set to its first input supply (VCC3V3_XDS). If USB is not connected to the J12, the mux output is from VCC3V3_TA, which is an always ON power supply.

4.3.2 USB Type-C Interface for Power Input

The AM64x SKEVM is powered through USB type-C Connector. The USB Type-C source should be capable of providing 3A at 5 V and should advertise the current sourcing capability through CC1 and CC2 signals. On SKEVM, CC1 and CC2 from USB type-C connector are interfaced to the port controller TUSB320LAIRWBR IC. This device uses the CC pins to determine port attach and detach, cable orientation, role detection, and port control for Type-C current mode. This IC allows for the pin swapping when the Type-C cable is flipped and inserted. The CC logic block monitors the CC1 and CC2 pins for pull-up or pull-down resistances to determine when a USB port has been attached, the orientation of the cable, and the role detected. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected. Pin PORT is pulled down to ground through resistor to configure it as UFP (Upward Facing Port) mode. VBUS detection is implemented to determine a successful attach in UFP mode. Pin ADDR is left open to configure it as GPIO mode. OUT1 and OUT2 pin is connected to NOR gate. Active low on both OUT1 and OUT2 pin advertises high current (3A) in the attached state which enables the switching regulator with part No. LM61460AASQRJRRQ1, which generates VCC3V3SYS_EXT supply, the input supply to the PMIC section. In UFP mode, the TUSB320 device constantly presents pull-down resistors (Rd) on both CC pins. The TUSB320 device monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The TUSB320 device de-bounces the CC pins and waits for VBUS detection before successfully attaching. As a UFP, the TUSB320 device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs.

SKEVM power requirement is 5 V at 3A. If the source is not capable of providing 5 V at 3A, output at the NOR gate becomes low, which disables (LM61460AASQRJRRQ1) VCC3V3SYS_EXT Regulator. Thus, all power supplies except VCC3V3_TA does not come up.. Board gets powered ON completely only when the source is capable of providing 5 V at 3A.

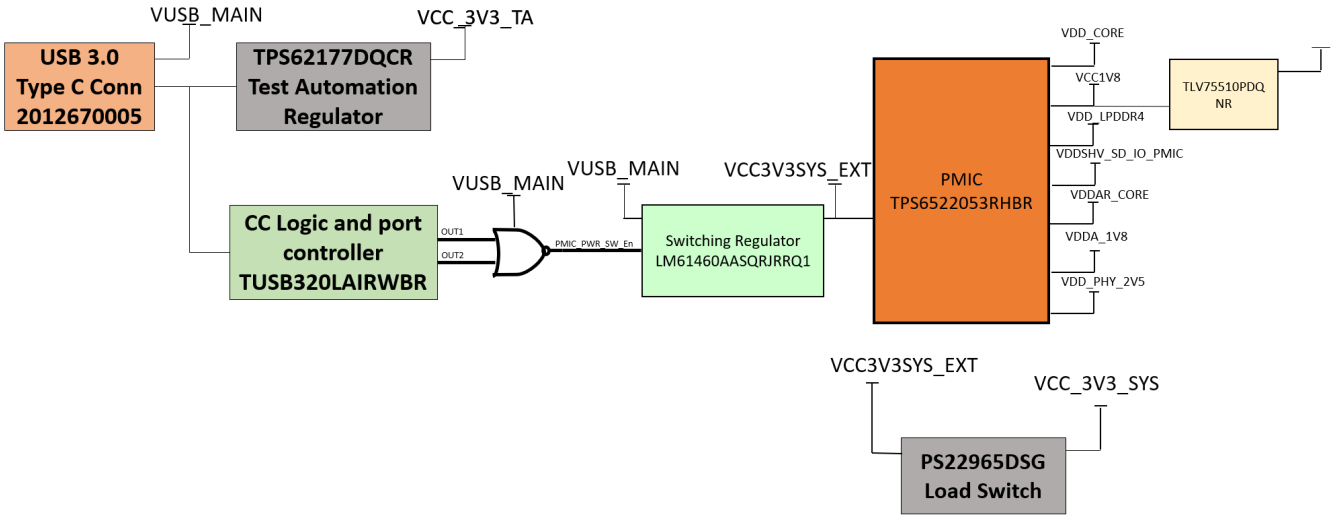


Figure 4-3. USB Type-C Interface for Power Input

Table 4-2. Current Sourcing Capability and State of USB Type C Cable

OUT1	OUT2	Advertisement
H	H	Default current in unattached state
H	L	Default current in attached state
L	H	Medium current (1.5 A) in attached state
L	L	High current (3.0 A) in attached state

4.3.3 Power Fault Indication

The red LED LD15 indicates the power fault condition (i.e. current less than 3 A) by using USB type C configuration channel logic and port controller IC.

Table 4-3. Power Fault Indication LED

LED	ON Status	OFF Status
LD15	Source provides less than 15 W	Source provides the required 15-W power

4.3.4 Power Supply

The AM64x SKEVM uses one PMIC and three discrete regulators to supply the necessary voltage and power to the SoC, various memories, Wilink module, and other peripherals on the board. Probe points for power supplies provided on the SKEVM Board are mentioned in Table 4-4.

Table 4-4. Power Test Points

Points on Bottom Side					
Sl. No	**Power Supply**	**Probe Point**	**Ground**	**Probe Point**	**Expected Voltage (V)**
1	VUSB_MAIN	TP28	DGND	J3.2	5
2	XDS_USB_VBUS	TP75	DGND	J3.2	5
3	VCC_3V3_SYS	TP80	DGND	J3.2	3.3
4	VDDAR_CORE	TP85	DGND	J3.2	0.85
5	VPP_1V8	TP89	DGND	J3.2	0
6	VDD_CORE	TP81	DGND	J3.2	0.75
7	VDD_LPDDR4	TP83	DGND	J3.2	1.1
8	VDD_1V0	TP88	DGND	J3.2	1
9	VCC1V8	TP82	DGND	J3.2	1.8
10	VDD_PHY_2V5	TP87	DGND	J3.2	2.5
11	VDDSHV_SD_IO_PMIC	TP84	DGND	J3.2	3.3
12	VDD_MMC1	C47.1	DGND	J3.2	3.3
13	VBUS_USB_CP2105	TP76	DGND	J3.2	5
14	VCC3V3_XDS	TP74	DGND	J3.2	3.3
15	VDDSHV_SD_IO	TP15	DGND	J3.2	3.3
Points on Top Side					
16	VCC3V3SYS_EXT	TP78	DGND	J3.2	3.3
17	VDDA_1V8	TP86	DGND	J3.2	1.8
18	VCC3V3_TA	C340.1	DGND	J3.2	3.3
19	VCC3V3_TA_XDS	C421.1	DGND	J3.2	3.3

Table 4-5 gives details about power-good LEDs provided on SKEVM board to give users positive confirmation of the status of each supply.

Table 4-5. Power LEDs

Sl.No	Power Supply	LED Part Reference
1	VCC3V3SYS_EXT	LD2

Table 4-5. Power LEDs (continued)

Sl.No	Power Supply	LED Part Reference
2	VCC_3V3_SYS	LD16
3	VDDAR_CORE	LD16
4	VDDA_1V8	LD16
5	VDD_LPDDR4	LD16
6	VDD_CORE	LD16
7	VCC1V8	LD16
8	VDDSHV_SD_IO_PMIC	LD16
9	VDD_PHY_2V5	LD16
10	VDDA_1V8	LD16
11	VDD_CP2105	LD18

4.3.5 Power Sequencing

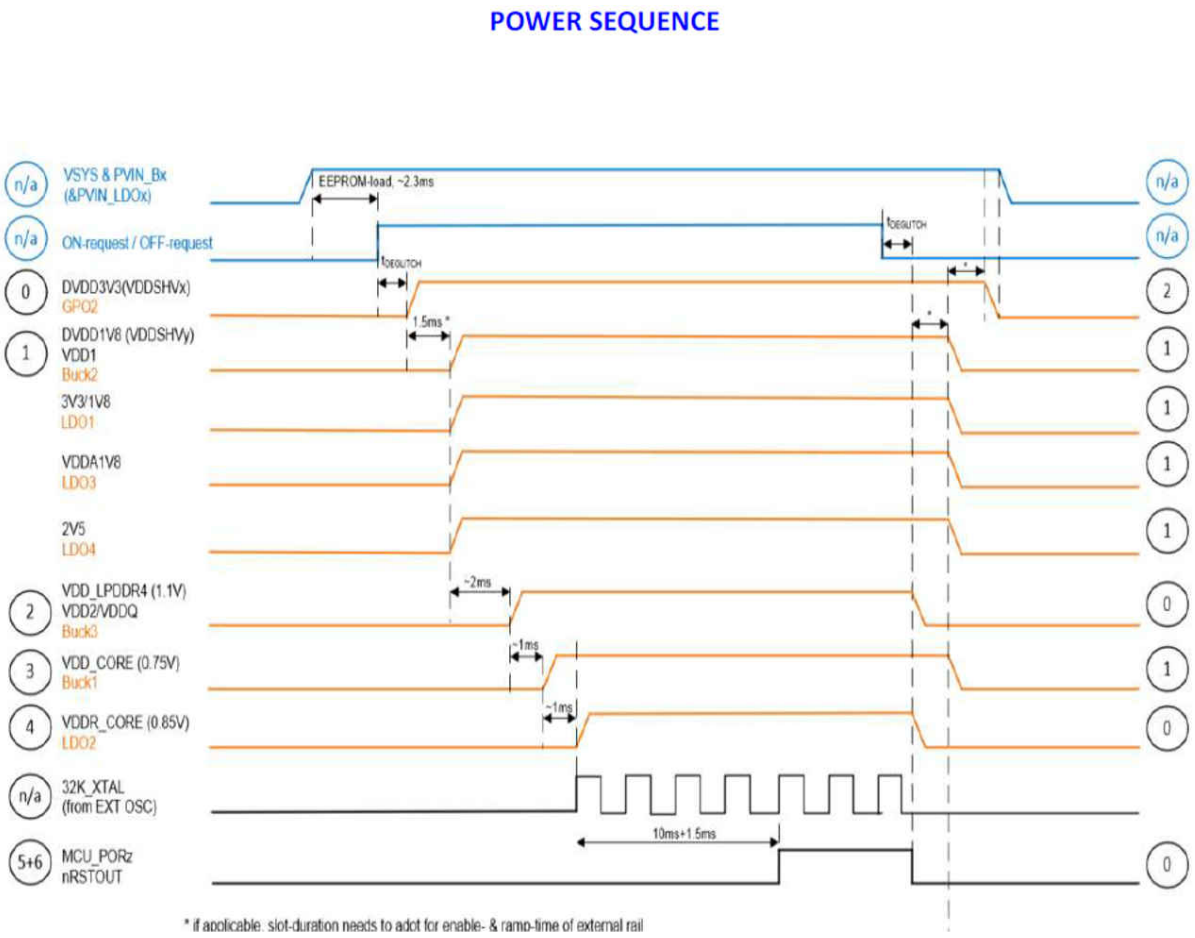


Figure 4-4. Power-Up and Power-Down Sequencing

4.3.6 SOC Power

The SoC Core voltage (VDD_CORE) of the AM64x SoC is set to 0.75 V. SoC Array Core Voltage (VDDR_CORE) and other array core voltages (VDDA_0P85_SERDES0_C, VDDA_0P85_SERDES0, VDDA_0P85_USB0, VDD_DLL_MMC0, and VDD_MMC0) are configured to 0.85 V and are supplied through a common rail.

The SoC has different IO groups. Each IO group is powered by specific power supplies as given in Table 4-6.

Table 4-6. SoC Power Supply

Sl.No	Power Supply	SoC Supply Rails	IO Power Group	Power
1	VDDAR_CORE	VDDA_0P85_SERDES0	SERDES0	0.85
		VDDA_0P85_SERDES0_C		0.85
		VDDA_0P85_USB0	USB0	0.85
		VDD_MMC0	MMC0	0.85
		VDDR_CORE	CORE	0.85
2	SoC_DVDD3V3	VDDSHV_MCU	MCU	3.3
		VDDA_3P3_USB0	USB0	3.3
		VDDSHV0	General	3.3
		VDDSHV1	PRG0	3.3
		VDDSHV2	PRG1	3.3
		VDDSHV3	GPMC	3.3
		VMON_3P3_MCU		3.3
		VMON_3P3_SOC		3.3
3	VDDA_1V8_MCU	VDDA_MCU	MCU	1.8
4	VDDA_1V8_SERDES	VDDA_1P8_SERDES0	SERDES0	1.8
5	VDDA_1V8_USB0	VDDA_1P8_USB0	USB0	1.8
6	VDDA_1V8	VDDS_OSC	OSC0	1.8
		VDDA_TEMP_0/1		1.8
		VDDA_PLL_0/1/2		1.8
7	VDDS_DDR	VDDS_DDR	DDR0	1.1
		VDDS_DDR_C		1.1
8	SOC_DVDD1V8	VDDSHV4	FLASH	1.8
		VDDS_MMC0	MMC0	1.8
		VMON_1P8_MCU		1.8
		VMON_1P8_SOC		1.8
9	VDDSHV_SD_IO	VDDSHV5	MMC1	3.3
10	VDDS_MMC0/ ADC0_VREFP	VDDS_MMC0	MMC0	0

4.4 Configuration

4.4.1 Boot Modes

The boot mode for the SK EVM board is defined by two banks of switches SW2 and SW3 or by the I2C buffer connected to the test automation connector. This allows for AM64x boot mode control by either the user (DIP Switch Control) or the test automation header. All the boot mode pins require at the minimum a footprint for a pull-up or pull-down resistor. Any boot mode pin that must be toggled to support a needed boot mode must have a weak pull-down resistor and a switch (416131160808 from Wurth) capable of connecting a stronger pull-up resistor. The switch will disconnect the pull-up resistor in the OFF position. For boot mode pins that are not controlled by switches, pull-up and pull-down resistor pads should be included. Various boot modes for AM64x must be controlled by the user with the help of 8-Bit DIP switches. The following boot modes are supported by SK EVM:

- OSPI
- MMC1 - SD-Card
- CSPW Ethernet
- USB devices

The boot mode pins of the SoC have associated alternate functions during normal operation. Hence isolation is provided using Buffer ICs to cater for alternate pin functionality. The output of the buffer is connected to the bootmode pins on the AM64x and the output is enabled when the bootmode is needed during a reset cycle. The input to the buffer is connected to the DIP switch circuit and to the output of an I2C buffer set by the test automation circuit. If the test automation circuit is going to control the bootmode, all the switches will manually be set to the OFF position. The bootmode buffer should be powered by an always on power supply to ensure that the bootmode remains present even if the SoC power is cycled..

Table 4-7 provides guidance to select the boot mode before the device is powered up.

Table 4-7. BOOT-MODE Pin Mapping

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Backup Boot Mode Configuration	Backup Boot Mode			Primary Boot Mode Configuration			Primary Boot Mode				PLL Configuration		

• BOOT-MODE [0:2] – Denote system clock frequency for PLL configuration. By default this bits are set for 25 MHz.

Table 4-8 gives details ON PLL reference clock selection.

Table 4-8. PLL Reference Clock Selection BOOTMODE [2:0]

SW3.6	SW3.7	SW3.8	PLL REF CLK (MHz)
OFF	OFF	OFF	19.2
OFF	OFF	ON	20
OFF	ON	OFF	24
OFF	ON	ON	25
ON	OFF	OFF	26
ON	OFF	ON	27
ON	ON	OFF	Reserved
ON	ON	ON	No PLL Configuration Done (slow speed backup)

• BOOT-MODE [3:6] – This provides primary boot mode configuration to select the requested boot mode after POR, that is, the peripheral/memory to boot from. Table 4-9 provides primary boot device selection details.

Table 4-9. Boot Device Selection BOOT-MODE [6:3]

SW3.2	SW3.3	SW3.4	SW3.5	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Reserved
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	Ethernet RGMII
OFF	ON	OFF	ON	Ethernet RMII
OFF	ON	ON	OFF	I2C
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMC/SD card
ON	OFF	OFF	ON	emmc
ON	OFF	ON	OFF	USB
ON	OFF	ON	ON	Reserved
ON	ON	OFF	OFF	GPMC NOR
ON	ON	OFF	ON	PCIe
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No boot/Dev Boot

• BOOT-MODE [10:12] – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.

Table 4-10 provides backup boot mode selection details.

Table 4-10. Backup Boot Mode Selection BOOT-MODE [12:10]

SW2.4	SW2.5	SW2.6	Backup Boot Device Selected
OFF	OFF	OFF	None (No backup mode)
OFF	OFF	ON	USB
OFF	ON	OFF	Reserved
OFF	ON	ON	UART
ON	OFF	OFF	Ethernet
ON	OFF	ON	MMC/SD
ON	ON	OFF	SPI
ON	ON	ON	I2C

• BOOT-MODE [9:7] – These pins provide optional settings and are used in conjunction with the primary boot device selected.

Table 4-11 gives primary boot media configuration details.

Table 4-11. Primary Boot Media Configuration BOOT-MODE [9:7]

SW2.7	SW2.8	SW3.1	Boot Device
Reserved			Reserved
Speed	Iclk	Csel	OSPI
Reserved	Iclk	Csel	QSPI
Reserved	Mode	Csel	SPI
Clkout	Delay	Link stat	Ethernet RGMII
Clkout	Clk src	Reserved	Ethernet RMII
Bus Reset	Reserved	Addr	I2C
Reserved		Reserved	UART
Port	Reserved	Fs/raw	MMC/ SD card

Table 4-11. Primary Boot Media Configuration BOOT-MODE [9:7] (continued)

SW2.7	SW2.8	SW3.1	Boot Device
Reserved		voltage	eMMC
Reserved	Mode	Lane swap	USB
Reserved			Reserved
Reserved			GPMC NOR
Reserved		Clocking	PCIe
Speed	Pin Cmd	Csel	xSPI
Reserved		No/Dev	No boot/Dev Boot

• BOOT-MODE [13] – These pins provide optional settings and are used in conjunction with the backup boot device devices. Refer to the TRM for more details on bit details. Switch SW2.6 when ON sets 1 and sets 0 if OFF.

• BOOT-MODE [14:15] – Reserved.

Table 4-12 provides backup boot media configuration options.

Table 4-12. Backup Boot Media Configuration BOOT-MODE [13]

SW2.3	Boot Device
Reserved	None
Mode	USB
Reserved	Reserved
Reserved	UART
IF	Ethernet
Port	MMC/SD
Reserved	SPI
Reserved	I2C

4.5 JTAG

The SKEVM board includes XDS110 class on board emulation and a 20-pin cTI header to support TI internal testing of software builds. The SKEVM board includes the circuitry needed for XDS110 emulation. The connection for the emulator uses an USB2.0 micro-B connector J12 and the circuit acts as a powered USB slave device. The VBUS power from the connector is used to power the emulation circuit such that connection to the emulator is not lost when the power to the EVM is removed. Voltage translation buffers are needed to isolate the XDS110 circuit from the rest of the EVM. Additionally, XDS110 also offers UART to USB signal translation on the same USB port. UART1 of SoC MAIN Domain without flow control is connected to XDS110 UART port via an isolator.

Optionally, JTAG interface on SKEVM is also provided through 20-pin standard JTAG cTI Header J14. This allows the user to connect an external JTAG Emulator cable. Voltage translation buffers are used to isolate the JTAG signals from cTI header from the rest of the EVM. The output from the voltage translators from XDS110 section and cTI Header section is muxed and connected to SoC AM64x JTAG interface. If a connection to the cTI 20-pin JTAG connector is sensed using a present detect circuit, the mux will be set to route the 20-pin signals to the AM64x in place of the on-board emulation circuit.

The pin-outs of cTI 20-pin JTAG connector J14 are given in Table 4-13. An ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ±15-kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8-kV contact discharge and ±12- kV air-gap discharge.

Table 4-13. cTI 20 Pin Connector (J14) Pin-outs

Pin No.	Signal	Pin No.	Signal
1	JTAG_TMS	11	JTAG_cTI_TCK
2	JTAG_TRST#	12	DGND

Table 4-13. cTI 20 Pin Connector (J14) Pin-outs (continued)

Pin No.	Signal	Pin No.	Signal
3	JTAG_TDI	13	JTAG_EMU0
4	JTAG_TDIS	14	JTAG_EMU1
5	VCC_3V3_SYS	15	JTAG_EMU_RSTN
6	NC	16	DGND
7	JTAG_TDO	17	NC
8	SEL_XDS110_INV	18	NC
9	JTAG_cTI_RTCK	19	NC
10	DGND	20	DGND

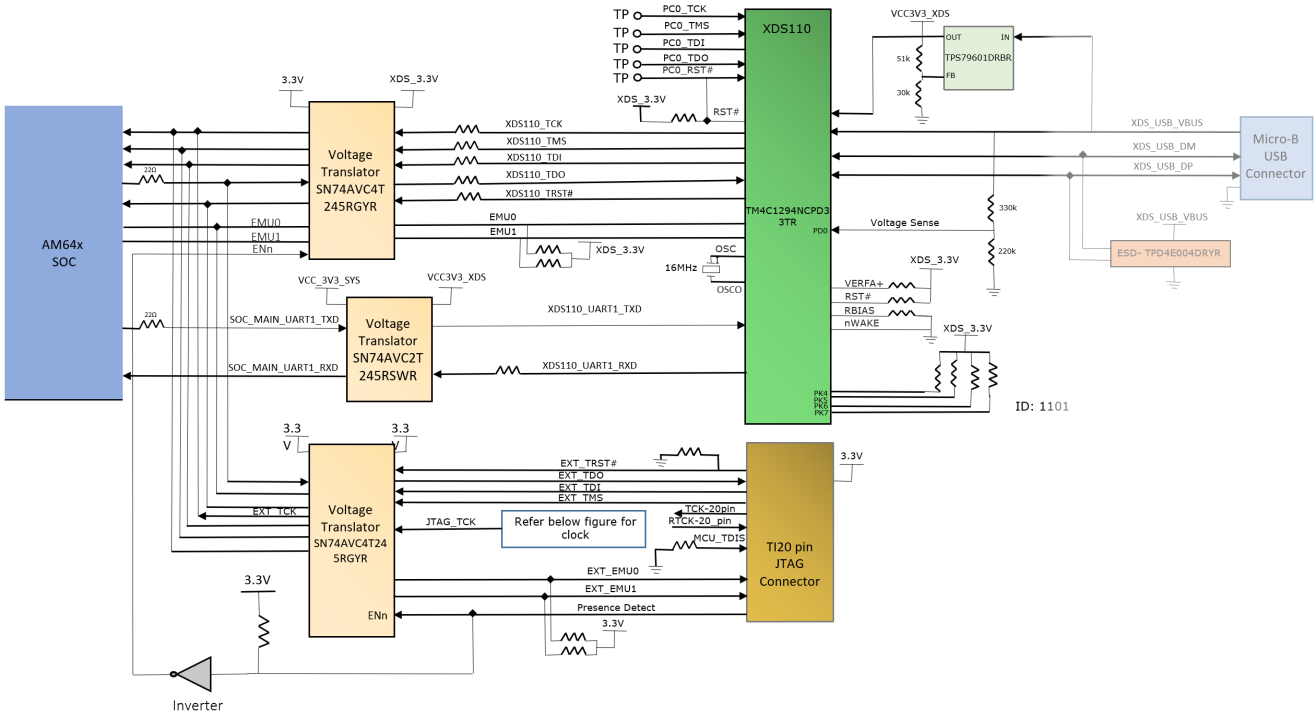


Figure 4-5. JTAG Interface

4.6 Test Automation

The SKEVM has a 40-pin test automation header (J16) to allow an external controller to manipulate some basic operations such as Power Down, POR, Warm Reset, Boot Mode control, and so forth. The test automation header includes four GPIOs and two I2C interfaces (I2C1, Boot mode I2C0).

The test automation circuit has voltage translation circuits so that the controller is isolated from the IO voltages used by the AM64x. Boot mode for the AM64x must be controlled by either the user using DIP Switches or the test automation header through the I2C IO Expander.

Boot Mode Buffers are used to isolate the Boot Mode controls driven through DIP Switches or the I2C IO Expanders. Power to Test Automation Circuit is provided from a Power Mux (TPS2121RUXT), which has the input supplies VCC3V3_TA supply generated from a dedicated regulator and VCC3V3_XDS generated from an LDO (it is the supply for XDS110 Debugger section). The basic controls of test automation header J16 are as follows. Table 4-14 gives details about test automation header signals.

Optionally, the Test Automation header functionality can be implemented by the XDS110 controller. Hence resistor options (R420, R421, R422, R423, R424, R425, R426, R427, R436, R437, R438, and R439) are provided for Power Down, POR, Warm Reset, Boot Mode controls, and GPIO signals. By default, these resistors are made as DNI so that an external controller controls the basic operations through the Automation header. When the firmware for the XDS110 is developed, mount the above mentioned resistors and DNI the resistors

R380, R381, R382, R383, R384, R385, R386, R432, R433, R434, and R435 to control the basic operations through the XDS110 microcontroller.

Proper Isolation to be provided on Boot Mode signals to allow normal operation. Two I2Cs are available on the test automation header. SoC _I2C [1] is connected to test automation header to communicate with external controller, and the other I2C is connected to Boot mode buffer to control boot mode of AM64x.

Table 4-14 lists the reset signals routed from test automation header. The boot mode for the AM64x can be controlled by either the user or the test automation header.

Table 4-14. List of Signals Routed to Test Automation Header J16

Signal	Signal Type	Function
POWER_DOWN	GPIO	Used to Power down the Board
PORZn	GPIO	Used to Reset the SoC PORz
WARM_RESETn	GPIO	Used to Reset the SoC Warmreset
GPIO1	GPIO	Used to Generate the interrupt on GPIO1_59_INTn Pin
GPIO2	GPIO	GPIO for communication with AM64X
GPIO3	GPIO	Used to Enable the BOOTMODE Buffer
GPIO4	GPIO	Used to Reset the Boot mode IO Expander
Bootmode I2C0	I2C	Communicates with boot mode I2C buffer
I2C1	I2C	Communicates with AM64x

If the test automation circuit is going to control the boot mode, all the switches must be manually be set to the off position. The pins used for boot mode also have other functions which are isolated by disabling the boot mode buffer during normal operation. Figure 4-6 shows the test automation signal connection with AM64x.

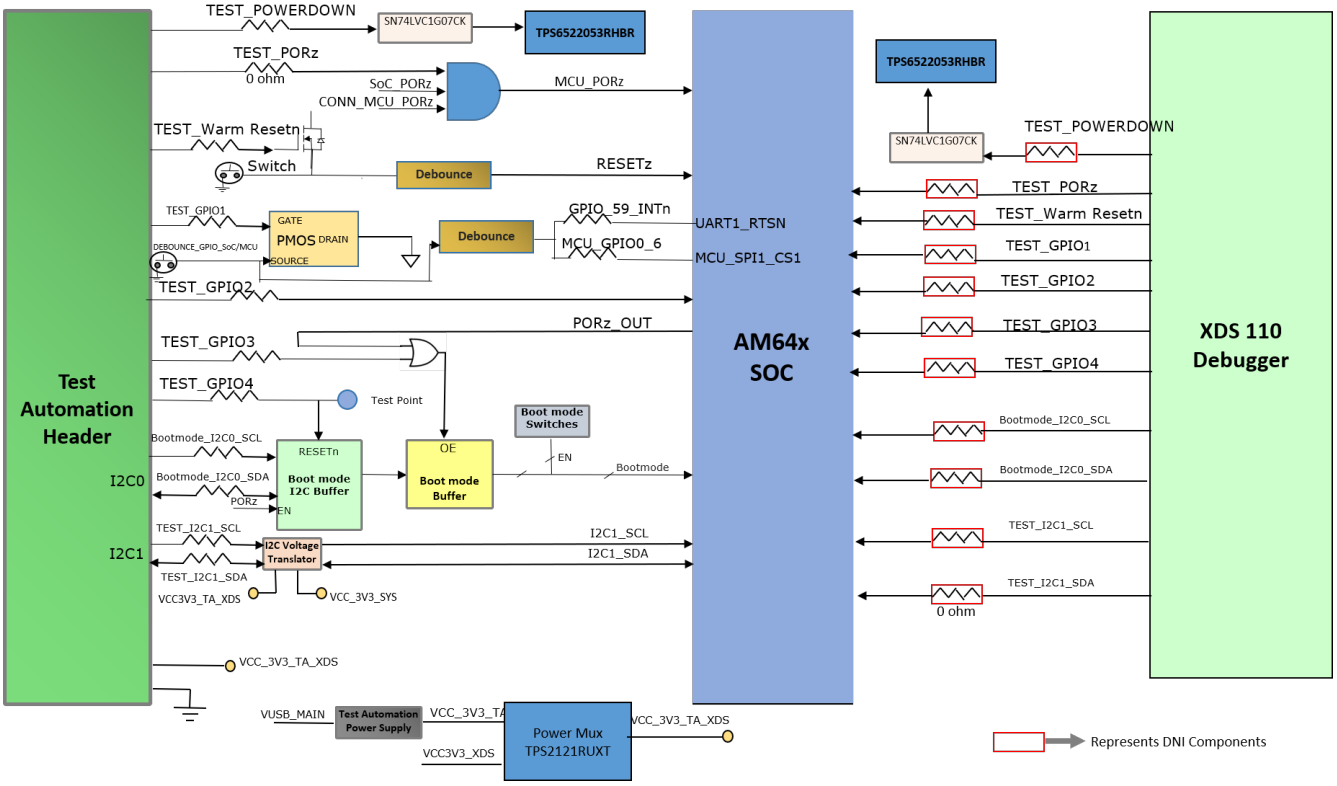


Figure 4-6. Test Automation Header

Test Automation Header signals are optionally connected to the XDS110 microcontroller through zero ohm resistors. By default, those resistors are made as DNI.

Table 4-15. Automation Header Signals Connected to XDS110

TM4C1294 PIN Name	Signal Name
PM0	TEST_POWERDOWN
PM1	TEST_PORZn
PM2	TEST_WARMRESETn
PM3	TEST_GPIO1
PM4	TEST_GPIO2
PM5	TEST_GPIO3
PM6	TEST_GPIO4
PM7	TEST_POWERDOWN
PG0	TEST_PORZn
PG1	TEST_WARMRESETn

Table 4-16 lists test automation header's pin-out and IO direction.

Table 4-16. Test Automation Header (J16) Pin-Outs

Pin No.	Signal Name	IO Direction (wrt SoC)
1	VCC3V3_TA	Power (out)
2	VCC3V3_TA	Power (out)
3	VCC3V3_TA	Power (out)
4	NC	NA
5	NC	NA
6	NC	NA
7	DGND	Ground
8	NC	NA
9	NC	NA
10	NC	NA
11	NC	NA
12	NC	NA
13	NC	NA
14	NC	NA
15	NC	NA
16	DGND	Ground
17	NC	NA
18	NC	NA
19	NC	NA
20	NC	NA
21	NC	NA
22	NC	NA
23	NC	NA
24	NC	NA
25	DGND	Ground
26	TEST_POWERDOWN	Input
27	TEST_PORZn	Input
28	TEST_WARMRESETn	Input
29	NC	NA
30	TEST_GPIO1	Bidirectional
31	TEST_GPIO2	Bidirectional
32	TEST_GPIO3	Input
33	TEST_GPIO4	Input

Table 4-16. Test Automation Header (J16) Pin-Outs (continued)

Pin No.	Signal Name	IO Direction (wrt SoC)
34	DGND	Ground
35	NC	NA
36	SOC_I2C1_TA_SCL	Bidirectional
37	BOOTMODE_I2C_SCL	Bidirectional
38	SOC_I2C1_TA_SDA	Bidirectional
39	BOOTMODE_I2C_SDA	Bidirectional
40	DGND	Ground
41	DGND	Ground
42	DGND	Ground

4.7 UART Interface

The two UART ports MAIN_UART0 and MCU_UART0 provided by AM64x are connected to two channel USB to UART Bridge (CP2105) and terminated to a USB Micro B Connector J11. Two ports of the CP2105 are connected to MAIN_UART0 and MCU_UART0 with the RXD, TXD, RTS, and CTS signals.

The USB interface circuit is used in bus powered configuration and a voltage translator (SN74AVC4T245) is used to isolate AM64x IOs. The CP2105 includes an on-chip 5-V to 3.45-V voltage regulator. LD18 is used to indicate power good status of CP2105. This allows the CP2105 to be configured as a USB bus-powered device. The voltage regulator output appears on the VDD pin and can be used to drive the IO supply and one of the supply rails of the voltage translator. Internally, the same VDD is used to operate the core section of CP2105. CP2105 also includes an integrated clock and hence no external crystal is required. MAIN_UART0 and MCU_UART0 from SOC are at 3.3-V IO level. The devices use the internal POR circuit. For normal operation, the nRST pin must be pulled up to 3V3 supply through the 10K resistor. Because the device operates in bus powered configuration, VBUS from the USB connector must be connected to the “REGIN” pin of CP2105 to serve as the input for the internal regulator.

A ESD protection is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ±15-kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8-kV contact discharge and ±12- kV air-gap Discharge.

Figure 4-7 shows the dual UART to USB bridge connection with AM64x.

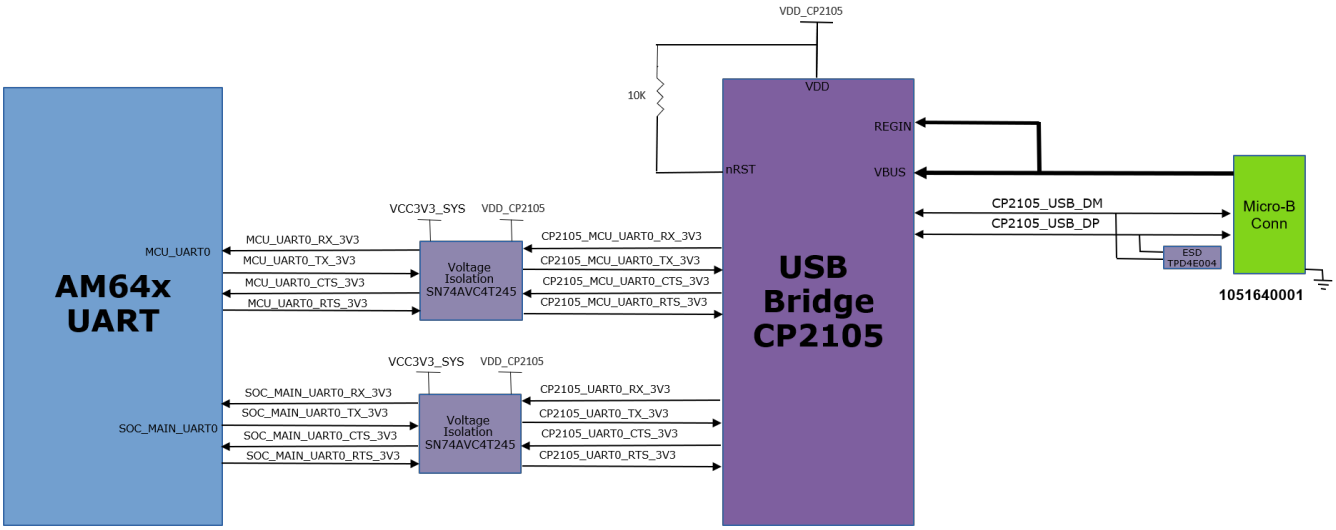


Figure 4-7. UART Interface

4.8 Memory Interfaces

4.8.1 LPDDR4 Interface

The SK EVM has 2GB, 16-bit wide LPDDR4 memory with operating data rate of 1666 MTps. Micron's MT53E1G16D1FW-046 WT: A is used. The LPDDR memory is mounted on-board (single chip) and requires 1.1 V and thus reduces power demand. The LPDDR4 device requires I/O power and core 2 power of 1.1 V, DRAM activating power supply (core 1) of 1.8 V.

LPDDR4 reset is active high signal, which is controlled by SOC, and the signal is pulled low to set the default active state and a footprint for pull-down is also provided. A 240-Ω resistor is connected from ZQ pin to 1.1-V supply for the LPDDR4 device and the SoC DDR0_CAL pin is grounded.

The ODT (On Die Termination) is applied to DQ, DQS, and DM_n signals. The device is capable of providing three different ODT modes: Nominal, Dynamic, and Park with termination values: RTT (Park), RTT (NOM), and RTT (WR). Figure 4-8 shows the DDR interface between LPDDR4 and AM64x.

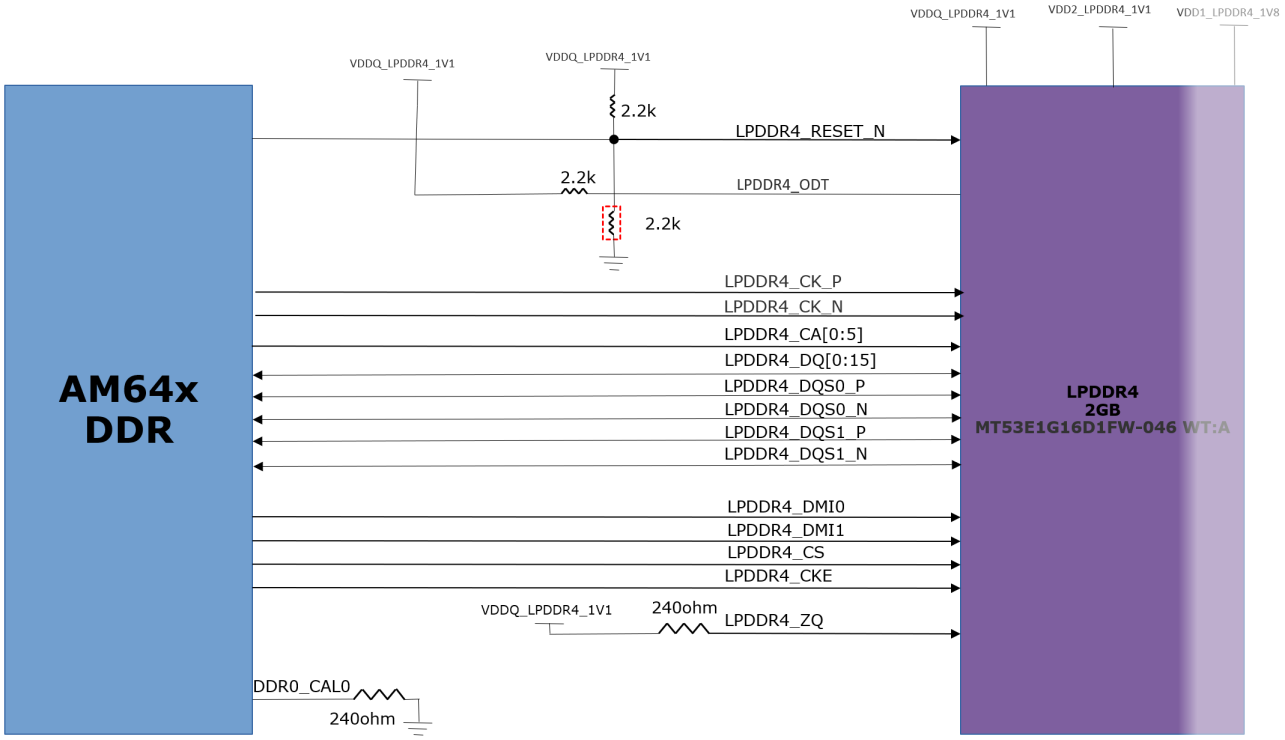


Figure 4-8. LPDDR4 Interface

4.8.2 MMC Interface

The AM64x processor provides two MMC interfaces. One is connected to Wilink Module, and the other is used for micro SD card interface.

4.8.2.1 Micro SD Interface

The SKEVM board provides a micro SD card interface connected to the MMC1 port of the AM64x SOC. The micro-SD card interface supports 16 GB density with UHS1 operation including IO operations at both 1.8 V and 3.3 V. The circuit included in AM64x SoC to support the IO voltage switching is connected to IO voltage of SD signals to allow the processor to negotiate IO voltage. For high-speed cards, the ROM Code of SOC attempts to find the fastest speed that the card and controller can support and have a transition to 1.8 V. The internal SDIO LDO output from the SOC available at CAP_VDDSHV_SDLDO pin is connected to IO voltage of SD signals and VDDSHV_MMC1 power pins of SOC, which is the power supply for MMC1 interface.

An ESD protection device (TPD6E001RSE) is provided for data, clock, and command signals. TPD6E001RSE is a line termination device with integrated TVS diodes providing system-level IEC 61000-4-2 ESD protection, ± 8-kV contact discharge, and ± 15kV air-gap discharge.

The SD card is set to operate in SD mode. The CD (card detect) pin of SD card connector is pulled high and connected to the CD pin of the SOC. Figure 4-9 shows the block diagram of the micro-SD card interface.

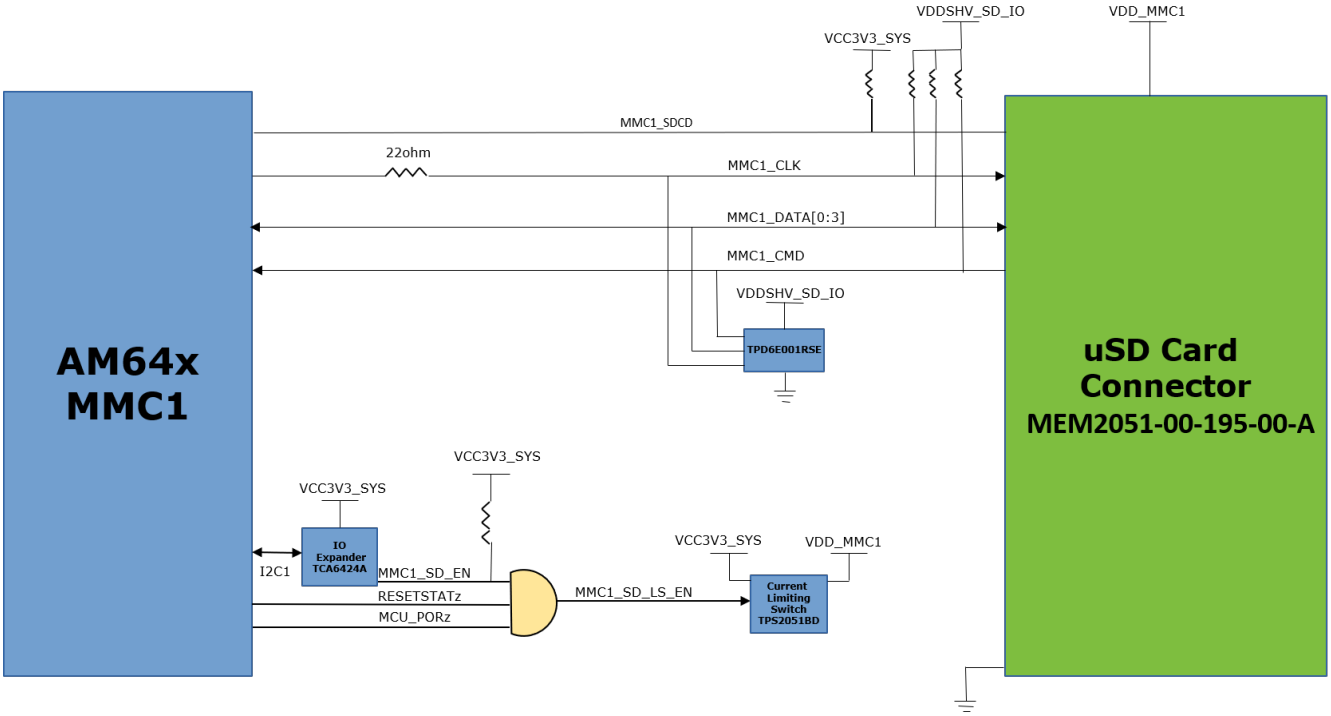


Figure 4-9. Micro SD Interface

4.8.2.2 WiLink Interface

The SKEVM board has WiLink Module (WL1837MODGIMOCT) from TI connected to the MMC0 port of the AM64x SoC. The WL1837MOD is a Wi-Fi, dual-band, 2.4- and 5-GHz module solution with two antennas supporting Industrial temperature grade. The Module is connected to 4-bit IO of the MMC0 interface supporting IEEE standard 802.11a/b/g/n data rates with 20 or 40-MHz SISO or 20-MHz MIMO. The Module offers high throughput and extended range along with Wi-Fi and Bluetooth coexistence in a power-optimized design.

The device supports the following Bluetooth features:

- Bluetooth 4.2 secure connection as well as CSA2
- Concurrent operation and built-in coexisting and prioritization handling of Bluetooth and Bluetooth low energy wireless technology, audio processing, and WLAN
- Dedicated audio processor supporting on-chip SBC encoding + A2DP
- Assisted A2DP (A3DP): SBC encoding implemented internally
- Assisted WB-speech (AWBS): modified SBC codec implemented internally. Figure 4-10 shows the block diagram of Wilink module interfaced with AM64x.

SKEVM does not support A2DP BT Audio profile or HF profile.

The Module requires two power supplies, 3.3 V for VBAT_IN and 1.8 V for VIO_IN. The MMC0 interface of SOC is powered by VDDSHV_MMC0 power supply, which is connected to 1.8-V IO supply. Bluetooth UART signals, enable of BT and WLAN and WLAN_IRQ signals are connected to GPIO's of AM64x using level translator (SN74AVC4T245RSVR). Input clock is provided by using 32.768 KHz oscillator (ASDK2-32.768KHZ-LRT).

Test points are provided on MMC0_DAT [4:7] pins of SOC and WL_GPIO, BT_UART_DEBUG, WL_UART_DEBUG pins on WL1837 Module.

A 14-pin Wilink connector is also provided. An external Wi-Fi module (Bluetooth module is not supported) can be communicated with SoC through the 14-pin WiLink connector. By default, the 14-pin Wilink connector and 0E resistors are not populated on the signals which are connected to the 14-pin Wilink connector.

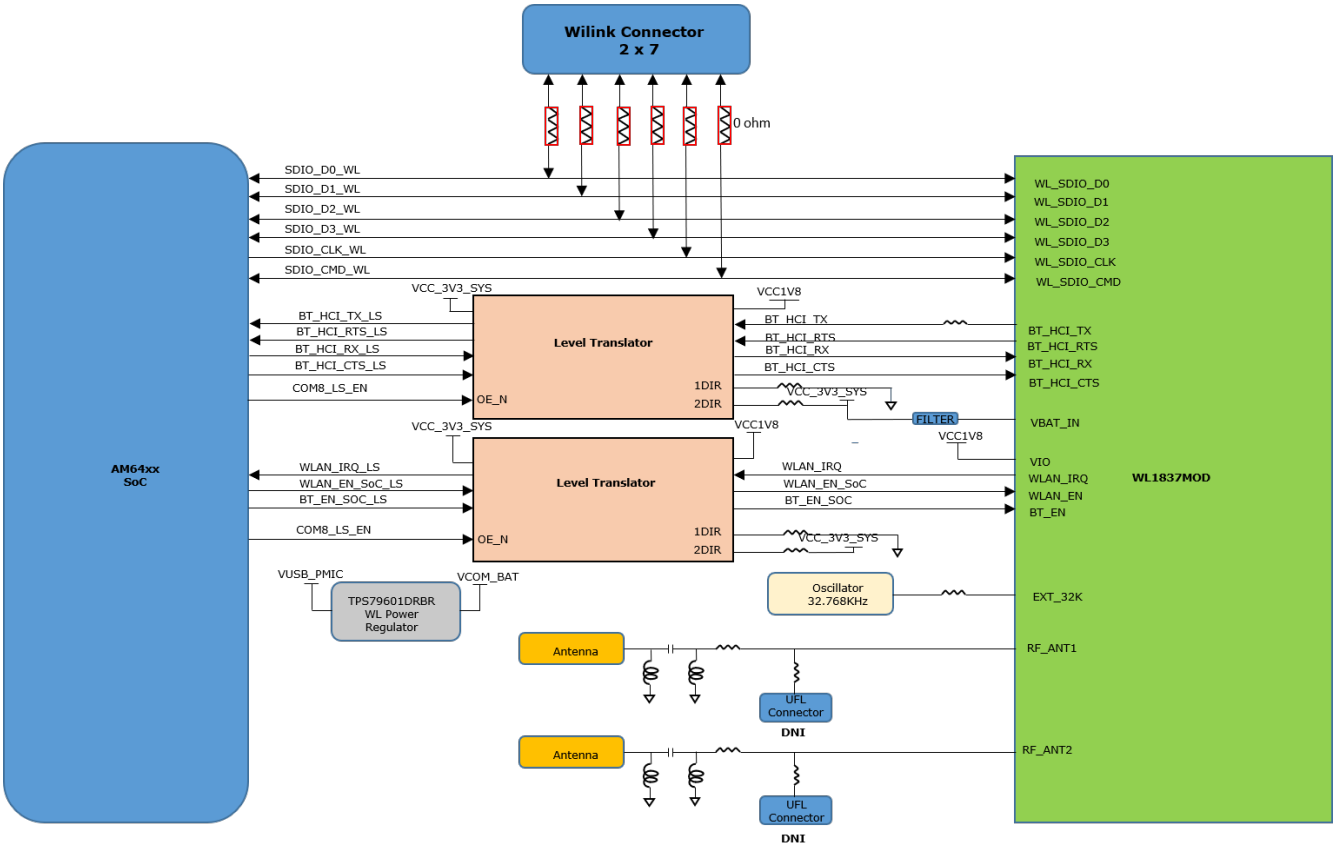


Figure 4-10. WiLink Module Interface

4.8.2.3 OSPI Interface

The SK EVM board has a 512-Mbit OSPI memory device of part number S28HS512TGABHM010 from Cypress connected to the OSPI0 interface of the AM64x SOC. The OSPI interface supports memory speed up to 166 MHz. The OSPI flash is powered by 1.8-V IO supply. The 1.8-V supply is provided to both the VCC and VCCQ pins of the flash memory.

The reset for the flash is connected to a circuit that ANDs the RESETSTATz, PORz_OUT, and OSPI0_CSN2 (GPIO_OSPI_RSTn) from SoC. This applies reset for warm and cold reset. A pull-up is provided on GPIO_OSPI_RSTn coming from the SOC pin to set the default active state.

Two signals are routed to OSPI0_DQS:

1. OSPI0_DQS from the memory device
2. OSPI0_LBCLK from SoC

To route DQS from memory device: DNI R33 and R39.

To route OSPI0_LBCLK from SoC: Mount R33 and R39.

OSPI and QSPI implementation: 0-ohm resistors are provided for DATA [7:0], DQS, INT# and CLK signals. Footprints to mount external pull up resistors are provided on DATA [7:0] to prevent bus floating.

Figure 4-11 shows the OSPI interface block diagram for AM64x SK EVM.

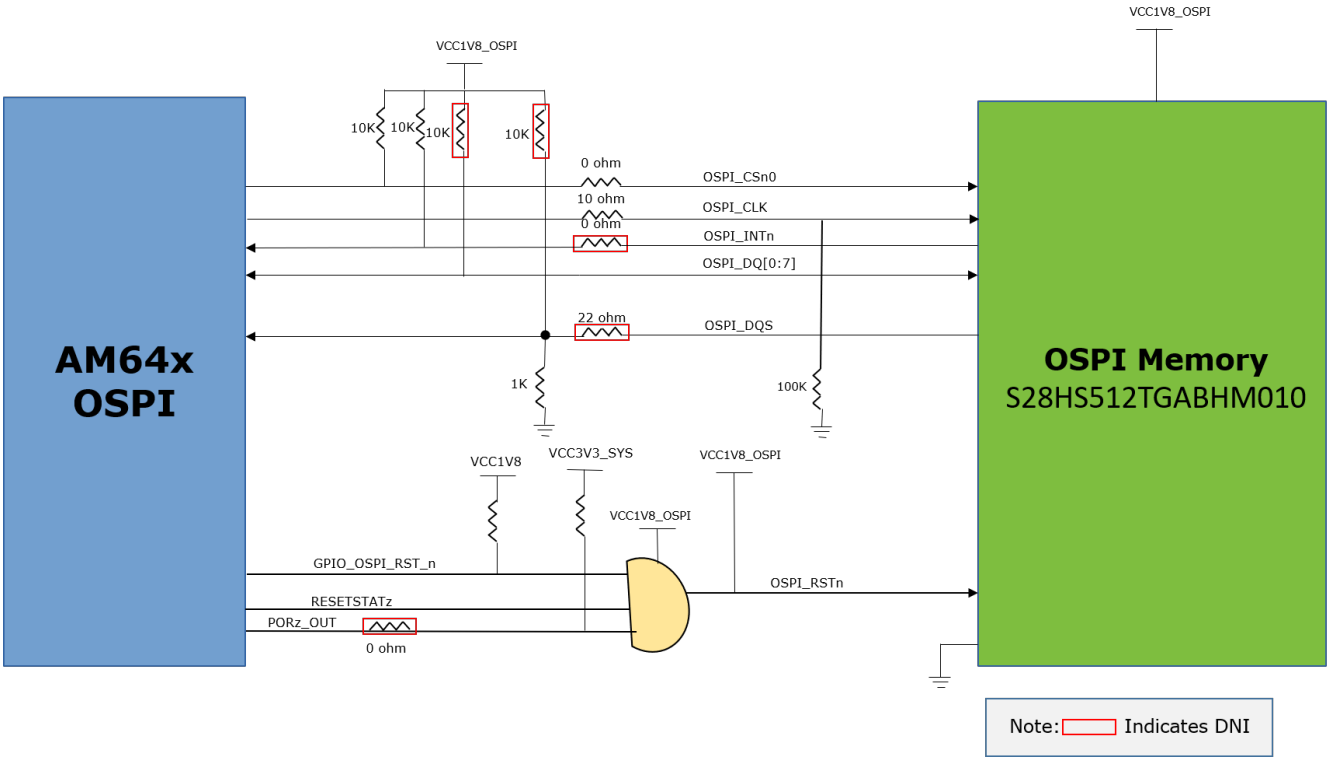


Figure 4-11. OSPI Interface

4.8.2.4 Board ID EEPROM Interface

The AM64x processor is identified by its version and serial number, which are stored in the onboard EEPROM. The Board ID memory is configured to respond to address 0x51. AT24C512C-MAHM-T from Microchip is used, and is interfaced to the I2C0 port of the SOC. The I2C address of the EEPROM can be modified by driving the A0, A1, A2 pins to LOW. The write-protect input, when connected to GND, allows normal write operations. When the WP pin is connected directly to VCC, all write operations to the protected memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND. WP is connected through GND through a 10k resistor.

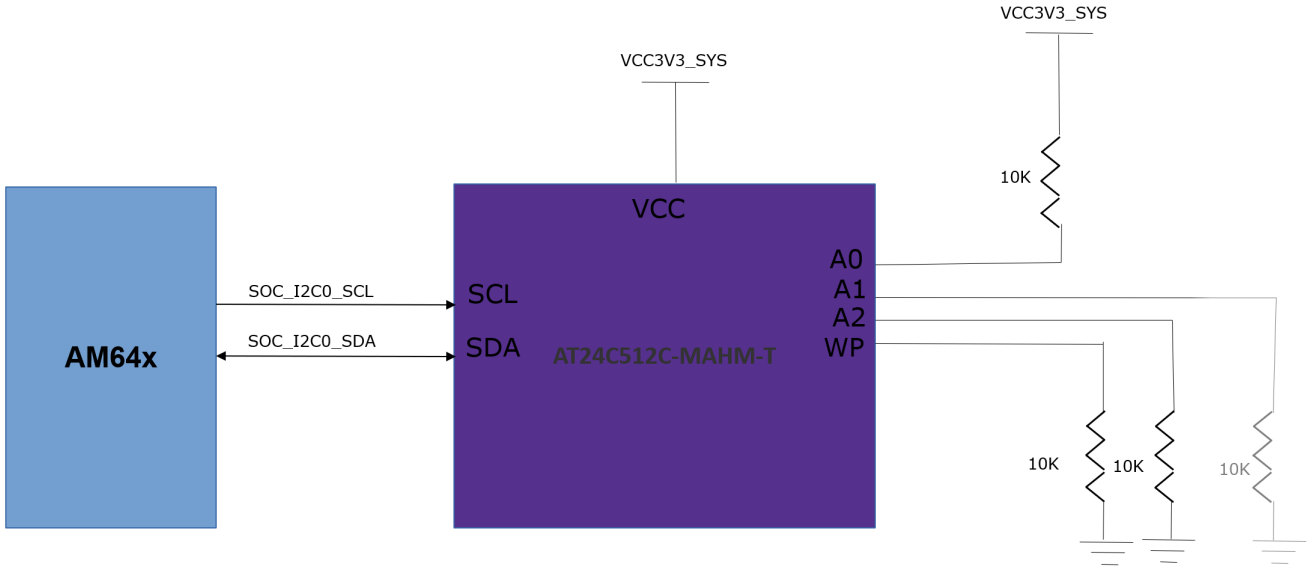


Figure 4-12. Board ID EEPROM

4.9 Ethernet Interface

SKEVM offers two Ethernet ports of 1Gigabit speed for external communication. Two channels of RGMII Gigabit Ethernet CPSW ports from the AM64x SoC should be connected to two separate Gigabit Ethernet PHY transceivers DP83867, which is finally terminated on two RJ45 connectors with integrated magnetics.

The 48-pin version of the PHY DP83867 should be configured to advertise 1-Gb operation with the internal delay set to accommodate the internal delay inside the AM64x. The RGMII1 signals shared with PRG1 should be used for the RX path to allow the PRG0 to be connected to the PRU header on the board. CPSW_RGMII1 and CPSW_RGMII2 ports of PRG1 share a common MDIO bus to communicate with the external PHY transceiver.

The two port RJ45 connector (LPJG16314A4NL) used on the board for Ethernet 10/100/1G connectivity. RJ45 connectors have integrated magnetics and LEDs for indicating 1000BASE-T link and receive or transmit activity.

4.9.1 DP83867 PHY Default Configuration

The DP83867 PHY uses four level configurations based on resistor strapping, which generate four distinct voltages ranges. The resistors are connected to the RX data and control pins, which are normally driven by the PHY and are inputs to the AM64x. The voltage range for each mode is shown below.

Mode 1 - 0 V to 0.3234 V

Mode 2 – 0.462 V to 0.6303 V

Mode 3 – 0.7425 V to 0.9372 V

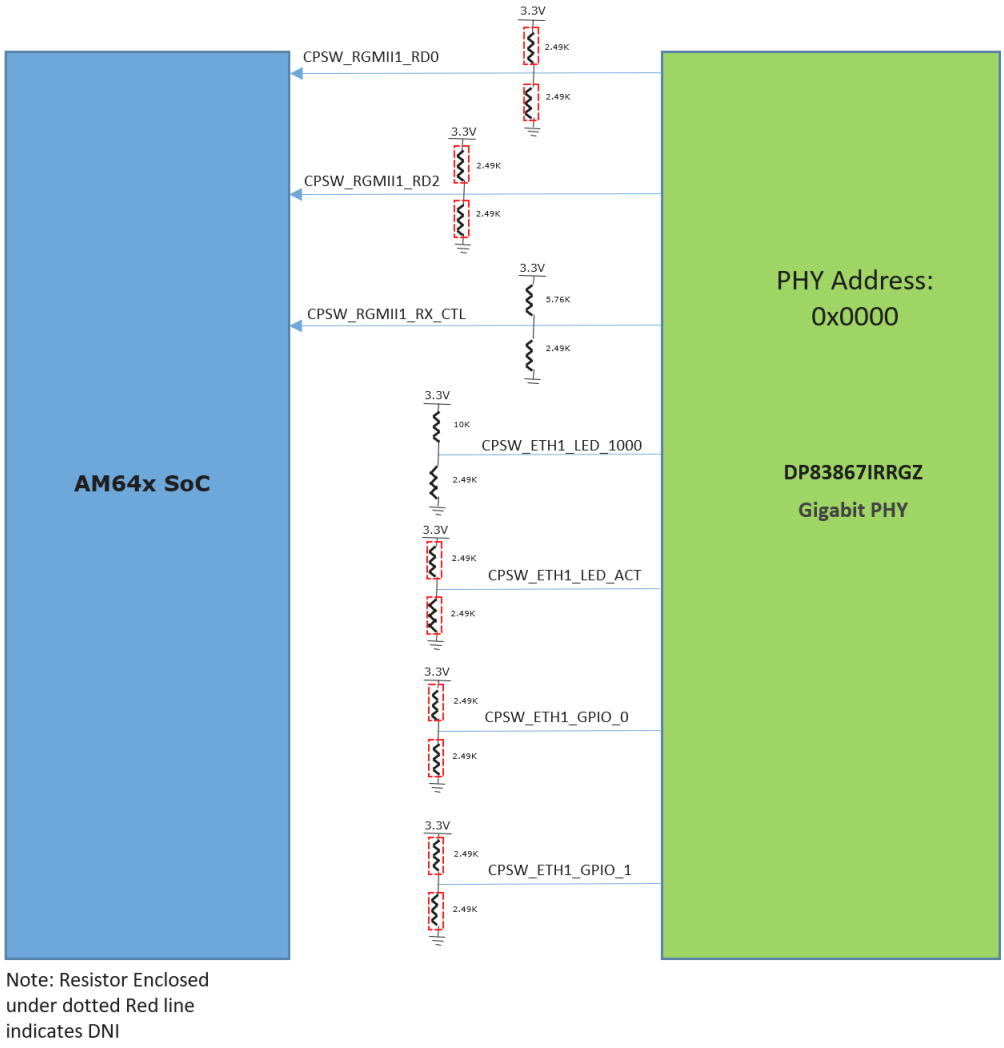
Mode 4 – 2.2902 V to 2.904 V

The DP83867 device includes an internal pull-down resistor. The value of the external pull resistors is selected to provide voltage at the pins of the AM64x as close to ground or 3.3 V as possible. The strapping is shown in Figure 4-13. The strap values are given in Table 4-17

Table 4-17. Strap Value Configuration

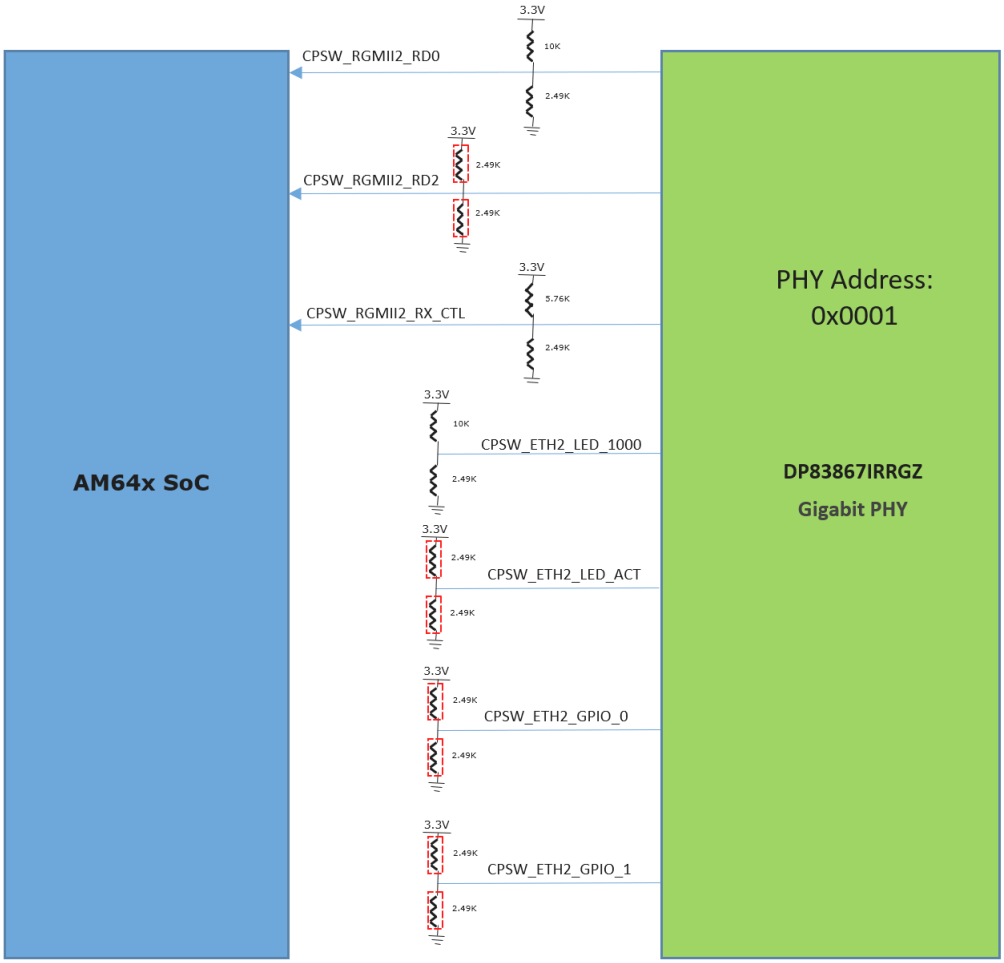
Mode	Target Voltage			Ideal Rhi (k Ω)	Ideal Rlo (k Ω)
	Vmin(V)	Vtyp(V)	Vmax(V)		
1	0	0	0.098 * VDDIO	OPEN	OPEN
2	0.140 * VDDIO	0.165 * VDDIO	0.191 * VDDIO	10	2.49
3	0.225 * VDDIO	0.255 * VDDIO	0.284 * VDDIO	5.76	2.49
4	0.694 * VDDIO	0.763 * VDDIO	0.886 * VDDIO	2.49	OPEN

Address strapping is provided for CPSW PHY-1 to set address -00000 (0h) and CPSW PHY-2 to set address 00001(01h). By default, strapping pins have internal pull-down resistors. Footprint for both pull up and pull down is provided on all the strapping pins except LED_0. LED_0 is for Mirror Enable, which is set to mode 1 by default, Mode 4 is not applicable and Mode2, Mode3 option is not desired. Default strap setting of CPSW RGM I 1Ethernet PHY and CPSW RGMII1 Ethernet PHY are given in Table 4-18 and Table 4-19.



Note: Resistor Enclosed under dotted Red line indicates DNI

Figure 4-13. CPSW Ethernet PHY-1 Strap settings



Note: Resistor Enclosed under dotted Red line indicates DNI

Figure 4-14. CPSW Ethernet PHY-2 Strap settings

Table 4-18. Default Strap Setting of CPSW RGMII-1 Ethernet PHY

Strap Setting	Pin Name	Strap Function	Mode for PRG1_PRU1, PRG1_PRU0	Value of Strap Function for PRG1	Description
PHY Address	RX_D2	PHY_AD3	1	0	PHY Address: 0000
		PHY_AD2	1	0	
	RX_D0	PHY_AD1	1	0	
		PHY_AD0	1	0	
Auto Negotiation	RX_DV/RX_CTRL	Auto- neg	3	0	Auto neg Disable=0

Table 4-18. Default Strap Setting of CPSW RGMII-1 Ethernet PHY (continued)

Strap Setting	Pin Name	Strap Function	Mode for PRG1_PRU1, PRG1_PRU0	Value of Strap Function for PRG1	Description
Modes of Operation	LED2	RGMII Clock Skew TX[1]	5	0	RGMII TX Clock Skew is set to 0 ns
		RGMII Clock Skew TX[0]	5	0	
	LED_1	RGMII Clock Skew TX[2]	5	1	
		ANEG_SEL	1	0	advertise ability of 10/100/1000
	LED_0	Mirror Enable	1	0	Mirror Enable Disabled
	GPIO_1	RGMII Clock Skew RX[2]	1	0	RGMII RX Clock Skew is set to 2 ns
		RGMII Clock Skew TX[1]	1	0	
	GPIO_0	RGMII Clock Skew RX[0]	1	0	

Table 4-19. Default Strap Setting of CPSW RGMII-2 Ethernet PHY

Strap Setting	Pin Name	Strap Function	Mode for PRG1_PRU1, PRG1_PRU0	Value of Strap Function for PRG0 and PRG1	Description
PHY Address	RX_D2	PHY_AD3	1	0	PHY Address: 0001
		PHY_AD2	1	0	
	RX_D0	PHY_AD1	2	0	
		PHY_AD0	2	1	
Auto Negotiation	RX_DV/RX_CTRL	Auto- neg	3	0	Auto neg Disable=0
Modes of Operation	LED2	RGMII Clock Skew TX[1]	5	0	RGMII TX Clock Skew is set to 0 ns
		RGMII Clock Skew TX[0]	5	0	
	LED_1	RGMII Clock Skew TX[2]	5	1	
		ANEG_SEL	1	0	advertise ability of 10/100/1000
	LED_0	Mirror Enable	1	0	Mirror Enable Disabled
	GPIO_1	RGMII Clock Skew RX[2]	1	0	RGMII RX Clock Skew is set to 2 ns
		RGMII Clock Skew TX[1]	1	0	
	GPIO_0	RGMII Clock Skew RX[0]	1	0	

4.9.2 DP83867 – Power, Clock, Reset, Interrupt, and LEDs

The PHY devices include integrated MDI termination resistors. Thus, external termination is not provided.

Power: the RGMII signals from PRG0 and PRG1 domain are at 3.3-V IO level. The Gigabit PHY device DP83867 requires I/O power of 3.3 V and analog supply of 2.5 V and 1.0 V

Clock: A 25-MHz LVCMOS clock is given to the PHYs through clock buffer LMK1C1103 (individual outputs).

Reset: The reset for PHYs is from a circuit that ANDs the PORz_OUT and GPIO from IO expander and an optional RESETSTATz from the SoC. By default, RESETSTATz is not used for resetting the PHY. The IO expander is controlled through the I2C1 port of the AM64x SOC. Footprints for both a pull-up and a pull-down

resistor are provided to the GPIO to set the default value. Each of the Ethernet PHYs have separate Reset Signals driven by GPIOs. A hardware reset is accomplished by applying a low pulse, with a duration of at least 1 micro-second to the RESET_N pin.

Interrupt: The interrupt from two CPSW RGMII PHYs from the PRG1 domain are tied together and is connected to the EXTINTN pin of AM64x SOC.

Four configurable LED pins and two GPIO of Ethernet PHY are used to indicate link status. Several functions can be multiplexed onto the LEDs for different modes of operation. The LED operation mode can be selected using the LEDCR1 register address 0x0018 on the DP83867 device. The default configuration are as follows.

LED0: By default, this pin indicates that a link is established. Additional functionality is configurable via LEDCR1 [3:0] register bits in the DP83867 device. LDE0 is not used in the CPSW PHY (DP83867), this is also a strap pin which is used to set mirror enable. Because these features are not required, the strapping for the LED0 is not provided.

LED_1: By default, this pin indicates that the 1000BASE-T link is established. This setting can be changed to auto negotiate to 10/100Mbps using the strap resistors. Additional functionality is configurable through the LEDCR1 [7:4] register bits in the DP83867 device. LED_1 is a also an strap pin which has an internal pull-down resistor to set the RGMII TX clock skew in the DP83867 device. Because this pin is set to active on both devices, this results in dim LED lighting when the LED is driven directly. Thus, a MOSFET is used to drive the LED, as shown in Figure 4-15.

LED_2: By default, this pin indicates receive or transmit activity. Additional functionality is configurable through the LEDCR1 [11:18] register bits in the DP83867 device. LED_2 is also a strap pin, which has an internal pull-down resistor to set the RGMII TX clock skew in the DP83867 device. The default condition is to auto negotiate and advertise the link as 10/100/1000Mbps, and this can be changed using the strap resistors provided. The pull up resistor is used for strap setting results in dim LED lighting when the LED is driven directly. Thus, a MOSFET is used to drive the LED, as shown in Figure 4-15.

GPIO0: In the DP83867 PHY, the GPIO can be configured to function as LED3 through the GPIO Mux Control Register 1 (GPIO_MUX_CTRL1), and the LED configuration can be set by programming the LEDCR1 register; this pin is used to indicate operation as a 100-Mbps connection. A MOSFET is used to drive the LED, as shown in Figure 4-15.

GPIO1: In the DP83867 PHY, the GPIO can be configured to function as LED3 through the GPIO Mux Control Register 1 (GPIO_MUX_CTRL1), and the LED configuration can be set by programming the LEDCR1 register, This is also a strap pin, which is used to set fast link drop (FDP); currently this is disabled.

LED indication in Ethernet RJ45 Connector: LED control is achieved through an external MOSFET.

RJ45 Connector LED Indication - CPSW (DP83867): LED1 is connected to RJ45 LED (Green) to indicate a 10/100 or 1000-MHz link, and LED2 is connected to RJ45 LED (Green) to indicate transmit/receive activity.

LED Control is achieved through an external MOSFET.

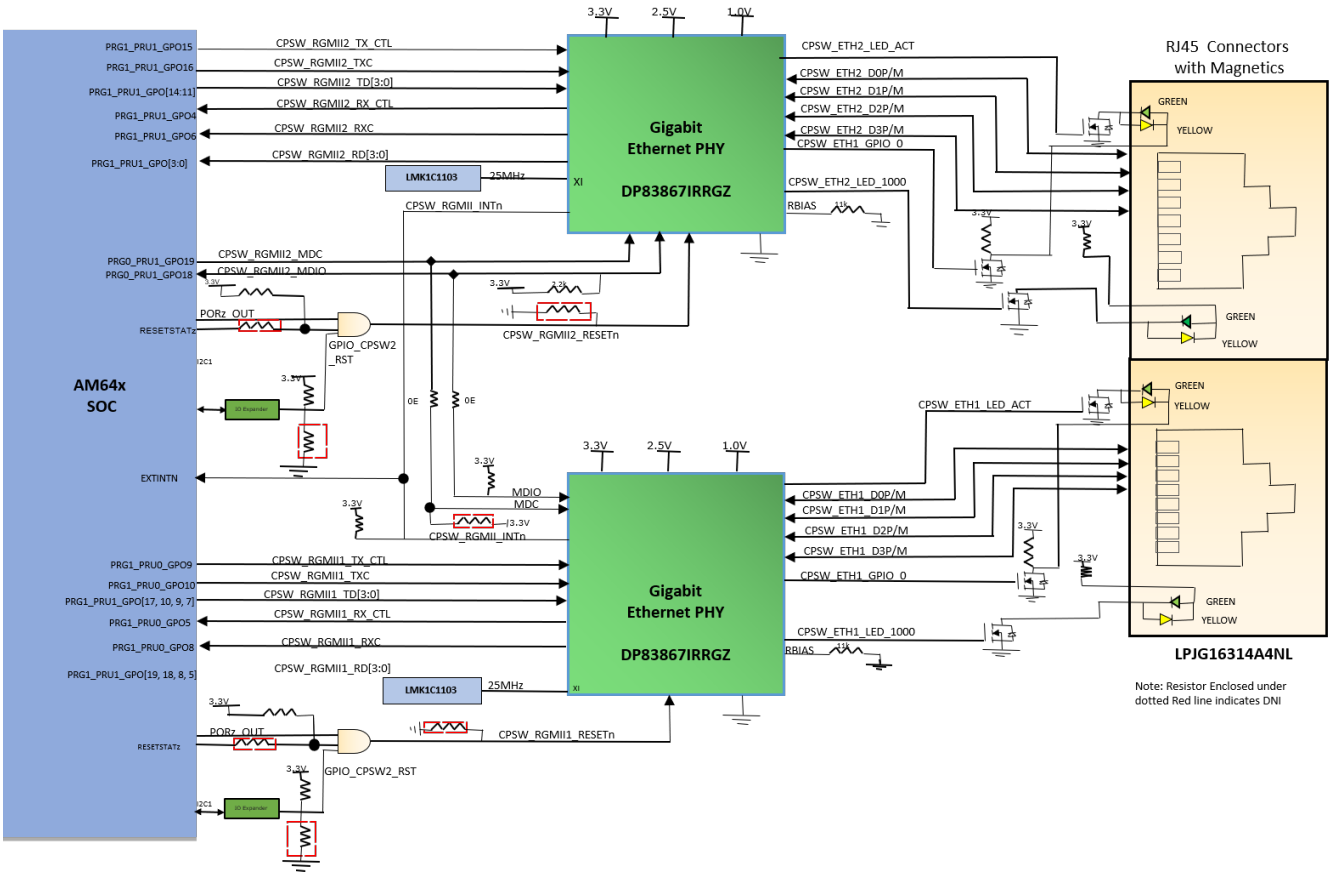


Figure 4-15. Ethernet Interface

Note

Resistors highlighted by a red color box are DNI components.

4.9.3 Industrial Application LEDs for Indication

There are 8 LEDs connected to an I2C-based LED driver (TPIC2810D), which is controlled by the SoC through the I2C1 port. These 8 LEDs can be toggled based on the user application. Primarily these eight LEDs are meant for Industrial application.

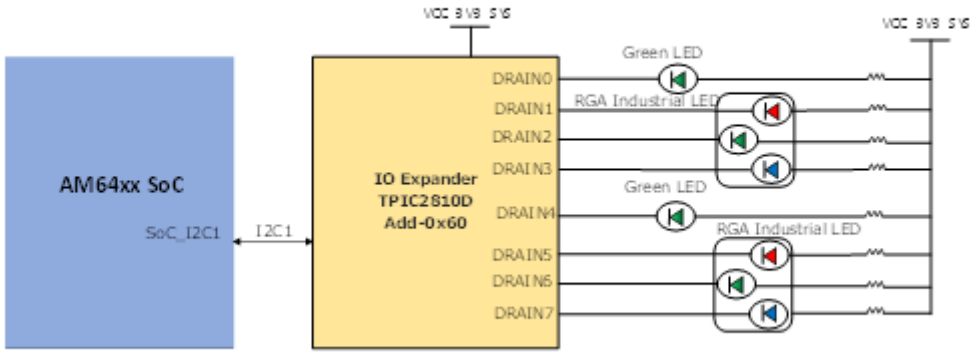


Figure 4-16. Ethernet Interface - LEDs

4.10 USB 3.0 Interface

On the AM64x SKEVM, USB 3.0 HOST interface is offered through USB Type-A Connector (692121030100) which supports a data rate up to 5Gbps. Super-speed differential signals from the Type-A connector are connected to the SERDES-0 block of the SoC through a choke and ESD protection device. USB2.0 Lines of the Type-A connector are directly interfaced to the USB0 port of the AM64x SOC. USB0_DRVVBUS from the SoC enables the 5-V power switch to provide VUSB_TYPEA supply used for the USB Type-A connector.

An ESD protection device meeting the USB 3.0 speed and capacitance specification is included on all USB3.0 Lines (TX_P, RX_P, TX_N, and RX_N) to dissipate ESD strikes. A common mode choke on USB data lines is provided for EMI/EMC. An ESD protection device with part number TPD4S012 is included to dissipate ESD strikes on USB2.0 DP/DM signals.

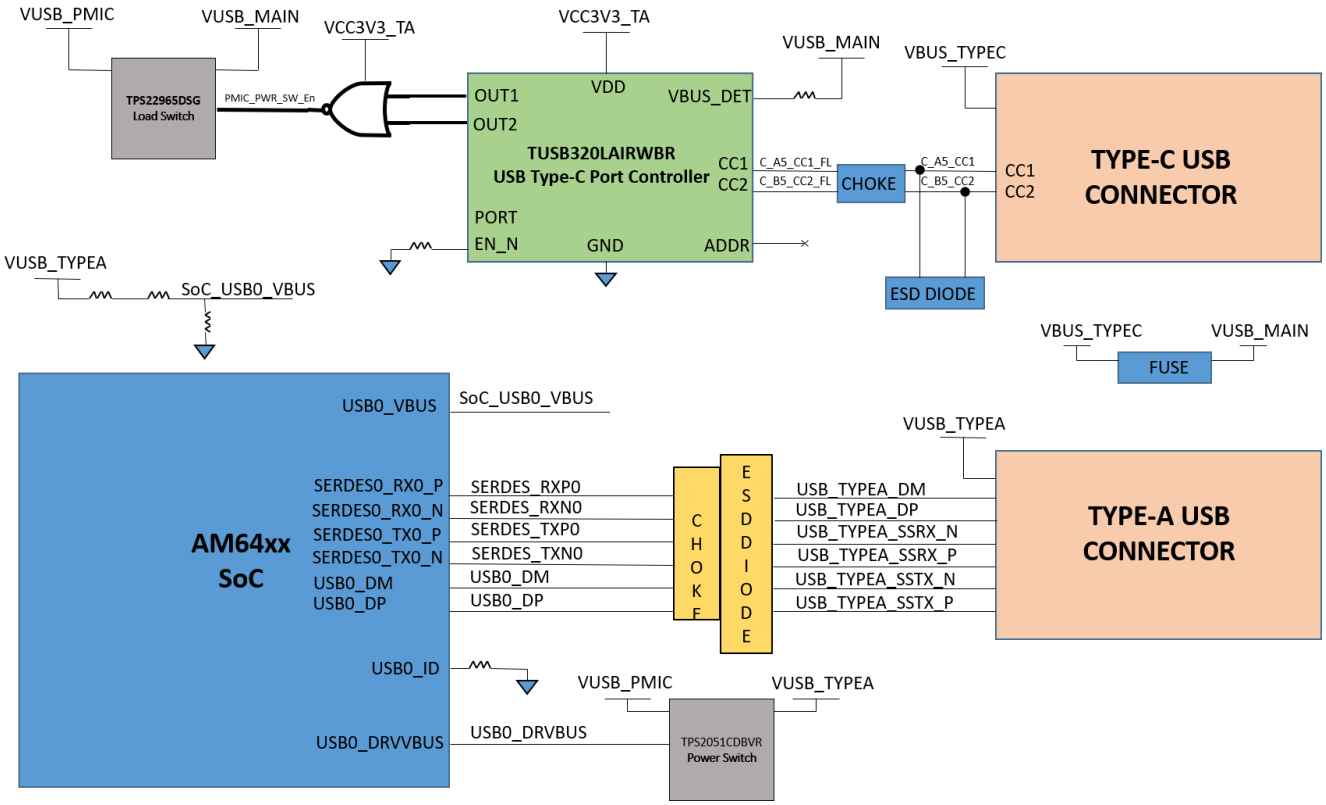


Figure 4-17. USB 3.0 Host Interface

4.11 PRU Connector

PRU header offers low speed connection to the PRG0 interface. PRU_ICSSG signals from a PRG0 port (PRG0_PRU0 and PRG0_PRU1) are terminated on the PRU expansion connector. PRU0 signals are connected to a 27x2 standard 0.1” spaced 54-pin connector. The connector contains MDIO control signals (2 pins), PRG0_PRU0_GPO [0: 19], PRG0_PRU1_GPO [0: 17], +3.3V PWR (2 pins) and Ground reference (5 pins), DETECT, RESET, INT going to the daughter card and SoC I2C0 lines (2 pins). 3.3 V are current limited to 200 mA. This is achieved by using load switch TPS22902YFPR. Enable for the load switch is controlled by the SoC.

Signals routed from the PRU connector are listed in Table 4-20

Table 4-20. Selection of PRG0 Signals on PRU Connector

Pin	Net Name	Pin	Net Name
1	VCC3V3_PRU	2	DGND
3	PRU_DETECT	4	PRU_RESETz
5	PRU_INTn	6	SoC_I2C0_SCL
7	PRG0_PRU0GPO16	8	SoC_I2C0_SDA
9	PRG0_MDIO0_MDC	10	NC

Table 4-20. Selection of PRG0 Signals on PRU Connector (continued)

Pin	Net Name	Pin	Net Name
11	PRG0_MDIO0_MDIO	12	NC
13	PRG0_PRU0GPO0	14	PRG0_PRU0GPO1
15	PRG0_PRU0GPO2	16	PRG0_PRU0GPO3
17	PRG0_PRU0GPO4	18	PRG0_PRU0GPO5
19	PRG0_PRU0GPO6	20	PRG0_PRU0GPO7
21	PRG0_PRU0GPO8	22	PRG0_PRU0GPO9
23	PRG0_PRU0GPO10	24	PRG0_PRU0GPO11
25	PRG0_PRU0GPO12	26	PRG0_PRU0GPO13
27	PRG0_PRU0GPO14	28	PRG0_PRU0GPO15
29	DGND	30	PRG0_PRU0GPO17
31	PRG0_PRU0GPO18	32	PRG0_PRU0GPO19
33	DGND	34	DGND
35	PRG0_PRU1GPO0	36	PRG0_PRU1GPO1
37	PRG0_PRU1GPO2	38	PRG0_PRU1GPO3
39	PRG0_PRU1GPO4	40	PRG0_PRU1GPO5
41	PRG0_PRU1GPO6	42	PRG0_PRU1GPO7
43	PRG0_PRU1GPO8	44	PRG0_PRU1GPO9
45	PRG0_PRU1GPO10	46	PRG0_PRU1GPO11
47	PRG0_PRU1GPO12	48	PRG0_PRU1GPO13
49	PRG0_PRU1GPO14	50	PRG0_PRU1GPO15
51	PRG0_PRU1GPO16	52	PRG0_PRU1GPO17
53	DGND	54	VCC3V3_PRU

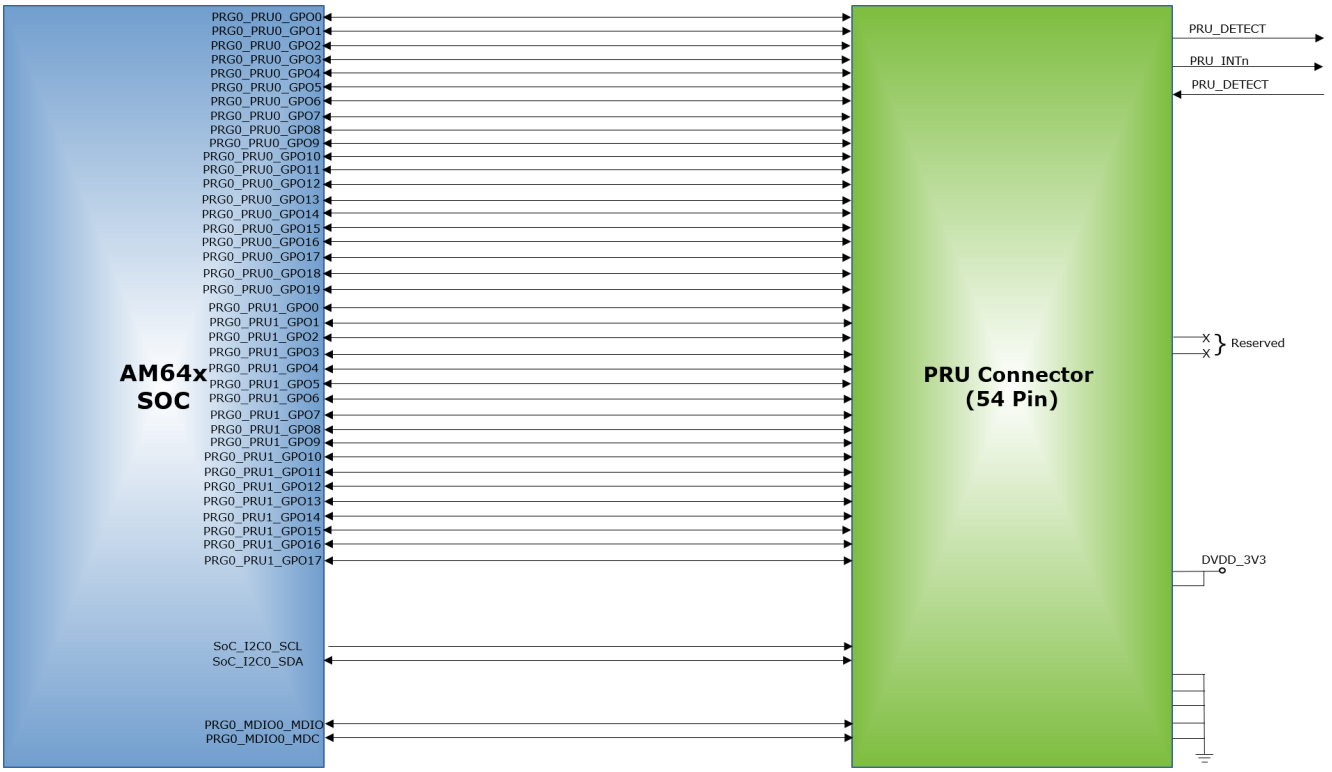


Figure 4-18. 54-Pin PRU Connector

4.12 User Expansion Connector

This connector is compatible with the standard expansion connector found on a Raspberry Pi®™ 4B, allowing seamless interface with HAT boards. Four mounting holes must be oriented with the connector to allow for connection of these boards. Signals connected from SoC to the Expansion Header include: SPI (0), SPI (1), UART (5), I2C (0), I2C (2), EHRPWM4_A / B, EHRPWM5_A / B along with GPIOs [32, 38, 39, 40, 41, 42] along with 5-V and 3.3-V PWR and GND. Each of the power supplies 5 V and 3.3 V are current limited to 155 mA and 500 mA, respectively. This is achieved by using load switch TPS22902YFPR. Enable for the load switch is controlled by the IO expander. Signals routed from User Expansion connector are listed in Table 4-21.

Table 4-21. 40 Pin User Expansion Connector

Pin	Net Name	Pin	Net Name
1	VCC3V3_RPI	2	VCC5V0_RPI
3	RPI_I2C2_SDA	4	VCC5V0_RPI
5	RPI_I2C2_SCL	6	DGND
7	RPI_GPIO0_35	8	SOC_MAIN_UART5_TXD
9	DGND	10	SOC_MAIN_UART5_RXD
11	RPI_SPI1_CS1	12	RPI_SPI1_CS0
13	RPI_GPIO0_42	14	DGND
15	RPI_GPIO0_32	16	RPI_GPIO0_38
17	VCC3V3_RPI	18	RPI_GPIO0_39
19	RPI_SPI0_D0	20	DGND
21	RPI_SPI0_D1	22	RPI_GPIO0_40
23	RPI_SPI0_CLK	24	RPI_SPI0_CS0
25	DGND	26	RPI_SPI0_CS1
27	SoC_I2C0_SDA	28	SoC_I2C0_SCL
29	RPI_ETHRPWM5_A	30	DGND
31	RPI_ETHRPWM5_B	32	RPI_ETHRPWM4_A
33	RPI_ETHRPWM4_B	34	DGND
35	RPI_SPI1_D1	36	RPI_SPI1_CS2
37	RPI_GPIO0_41	38	RPI_SPI1_D0
39	RPI_HAT_DETECT	40	RPI_SPI1_CLK

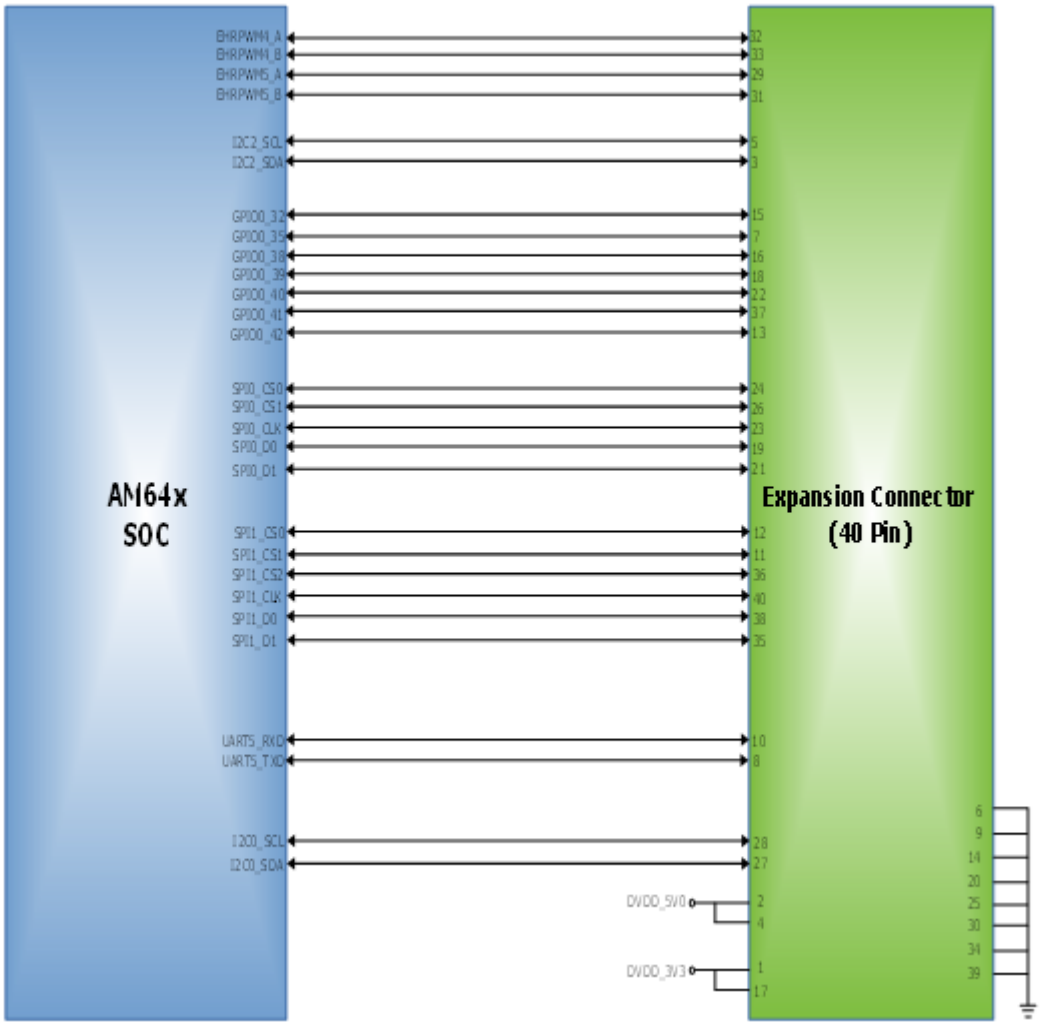


Figure 4-19. 40-Pin User Expansion Connector

4.13 MCU Connector

A safety signal connector is a 14x2 standard 0.1” spaced header. The MCU connector only includes signals connected to the MCU. 18 signals include MCU_I2C0, MCI_I2C1, MCU_UART1 (with flow control), MCU_SPI0, and MCU_SPI1 signals. Additional control signals provided on the connector include CONN_MCU_RESETz, CONN_MCU_PORz, MCU_RESETSTATz, MCU_SAFETY_ERRORn, 3.3V IO to MCU, and GND. The MCU connector does not include the Board ID memory interface. Allowed current limit is 100 mA on 3.3-V rail.

Table 4-22. MCU Connector (28 Pin)

Pin	Net Name	Pin	Net Name
1	VCC_3V3_SYS	2	DGND
3	MCU_SPI0_CS1	4	MCU_SPI0_D1
5	MCU_GPIO0_8	6	MCU_SPI0_D0
7	DGND	8	MCU_SPI0_CS0
9	TEST_LED2	10	MCU_GPIO0_6
11	MCU_GPIO0_7	12	MCU_UART1_CTS_3V3
13	MCU_UART1_RX_3V3	14	MCU_GPIO0_9
15	DGND	16	MCU_I2C1_SDA
17	MCU_UART1_RTS_3V3	18	MCU_SPI0_CLK
19	MCU_UART1_TX_3V3	20	DGND

Table 4-22. MCU Connector (28 Pin) (continued)

Pin	Net Name	Pin	Net Name
21	MCU_I2C0_SDA	22	MCU_I2C1_SCL
23	MCU_RESETSTATz	24	MCU_I2C0_SCL
25	CONN_MCU_RESETz	26	MCU_SAFETY_ERRORz_3V3
27	DGND	28	CONN_MCU_PORz

Figure 4-20. 28-Pin MCU Connector

4.14 Interrupt

The SK EVM supports the following timer and interrupt options.

Three interrupts are available to provide reset for MCU_PORz and MCU_RESETz and RESET_REQz. One push button switch is available for GPIO interrupt which is connected to both main domain and MCU domain GPIO pin.

Warm reset can also be applied through the test automation header.

4.15 I2C Interface

There are three I2C interfaces used in SK EVM board.

- SoC_I2C0 Interface: SoC I2C [0] is connected to Board ID EEPROM, PMIC, PRU Header, and User Expansion Header. I2C0 interface is used by the software to identify the EVM through the Board ID memory device AT24C512C-MAHM-T 512Kb serial EEPROM configured to respond to addresses 0x51. I2C0 interface on the SKEVM is also used by the software to configure and control the PMIC device. I2C0 is also connected to the User expansion Header and PRU Header.
- SOC I2C (1) Interface: SoC I2C [1] is connected to 8-Bit LED driver, 8-Bit GPIO expander, Temperature Sensors, and Test Automation Header.
- SOC I2C (2) Interface: Connected I2C [2] from SoC to the User Expansion Header.

Figure 4-21 depicts the I2C tree.

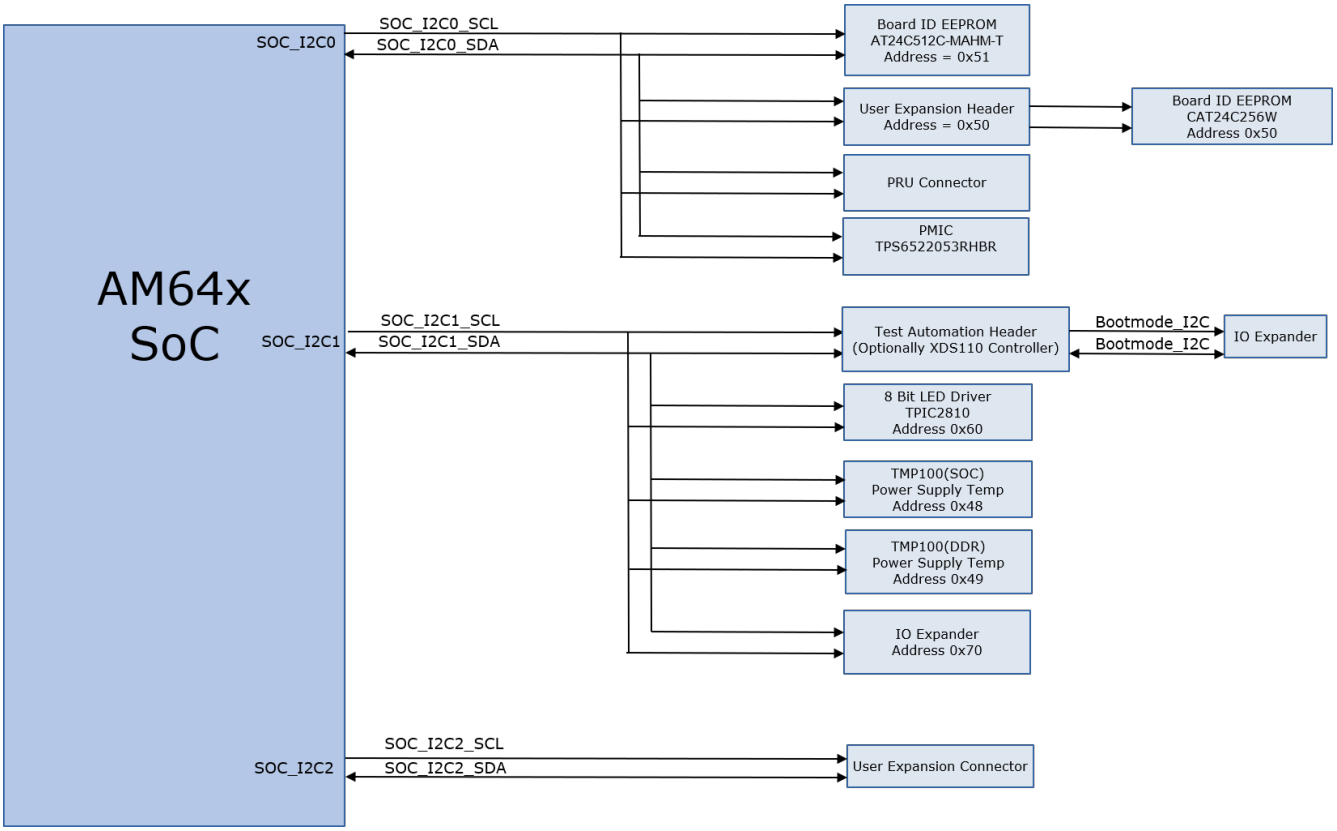


Figure 4-21. I2C Interface

4.16 IO Expander (GPIOs)

The I/O Expander used in the AM64x SoC is a 8-Bit I2C based I/O Expander used for daughter card plug-in detection and also to generate resets and enable signals to various peripheral devices connected to it. The I2C1 bus of the AM64x SoC is used to interface to the I/O Expander, and the address of the I/O Expander is 0X70. Table 4-23 lists the signals controlled by the IO expander.

Table 4-23. IO Expander Pin-outs

Pin no.	Signal	Direction	Device
P0	GPIO_CPSW2_RST	Output	CPSW PHY-2 ETHERNET
P1	GPIO_CPSW1_RST	Output	CPSW PHY-1 ETHERNET
P2	PRU_DETECT	Input	PRU Connector Detection
P3	MMC1_SD_EN	Output	SD Card Power Switch Enable
P4	VPP_LDO_EN	Output	SoC VPP Voltage Generation
P5	RPI_PS_3V3_En	Output	User Expansion Connector: 3V3 supply Power Switch Enable
P6	RPI_PS_5V0_En	Output	User Expansion Connector: 5V0 supply Power Switch Enable
P7	RPI_HAT_DETECT	Input	User Expansion Connector: Hardware Add-On Board Detection

5 Known Issues and Modifications

This section describes the currently known issues on each EVM revision and applicable workarounds. Issues that have been patched will have modification labels attached to the EVM assembly.

Table 5-1. AM64 SK EVM Known Issues and Modifications

Issue Number	Modification Label Number	Issue Title	Issue Description
1	N/A	Silkscreen Missprint on initial batch of boards	Initial SK-AM64B boards have "PROC100-002" stickers covering the revision# text.

5.1 Issue 1 - Silkscreen Missprint on Initial Board Batch

Issue Description:

The initial SK-AM64B boards have "PROC100-002" stickers covering the revision# text as a result of a silkscreen oversight.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2022	*	Initial Release

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