

DM388 Base Board

User's Guide



Literature Number: SPRUI85
August 2016

Preface	7
1 Introduction to DM388 Base EVM	9
1.1 DM388 Processor	10
1.2 Block Diagram	12
1.3 Key Features.....	13
1.4 Functional Overview	13
1.5 Memory and I/O Mapping	14
1.6 GPIO Mapping	15
1.7 I ² C Address Mapping	16
2 Interfaces and Power Section of DM388 Base EVM.....	17
2.1 EVM Interfaces	18
2.1.1 DDR Interface.....	18
2.1.2 NAND Interface.....	18
2.1.3 SD/MMC Interface.....	18
2.1.4 Audio Interface.....	19
2.1.5 EMAC Interface.....	19
2.1.6 EEPROM Interfaces	20
2.1.7 HDMI	21
2.1.8 Video DAC Interface	22
2.1.9 High-Speed USB Interface	22
2.1.10 SPI Flash Interface.....	22
2.1.11 UART Interface	22
2.1.12 I ² C Interface	23
2.1.13 Debug Interface	23
2.1.14 PCI Express Interface	23
2.1.15 MSP430™ Interface	24
2.2 Clock	25
2.3 Power	25
2.3.1 DM388 Power From PMIC	29
2.4 DM388 EVM Muxing Options.....	30
2.4.1 McASP0 Muxing.....	31
2.4.2 McASP1 Muxing.....	32
2.4.3 McASP0_AXR [4:5] Lines Muxing	33
2.4.4 McASP5 and GPIO Selection for VC Board	34
2.4.5 MCA1_AHCLKX Muxing	35
2.5 UART2, I2C2, and VOUT Muxing.....	35
3 Physical Description	37
3.1 DM388 EVM Layout.....	38
3.2 Connectors, Switches, Headers, and Jumpers.....	39
3.2.1 SD/MMC Card Holder	39
3.2.2 JTAG Header	40
3.2.3 Component Video Out	41
3.2.4 VGA Connector.....	42
3.2.5 Composite Video Connector	44
3.2.6 USB-OTG Connector	45

3.2.7	HDMI OUT Connector	47
3.2.8	Ethernet Connector	48
3.2.9	PCI Express Connector	50
3.2.10	UART Connector	52
3.2.11	EEPROM Header	55
3.2.12	MSP JTAG Header	56
3.2.13	Audio Connectors	57
3.2.14	Power Switches	58
3.2.15	Boot Mode Switches	59
3.2.16	Reset Switch SW4	61
3.2.17	Power-On Reset Switch SW7	62
3.2.18	GPIO Switches and LEDs.....	63
3.2.19	Fuses	63
3.3	Test Points	64
3.4	Expansion Connector	66
A	Schematics	73
B	Assembly Drawings	112

List of Figures

1-1.	DM388 Processor	10
1-2.	DM388 EVM Block Diagram	12
2-1.	PCIe Clock AC-Decoupling Capacitors – Host Clocking Enabled	24
2-2.	IP_EVM_12V.....	26
2-3.	TPS_EVM_5V0.....	26
2-4.	BCK2_3V3	27
2-5.	EVM_5V0.....	27
2-6.	EVM_3V3.....	28
2-7.	PMIC Circuitry	30
2-8.	McASP0 Muxing.....	31
2-9.	McASP1 Muxing.....	32
2-10.	McASP0 Muxing.....	33
2-11.	MCA5 and GPIO Selection	34
2-12.	Required Output Selection	35
2-13.	UART2, I2C2, and VOUT Muxing.....	36
3-1.	TMDXEVM388 Base EVM (Top View)	38
3-2.	TMDXEVM388 Base EVM (Bottom View)	39
3-3.	SD/MMC Card Holder	39
3-4.	JTAG Header	40
3-5.	Component Video Connectors.....	41
3-6.	Component Video Cable	42
3-7.	VGA Connector.....	43
3-8.	VGA Male-to-Male Cable.....	44
3-9.	Composite Video Out Connector.....	44
3-10.	Composite Video Cable	45
3-11.	USB-OTG Connectors	46
3-12.	HDMI Connector.....	47
3-13.	HDMI Cable	48
3-14.	Ethernet Connectors	49
3-15.	PCIe Connector.....	50
3-16.	PCIe Cable	52
3-17.	UART Connector	52
3-18.	MSP430 UART Connector	53
3-19.	UART F-F Serial Cable.....	54
3-20.	EEPROM Header	55
3-21.	MSP JTAG Header.....	56
3-22.	Audio Codec Connectors.....	57
3-23.	HP-Out, Mic-in, and Line-in Cables.....	58
3-24.	EVM Switch Arrangement.....	59
3-25.	Boot Mode Switches	60
3-26.	Reset Switches	62
3-27.	GPIO Switch and LEDs.....	63
3-28.	Major Test Points.....	64
A-1.	Version History	74
A-2.	DM385 Block Diagram.....	75
A-3.	Memory Map	76
A-4.	McASP Muxing	77

A-5.	DM385 McASP	78
A-6.	McASP Muxing and Decoders.....	79
A-7.	McASP B-B Connection	80
A-8.	AIC3106	81
A-9.	GMII0 Interface	82
A-10.	Ethernet Controller 0.....	83
A-11.	Ethernet Controller 1.....	84
A-12.	NAND Flash.....	85
A-13.	GPMC B-B Connector	86
A-14.	DM385 MMC0, MMC1, and MMC2	87
A-15.	DM385 DDR0 Terminations.....	88
A-16.	DDR0-0, DDR0-1, DDR0-2, and DDR0-3.....	89
A-17.	DM385 VIN0, VOUT0, and VOUT1.....	90
A-18.	Video B-B Connector	91
A-19.	DM385 Serial Interfaces.....	92
A-20.	SPI Flash	93
A-21.	DM385 HDMI, SATA, USB0, and USB1	94
A-22.	USB Interface	95
A-23.	DM385 PCIe, JTAG, and Video	96
A-24.	PCIe Connector.....	97
A-25.	SerDes Clocks	98
A-26.	DM385 Clocks	99
A-27.	Power Monitor CPU	100
A-28.	Power Monitors	101
A-29.	DM385 Power	102
A-30.	DM385 VSS	103
A-31.	TPS659113-A	104
A-32.	TPS659113-B	105
A-33.	TPS51116.....	106
A-34.	TPS65232.....	107
A-35.	Power Selection.....	108
A-36.	Power In.....	109
A-37.	Changes in Schematics	110
A-38.	DDR3_TP	111
B-1.	Assembly Drawing (Top Side)	113
B-2.	Assembly Drawing (Bottom Side).....	114

List of Tables

0-1.	Document History	7
0-2.	Board History	7
0-3.	Acronyms	8
1-1.	Memory and I/O Map	14
1-2.	GPIO Mapping	15
1-3.	I ² C Address Mapping	16
2-1.	McASP1 Mapping	19
2-2.	Board Information	21
2-3.	I ² C Power-Monitor Addresses	25
2-4.	McASP0 Mapping	31
2-5.	McASP1 Muxing	33
2-6.	McASP0_AXR Muxing	34
2-7.	Channel Selection	35
2-8.	Channel Selection and Output	35
2-9.	I/O Expander GPIOs	36
3-1.	Pinout of SD/MMC Card Holder	40
3-2.	Pinout of JTAG Header	41
3-3.	Pinout of RGB Connector	42
3-4.	Pinout of VGA Connector	43
3-5.	CV OUT	45
3-6.	Pinout of USB-OTG Connector	46
3-7.	Pinout of HDMI OUT	47
3-8.	Pinout of Ethernet Connectors	49
3-9.	Pinout of PCIe Connector	51
3-10.	Pinout of UART Connectors	53
3-11.	Pinout of EEPROM Header	55
3-12.	Pinout of MSP JTAG Header	56
3-13.	Pinout of Audio LINE OUT	57
3-14.	Pinout of Audio LINE IN	57
3-15.	Pinout of Audio MIC IN	58
3-16.	Boot Mode Combinations	60
3-17.	Warm Reset Push-Button	61
3-18.	Cold-Reset Push-Button	62
3-19.	Test Point Signals	65
3-20.	64-Pin Video Expansion Connector (J27)	66
3-21.	128-Pin Video Expansion Connector (J28)	67
3-22.	128-Pin GPMC Expansion Connector (J19)	68
3-23.	128-Pin MCASP Expansion Connector	70
3-24.	64-Pin GPMC Expansion Connector	71

About This Manual

Developed with Mistral Solutions, the DM388 base evaluation module (EVM) enables developers to start immediate evaluation of DM388 processors and begin building on different video applications.

This document describes the board level operations of the DM388 base EVM. The EVM is based on the Texas Instruments DM388 Applications Processor.

National Conventions

The DM388 base EVM will sometimes be referred to as the DM814x EVM or the base EVM.

Information About Cautions

This Document may contain cautions.

This is an Example of a Caution Statement

A caution statement describes a situation that could potentially damage your software, hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes, and User Guides

Information regarding the DM388 processor can be found at <http://www.ti.com>.

Table 0-1. Document History

Version Number	Description of Changes
0.1	Draft version

Table 0-2. Board History

PCB Revision	History
Revision A	Created
Revision B	HDDAC and GMPC sections changed

DaVinci, MSP430, Code Composer Studio are trademarks of Texas Instruments.
NEON is a trademark of ARM Limited.
ARM, Cortex are registered trademarks of ARM Limited.
Mentor is a registered trademark of Mentor Graphics Corporation.
PCI Express is a registered trademark of PCI-SIG.
Skype is a trademark of Skype.
DesignWare is a registered trademark of Synopsys, Inc..

Acronyms

[Table 0-3](#) lists the acronyms used in this document.

Table 0-3. Acronyms

Acronym	Definition
BGA	Ball grid array
CCS	Code Composer Studio
DDR	Double data rate
EEPROM	Electrically erasable programmable read-only memory
ESD	Electrostatic discharge
EVM	Evaluation module
GPIO	General purpose Input/Output
GPMC	General purpose memory controller
I ² C	Inter-integrated circuit
JTAG	Joint test action group
LCD	Liquid crystal display
LED	Light emitting diode
MAC	Media access controller
McBSP	Multichannel buffered serial port
OTG	On-the-go
PCB	Printed circuit board
PHY	Physical transceiver
SD/MMC	Secure digital and multimedia card
SDRC	SDRAM controller
SDRAM	Synchronous dynamic random access memory
SPI	Serial peripheral interface
SPDT	Single pole double throw
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus

Introduction to DM388 Base EVM

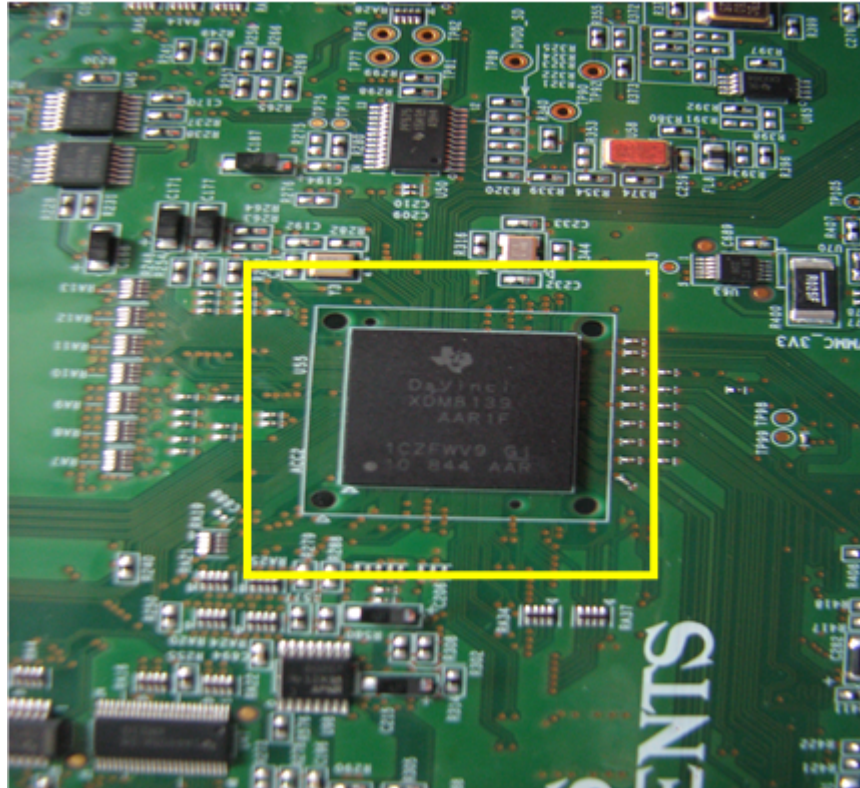
This chapter provides a functional overview of the DM388 processor, key features, and a high-level block diagram of the DM388 base EVM design. This chapter also provides information about memory and I/O mapping, GPIO mapping, and inter-integrated circuit (I²C) mapping of devices on the DM388 base EVM.

Topic	Page
1.1 DM388 Processor	10
1.2 Block Diagram	12
1.3 Key Features	13
1.4 Functional Overview	13
1.5 Memory and I/O Mapping	14
1.6 GPIO Mapping.....	15
1.7 I²C Address Mapping	16

1.1 DM388 Processor

The DM388 processor mainly consists of ARM® Cortex®-A8 RISC CPU with NEON™ technology extension, TI C674x VLIW floating-point DSP core, and high-definition video and imaging coprocessors.

Figure 1-1. DM388 Processor



The DM388 processor is a highly integrated, programmable platform that leverages DaVinci™ technology from TI to meet the processing needs of the following applications:

- IP-netcam
- Digital video server (DVS)
- High-definition webcam
- High-definition embedded video communication modules
- Remote media display (RMD) and interactive digital signage

In addition to these markets, this user's guide also addresses:

- 3G gesture control (HDI)
- Video doorbell
- Telemedicine
- Test and Measurement
- Analytics
- Instrumentation
- Inspection and machine vision
- Avionics
- Skype™ endpoint applications

An ARM Cortex-A8 RISC CPU with a NEON extension, a TI C674x VLIW floating-point DSP core, and high-definition video and imaging coprocessors provide the programmability.

The ARM Cortex-A8 32-bit RISC microprocessor with NEON floating-point extension includes:

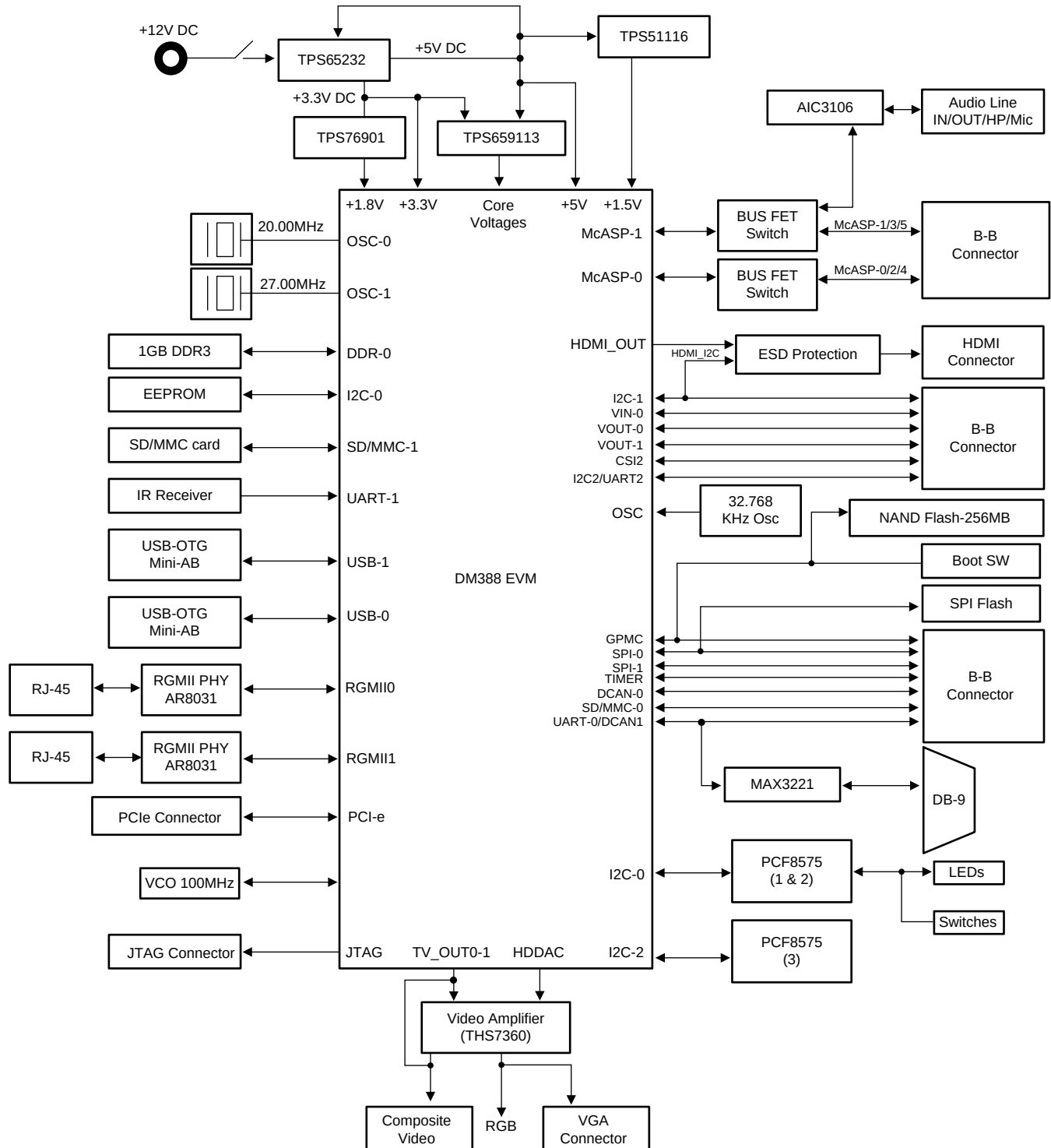
- 32KB of instruction cache
- 32KB of data cache
- 256KB of L2 cache
- 176KB of on-chip boot ROM (128KB of secure ROM and 48 KB of public ROM)
- 64KB of RAM

The DM388 processor is a 609-pin, Pb-Free BGA Package that has a 0.5-mm ball pitch with Via Channel technology to reduce the printed-circuit board (PCB) cost. The core of the ARM Cortex-A8 CPU operates at a speed of up to 1 GHz.

1.2 Block Diagram

Figure 1-2 shows the block diagram of the DM388 processor.

Figure 1-2. DM388 EVM Block Diagram



Copyright © 2016, Texas Instruments Incorporated

1.3 Key Features

The DM388 processor includes the following key features:

- High-performance digital media System-on-Chip (SoC)
- Memory
 - 32-bit DDR3 SDRAM interface (DDR0)
 - 1GB (256MB x4 chip) of memory from Micron is used on the DDR3 interface of the DM388 EVM
 - 256MB of NAND flash memory from Micron with socket for placing the NAND is used on the DM388 base EVM
- Power for the processor is derived from integrated power-management IC TPS659113.
- Analog video-out interface – Composite SD video from the TV OUT interface of the processor is available on the yellow RCA jack of the board.
- Component video out (RGB) from the HD digital-to-analog converter (DAC) interface of the processor is available on the board of the VGA connector.
- Digital video-out interface – Supported by an on-chip high-definition multimedia interface (HDMI) transmitter with a resolution and frame rate of 1080p60.
- USB interface – Dual high- and full-speed USB OTG 2.0 port with integrated PHYs
- Ethernet interface – Two RGMII ports interfaced to the MAC have a speed of 10/100/1000 Mbps.
- Stereo audio interface – Audio Line IN, Mic IN, Speaker OUT and Headset OUT
- Serial Interfaces – SD/MMC connector in 4-bit SD mode Supporting up to 48 MHz
- A 32-MB serial peripheral interface (SPI) flash memory is available on the DM388 EVM for SPI booting.
- Ultra-low-power MSP430™ microcontroller (MCU) to monitor the current flow of the DM388 device with INA226
- Dip switch to select different boot mode configurations
- Standard 20-pin JTAG debug interface
- Video, GPMC, and MCASP expansion board-to-board connectors are available to connect different application boards of the DM814x and AM387x (such as video camera, video conference, video security, and catalog application).
- PCI Express® 2.0 port with integrated PHY and one lane supports up to 5.0 GT/s
- RoHS compliant

1.4 Functional Overview

The DM388 EVM is based on the DM388 application processor from TI. The Micron memory MT41J256M8HX-125 is connected to the DM388 processor through the SSTL_15 interface. The DDR memory on the board consists of four chips (MT41J256M8HX-125) of micron memory that each have a capacity of 2Gb (256MB), and the memory has an excellent on-chip ODT for better signal quality. NAND flash memory is connected to the processor through the GPMC interface. The chip enable pin of the NAND device is connected to GPMC_nCS0 of the DM388 processor.

Analog video outputs of the EVM support composite TV outputs on the main board. The composite video outputs are available on the respective connector by default.

The DM388 base EVM supports multiple video input options from the application board through VIN0, VIN1, and the camera port. Any of the following interfaces can be active at a given point of time when the catalog application board is connected through the expansion board to the board connectors.

- S-video input digitized through video decoder (TVP5147)
- Composite video input digitized through video decoder (TVP5147)
- RGB video input digitized through video decoder (TVP7002)
- VGA input digitized through video decoder (TVP7002)
- Camera input from parallel camera interface

The EVM has a SD/MMC slot connected by using an SD/MMC1 4-bit interface on the main board. The SD/MMC2 interface is routed to the expansion connector for WLAN module on application board. The EVM has two RGMII Ethernet ports (RGMII0, RGMII1) using two external AR8031 Gigabit PHY devices that are interfaced to the processor through the RGMII interface. It has a PCIe2.0 ×4 connector with integrated PHY on the DM814x processor that can be configured as Root complex or Endpoint.

The EVM supports two UART interfaces (DM388 UART, MSP430 UART) through two serial ports (DB9 connector) on the main board. The board has two USB mini-AB connectors to support a high-speed USB OTG2.0 interface. One Stereo Line IN, MIC IN, Speaker OUT, and Stereo Headset OUT audio interface is supported through the audio codec TLV320AIC3106IRGZT on the EVM. The audio codec on the EVM is controlled by the I2C0 and MCASP1 interface.

The EVM has five DIP switches for various purposes such as selecting different boot modes, GPIO toggling, video-out enable, NAND and SPI flash selection, and resetting the GPIO. The EVM also includes three reset push-button switches, one SYS_WAKE push-button switch, and three slide switches for power flow. The EVM has a standard 20-pin JTAG header (10 × 2 1.27-mm pitch) for debug interface. This JTAG port can be accessed through Code Composer Studio™ development version 4.0 and higher. The EVM is powered by a 12-V, 5-A external power supply, and a TPS659113 power-management device provides the required CPU core voltages and I/O voltages for the DM388 processor.

1.5 Memory and I/O Mapping

Table 1-1 provides the memory and I/O mapping for the DM388 EVM.

Table 1-1. Memory and I/O Map

Device	Start Address	End Address	Size	Description
GPMC	0x0000_0000	0x1FFF_FFFF	512MB	GPMC
On-chip ROM	0x4000_0000	0x4001_FFFF	128KB	Secure ROM
	0x4002_0000	0x4002_BFFF	48KB	ROM
On-chip RAM	0x402F_0000	0x402F_FFFF	64KB	Secure RAM
	0x4030_0000	0x4031_FFFF	128KB	OCMC SRAM
PCIe	0x2000_0000	0x2FFF_FFFF	256MB	PCIe
DDR	0x8000_0000	0xFFFF_FFFF	2GB	DDR
I2C0	0x4802_8000	0x4802_8FFF	4KB	I2C0 peripheral registers
I2C1	0x4802_A000	0x4802_AFFF	4KB	I2C1 peripheral registers
I2C2	0x4819_C000	0x4819_CFFF	4KB	I2C2 peripheral registers
SPI0	0x4803_0000	0x4803_0FFF	4KB	SPI0 peripheral registers
SPI1	0x481A_0000	0x481A_0FFF	4KB	SPI1 peripheral registers
MMC	0x481D_8000	0x481E_7FFF	64KB	MMC/SD/SDIO1 peripheral registers

1.6 GPIO Mapping

Table 1-2 lists some of the GPIOs that are used in the DM388 base EVM.

Table 1-2. GPIO Mapping

Number	GPIO Name	Source	Purpose
1	ENET_WoL_INT	GP0[12]	WoL interrupt
2	HDMI_CT_HPD	PCF8575 DEVICE-3	Enabling load switch
3	HDMI_LS_OE	PCF8575 DEVICE-3	Enabling level shifter
4	DISABLE_SD	PCF8575 DEVICE-3	SD and SF channel control of video amplifier
5	DISABLE_SF	PCF8575 DEVICE-3	
6	BYPASS_SD	PCF8575 DEVICE-3	To bypass LPF of SD and SF in VA
7	BYPASS_SF	PCF8575 DEVICE-3	
8	FILTER1	PCF8575 DEVICE-3	Selectable filter for SF channels
9	FILTER1	PCF8575 DEVICE-3	
10	IO_EXP2_GP1	PCF8575 DEVICE-2	GPIO used in CATALOG board
11	IO_EXP2_GP2	PCF8575 DEVICE-2	GPIO used in CATALOG
12	MCA0_DEC_A	PCF8575 DEVICE-2	MCASP0 decoder select
	MCA0_DEC_B		Lines
13	MCA1_MUX_SEL	PCF8575 DEVICE-2	MCASP1 MUX select lines
14	MCA0/1/3_RSEL_A MCA0/1/3_RSEL_B	PCF8575 DEVICE-2	MCASP0/1/3_R decoder select lines
15	PCF8575_INT_IO2	GP0[13]	Interrupt
16	MCA0_AXR9	PCF8575 DEVICE-2	GPIO used in VC board
17	IO_EXP2_GP3	PCF8575 DEVICE-2	GPIO used in VC board
18	MCA5_MUX_OE	PCF8575 DEVICE-2	To select B/T GPIO N MCA5_AHCLKX
19	VOUT_FLD_SEL1	PCF8575 DEVICE-3	To provide the pin muxing option for the VOUT0_FLD and VOUT1_FLD pins
20	VOUT_FLD_SEL2	PCF8575 DEVICE-3	
21	GPIO_VC_1	PCF8575 DEVICE-2	GPIO used on the application board
22	GPIO_VC_2	PCF8575 DEVICE-2	
23	MCA1_MUX2_nOE	PCF8575 DEVICE-2	MCASP1 muxing selection
24	ENET_INT	GP1[10]	Interrupt from EMAC PHY ICs
25	PCF8575_INT_IO1	GP1[4]	Interrupt from PCF8575 (U39)
26	EN_BCK2_LS	TPS659113-GPIO 7	Enabling load switch
27	EN_BCK3_TPS65232	TPS659113-GPIO 2	Enabling PCI_3V3
28	EN_TPS51116	TPS659113-GPIO 0	Enabling DDR supply
29	MSP430_INT	PCF8575 DEVICE- 1	Interrupt from MSP430
30	TPS_INT1	TPS659113-INT 1	Interrupt from PMIC
31	TPS_SLEEP	PCF8575 DEVICE-1	Sleep for TPS659113
32	PCI_SW_RESETh	PCF8575 DEVICE-1	PCIe reset
33	IR_REMOTE_OFF	PCF8575 DEVICE 1	To control IR sensor
34	UART0_OFF	PCF8575 DEVICE-1	UART0 controlling
35	EXP_ETH_RESET	PCF8575 DEVICE-1	Ethernet reset
36	GPMC_ADD_SELh	PCF8575 DEVICE-1	To select either GPMC or HDMI lines
37	SW_VOUT_EN	TDA04H0SK1 device	Video software enable
38	GPMC_nWP	TDA04H0SK1 device	GPMC write-protect
39	RESET_GPIO	TDA04H0SK1 device	Enabling PCI POR buffer

1.7 I²C Address Mapping

[Table 1-3](#) provides the address mapping for the I²C interface on the DM388 base EVM.

Table 1-3. I²C Address Mapping

I ² C Used	Device	Address
I2C0	Audio codec	0x18
I2C0	EEPROM	0x50
I2C0	TPS659113	0x2D
I2C0	I/O Expander-PCF8575	0x20
I2C0	PCF8575-2	0x23
I2C2	PCF8575-3	0x20
I2C1	HDMI	
I2C0 and I2C2	Application board devices	
I2C0	MSP430	0x25

Interfaces and Power Section of DM388 Base EVM

This chapter provides information about the interfaces and power section of the DM388 EVM.

Topic	Page
2.1 EVM Interfaces.....	18
2.2 Clock	25
2.3 Power	25
2.4 DM388 EVM Muxing Options.....	30
2.5 UART2, I2C2, and VOUT Muxing.....	35

2.1 EVM Interfaces

The main interfaces of the DM388 base EVM are:

- DDR
- NAND flash
- SD/MMC
- Audio
- Ethernet
- EEPROM
- HDMI
- Composite video
- Component video
- VGA
- USB
- SPI flash
- UART
- JTAG
- PCI Express

2.1.1 DDR Interface

The DM388 supports single 32-bit mDDR/DDR2/DDR3 SDRAM interface (DDR0). The DDR3 device on the DM388 base EVM is the MT41J256M8HX-125 with configuration of 256MB x 8. Four 8-bit, 256-MB DDR3 devices are interfaced to 32-bit memory mDDR/DDR2/DDR3 SDRAM interface (DDR0). Hence a total of 1GB of DDR3 memory is interfaced DM814x/AM387x.

The DDR3 supply voltage (1.5 V) and termination voltage (0.75 V) for the DDR3 chips is generated by the synchronous buck converter (TPS51116). The reference voltage (0.75 V) is generated by a voltage divider. For the DQ and DQS lines, series termination is 0 Ω ; 22 Ω series termination is provided for DM lines. All of the address and control lines have a resistor (51 Ω) and a 0.1- μ F capacitor parallel termination.

DM0 and DQS0 are the references for write and read to the first DDR chip DDRx_0 (in each DDR interface). DM1 and DQS1 are the references for the second DDR chip (DDRx_1), DM2 and DQS2 are the references for the third DDR chip (DDRx_2), and DM3 and DQS3 are the references for the fourth DDR chip (DDRx_3). The address lines A[0:14], bank address lines BA[0:2], and the control signals are connected to each of the DDR3 chips.

2.1.2 NAND Interface

The MT29F2G16ABAEAWP:E is the NAND flash device used on the DM388 EVM. The memory configuration is 2Gb with a 16-bit databus. The NAND flash is interfaced to the GPMC port of the DM388. NAND flash has 16 multiplexed I/O lines for data and address. The address lines are selected by enabling the GPMC_ADV_N_ALE (address latch enable) to high. The chip select of NAND flash is connected to GPMC_nCS0 of the GPMC controller. A DIP switch (SW5) is provided on the DM388 base EVM to select between onboard NAND booting or NOR booting on an application board (video security). For onboard NAND booting, SW5.1 should be on. NAND IC is placed inside the 48-pin socket on the EVM.

The NAND and SPI interface selection table is silkscreened on the board for user convenience.

2.1.3 SD/MMC Interface

The SD/MMC card connector (MHC-W21-601-LF) interfaces to the SD1/MMC1 port of the DM388. The load switch (MIC94062YC6) controls the power supply to the MMC card (VMMC). VMMC is derived from the EVM_3V3 supply. The enable pin of the load switch (U70) is connected to GP1[2]. The load switch is enabled by default (resistor R266 connecting the GP1[2] pin to the EN pin of the load switch is not mounted in the default configuration).

The card detect pin of the SD/MMC connector is connected directly to the SD1_SD_CD (ball G28) of the DM388. The write-protect pin of the SD/MMC connector is not connected directly to the E29 pin of the DM388; a resistor option is available if the write-protect feature is required. Write-protect is multiplexed (muxed) with {UART0_DSRn/SPI[0]_SCS[2]n/I2C[2]_SDA/SD1_SDWP/GP1[3]}. By default, the SD/MMC card is not write-protected (resistor R265 connects the pin to E29 as described in this paragraph). The E29 pin is used for I2C2 data on the application boards as well as on the base board.

2.1.4 Audio Interface

The audio codec used in the DM388 base EVM is a TLV320AIC3106 device. The device is a low-power stereo audio codec with a stereo headphone amplifier with single-ended or fully-differential configurations. The stereo audio DAC supports sampling rates from 8 kHz to 96 kHz and includes programmable digital filtering in the DAC path for 3D, bass, treble, midrange effects, speaker equalization, and de-emphasis for 32-kHz, 44.1-kHz, and 48-kHz rates.

The stereo audio analog-to-digital converter (ADC) supports sampling rates from 8 kHz to 96 kHz and is preceded by programmable gain amplifiers or AGC that can provide up to 59.5-dB analog gain for low-level microphone inputs. A highly programmable PLL is included for flexible clock generation and support for all standard audio rates from a wide range of available MCLKs, varying from 512 kHz to 50 MHz. The audio codec operates at an analog supply of 3.3 V, a digital core supply of 1.8 V, and a digital I/O supply of 3.3 V. A 24.576-MHz clock is used as a master clock for the audio codec in the EVM.

The TLV320AIC3106 is controlled by I2C0 and McASP1 interfaces. McASP1 selection involves muxing logic because only two McASP instances are available on the DM388 device. Mux logic supports all of the legacy expansion boards of DM814x, which has six instances of McASP.

McASP1 is mapped to the onboard codec, McASP1, McASP3, and McASP5. McASP1 signals MCA1_ACLKX, MCA1_AFSX, MCA1_AXR[0], and MCA1_AXR[1] are mapped to other interfaces using two ICs of Quad x [2:1] MUX SN74CB3Q3257PWR (U36 and U49). Two GPIOs from I/O expander PCF8575PWR (U50) are used to select the required interfaces (onboard codec, McASP1, McASP3, and McASP5) from McASP1 lines using MUX logic.

GPIO MCA1_MUX2_nOE from I/O expander U50 is used to enable any multiplexer IC. GPIO MCA1_MUX_SEL is used to select a particular channel (or particular interface) from the MUX that is enabled.

Table 2-1 lists the McASP1 mapping.

Table 2-1. McASP1 Mapping

MCA1_MUX2_nOE	MCA1_MUX_SEL	MUX Selected	McASP1 is mapped to
0	0	MUX2 (CH 1)	McASP5
0	1	MUX2 (CH 2)	McASP3
1	0	MUX1 (CH 1)	McASP1 on expansion connector
1	1	MUX1 (CH 2)	Onboard codec

The default state of GPIOs from the I/O expander is high (logic 1). By default, McASP1 is mapped to the onboard codec.

NOTE: Interfaces that use McASP1, McASP3, and McASP5 cannot be tested simultaneously. Whenever McASP1 must be routed to expansion connectors to test the interfaces on the application boards, the onboard codec will be automatically disabled.

2.1.5 EMAC Interface

The EMAC software controls the flow of packet data between the device and two external Ethernet PHYs, with hardware flow control and quality-of-service (QOS) support. The EMAC software contains a 3-port gigabit switch, where one port is internally connected and the other two ports are brought out externally. Each external EMAC port supports 10Base-T (10 Mbps) and 100BaseTX (100 Mbps) in half- or full-duplex mode, or 1000BaseT (1000 Mbps) in full-duplex mode.

The EVM has two RGMII Ethernet ports (RGMII0, RGMII1) that use two external PHY AR8031 devices that are interfaced to the processor through the RGMII interface. A single MDIO interface (MDIO clock and MDIO data) is connected out to control the PHY configuration and status monitoring of RGMII0 and RGMII1. Multiple external PHYs can be controlled by the MDIO interface. The EMAC software I/Os operate at 3.3 V and are compatible with 2.5-V I/O signaling. Therefore, Ethernet PHYs with a 2.5-V I/O interface can be used.

The AR8031 requires a single, 3.3-V power supply with an I/O level of 2.5 V. On-chip regulators provide all other required voltages. The AR8031 embeds cable diagnostics test (CDT) technology on chip; this allows measuring the cable length, detecting the cable status, and identifying remote and local PHY malfunctions, bad or marginal patch cord segments, or connectors. Some of the problems that can be detected include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and a bad transformer. The AR8031 also supports Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up. The AR8031 integrates the termination R/C circuitry and the serial resistors for the line side and no external parallel termination required between PHY and magnetics on the board.

The EVM uses two external 25-MHz crystals (Y2 and Y7) to generate local clock for RGMII0 and RGMII1. The PHY uses three clock signals (RX_CLK, MDIO_CLK, and GTX_CLK) and four transmit and receive data lines. Signal RX_CLK comes from PHY to MAC, and signal GTX_CLK comes from MAC to PHY.

2.1.6 EEPROM Interfaces

The EVM uses a 256-Kb I²C CMOS Serial EEPROM CAT24C256WI-GT3 to store the board ID information. EEPROM is interfaced to the DM388 processor by using I2C0. The CAT24C256 device is a 256-Kb Serial CMOS EEPROM, internally organized as 512 pages of 64 bytes each. The device features a 64-byte page write buffer and supports the standard (100 kHz) and fast (400 kHz) I²C protocol.

The write-protect pin (WP) of EEPROM has been pulled low internally by default. If the EEPROM memory must be write-protected, pins 7 and 8 of J19 must be shorted by using a jumper.

Table 2-2 lists the board ID information that is stored. This information is read-only data and should be used to get complete details of the board.

Table 2-2. Board Information

Field Name	Size (in Bytes)	Field Contents
Header	4	0xAA 0x55 0x33 0xEE
Board name	8	813X_EVM
Version	4	B001 (Alphabet) = Beta.001 PCB Version B – Rev B Board 001 : Batch No
BOM version	2	XX (Number)
ECN version	2	XX (Number)
Test package version	2	XX (Number)
Batch code	4	WW YY (2 digits for week and 2 digits for year)
Board serial number	4	XXXX (4-digit number)
Configuration option	18	None
Processor mount option	1	0x01: Socketed 0x02: Soldered
Reserved	32719	None

2.1.7 HDMI

The DM388 processor includes an HDMI transmitter for digital video and audio data to display devices. The HDMI interface consists of a digital HDMI transmitter (HDMI 1.3a-compliant transmitter) core with a TMDS encoder, a core wrapper with interface logic and control registers, and a transmit PHY. An HDMI connector is connected to the processor through ESD protection device (TPD12S016PWR [U4]). The HDMI is controlled by the I2C1 interface of the DM388. The HDMI has three differential pairs of data lines and one differential pair of clock lines.

The HDMI has the following features:

- Hot-plug detection
- Supports up to a 165-MHz pixel clock
 - 1920 × 1080p at 75 Hz with 8-bit per component color depth
 - 1600 × 1200 at 60 Hz with 8-bit per component color depth
- Support for deep-color mode:
 - 10-bit per component color depth up to 1080p at 60 Hz (maximum pixel clock = 148.5 MHz)
 - 12-bit per component color depth up to 720p and 1080i at 60 Hz (maximum pixel clock = 123.75 MHz)
- The TMDS clock to the HDMI-PHY is up to 185.625 MHz.

NOTE: The GPMC_A22 signal is internally muxed with CE_REMOTE_IN on pin N2, and the GPMC_A23 signal is muxed with HDMI_HP_IN on R8 of the DM814x processor. GPMC lines or HDMI lines are selected through switch IC U98 (SN74CB3Q3257PWR) using a GPIO signal (GPMC_ADD_SELn) from U39 (PCF8575PWR). By default, HDMI lines are selected and used in the board.

2.1.8 Video DAC Interface

The DM388 processor supports one SD DAC module (AVDAC1BGTVV4) from the OMAP4430 and a GS70 3-channel HD DAC. The SD DAC module supports composite video standard with sampling rates up to 60 MSPS. The composite video signal (TV_OUT0) is connected directly from the processor to RCA jack J8. An option is available to pass the TV_OUT0 signal through video amplifier THS7360IPW (U5).

The HD DAC consists of three channels of 10-bit current-steering DACs. The output of the DAC can drive the composite video signal to 37.5- Ω load directly. The HD DAC also contains an internal band gap to provide a low-noise reference voltage to the video DAC. The HD DAC supports sampling rates up to 150 MSPS.

HD DAC signals HDDAC_A, HDDAC_B, and HDDAC_C from the processor are connected to component video connectors J7 (Green), J9 (Blue), and J6 (Red) through video amplifier THS7360IPW (U5). HD DAC signals from U5 are also routed to VGA connector P1. The VGA control signals and the sync signals are routed to P1 through an ESD protection device TPD7S019-15DBQR (U7). The control signals required for U5 are taken from I/O expander PCF8575PWR (U14) by using I2C2 lines.

2.1.9 High-Speed USB Interface

The USB controller provides a low-cost connectivity solution for numerous consumer portable devices by providing a mechanism for data transfer between USB devices with a line and bus speed of up to 480 Mbps. The USB subsystem of the DM388 device has two independent USB 2.0 modules (USB0 and USB1) built around two OTG controllers; the OTG supplement feature (support for a dynamic role change) is also supported. Each port can support a dual-role feature allowing for additional versatility that enables operation capability as a host or a peripheral. Both ports have identical capabilities and operate independently.

Each USB controller is built around the Mentor® USB OTG controller and the TI GS70 PHY. Each USB controller has a user-configurable 32KB of endpoint FIFO, and has the support for 15 transmit endpoints and 15 receive endpoints in addition to endpoint 0. The USB uses the CPPI 4.1 DMA to accelerate data movement through dedicated DMA hardware. The two USB modules share the CPPI DMA controller and accompanying queue manager, interrupt pacer, power-management module, and PHY and UTMI clock. The PHY does not have a built-in charge pump and requires an external power source to source the 5-V VBUS power. The PHY has a built-in charge detection for device mode and a control capability for host applications for implementing an external charge detection capability.

For an OTG controller, the procedure of the controller to assume the role of a host or a device is governed by the state of the ID pin. Also, the procedure is controlled by the USB cable connector type. The DM388 device bonds out these ID pins and allows the control to be handled directly from the connector (for example, the USB controller assumes the role based on the cable end inserted into the mini A/B connector [J3 and J4] on the EVM). A jumper option is available on the EVM to ground the USB_ID pin for USB0 (J12) and USB1 (J13). This jumper option enables the EVM to be used in Host Only mode.

2.1.10 SPI Flash Interface

The SPI flash interface is a high-speed synchronous serial I/O port that allows a serial bit stream (4 to 32 bits) to be shifted in and out of the device at the programmed bit-transfer rate. The DM388 processor supports four SPIs. The SPI0 signal from DM388 controls SPI flash memory device. A 32-Mb SPI flash memory (W25X32VSFIG) on the EVM provides SPI booting. For SPI booting, SW5.2 must be on and SW5.1 must be off.

2.1.11 UART Interface

The UART performs serial-to-parallel conversions on data received from a peripheral device, and performs parallel-to-serial conversions on data received from the CPU. There are three UART interfaces (UART0, UART1, and UART2) available for the DM388. One UART interface is available for the MSP430 on the EVM. UART0 on the base EVM is selected by enabling the UART0_OFF signal to low. UART0 is also routed to application boards through board-to-board connectors on the EVM. The UART interface (UART0) can be used on the base EVM or the application boards. UART0 supports a baud rate of up to 3.6 Mbps. UART1 is connected to the IR receiver on the EVM. The IR receiver is selected by enabling the IR_REMOTE_OFF signal to LOW.

2.1.12 I²C Interface

The device includes three I2C modules that provide an interface to other devices that are compliant with version 2.1 of the Philips Semiconductors Inter-IC bus (I2C-bus) specification. External components attached to this 2-wire serial bus can transmit and receive 8-bit data to and from the device through the I2C module.

The I²C port supports the following features in the DM388:

- Standard and fast modes from 10 to 400 kbps
- Noise filter to remove noise 50 ns or less
- Seven- and 10-bit device addressing modes
- Multimaster transmitter and slave receiver mode
- Multimaster receiver and slave transmitter mode
- Combined master transmit and receive and receive and transmit modes
- Two DMA channels, one interrupt line
- Built-in FIFO (32 byte) for buffered read or write

I2C0 of DM388 is being shared across devices like the audio codec, I/O expanders, MSP430 MCU, TPS659113, and EEPROM. I2C2 is shared across the I/O expander and VGA connector. Also, I2C0 and I2C2 are routed to the board-to-board expansion connector to support the interfaces on the application board. The HDMI interface uses I2C1 signals.

2.1.13 Debug Interface

The EVM supports two JTAG debug interfaces: DM388-JTAG and MSP430-JTAG. Debug connectors are used to test, debug, execute, trace, and download the program to the target unit. The following two JTAG connectors are on the board:

- 14-pin MSP430-JTAG header
- 20-pin DM388-JTAG Header

2.1.14 PCI Express Interface

PCIe is a serial-based technology that uses low-voltage differential signaling (LVDS) to reduce the number of data-signal lines and high-frequency clock signals in a point-to-point interconnect arrangement between two devices. PCIe also eliminates multiple host presences on the same bus.

The PCIe subsystem contains the DesignWare® core (DWC), PCIe dual-mode (DM) core, and SerDes PHY. The DM core operates in endpoint (EP) mode or root-complex (RC) port mode. The core supports a single in-port and a single out-port. The operating mode of the PCIe core is set to EP or RC based on: the value sampled from the BOOTMODE[4:0] pins, use as a secondary boot loader, or application software by configuring the PCIE_CFG [PCIE_DEVTTYPE] register. The DM core can be switched between modes at run time by applying a power-on reset.

PCIe supports high-speed data transfer at rates of up to 5.0 Gbps per lane per direction. PCIe on the EVM uses PCI_3V3 and IP_EVM_12V as the supply voltages. The clock required for clocking data and PHY functional clocks are generated by the PHY through the supplied external input 100-MHz differential clock from the device (U56 [CDCM61002RHBR]) on the EVM.

Use the following instructions to enable the PCIe to be compatible with the spread spectrum clock of a PC.

1. Remove the PCIe clock AC-decoupling capacitors on C218, C219, C228, and C229 (see [Figure 2-1](#)).
2. Place a 0805 size 270-pF or 0.1- μ F capacitor across the pads of C218 and C228 for negative reference clock and across the pads of C219 and C229 for positive reference clock that are in proximity.
3. Configure the DM388 board as EP and configure the computer as RC.

Figure 2-1. PCIe Clock AC-Decoupling Capacitors – Host Clocking Enabled

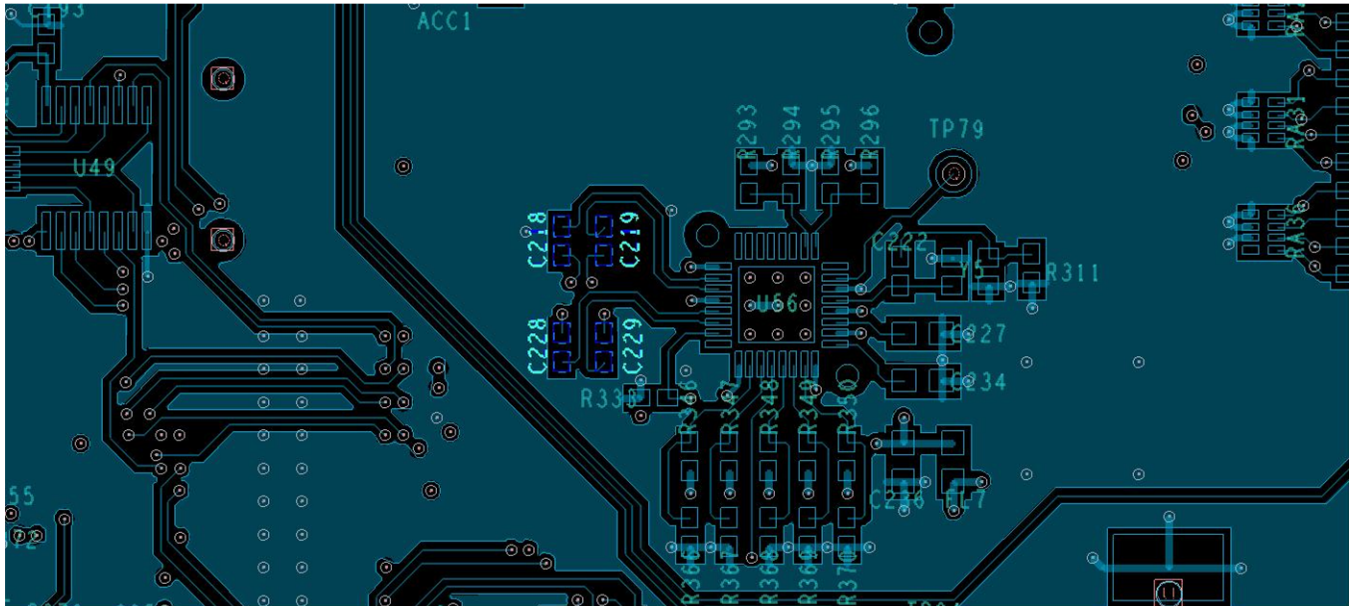


Table 2-3 shows the I²C addresses if the power monitors.

Table 2-3. I²C Power-Monitor Addresses

Supply Number	Supply Name	Address
1	PLL_1V8	1000000
2	HDMI_CSI_1V8	1000001
3	CVDD_ARM	1000010
4	VDDQ_DM_1V5	1000011
5	DVDD	1000100
6	VDDA_1V8	1000101
7	DVDD_GPMC	1000110
8	DVDD_C	1000111
9	CORE_VDD	1001000
10	CVDD_DSP	1001001
11	VMMC	1001010

2.2 Clock

The EVM has the following clocks:

- Y1 – Provides 32.768-kHz real-time clock (RTC) to the power-management IC (TPS659113).
- Y2 – Provides 25-MHz clock for Ethernet PHY (RGMII0).
- Y3 – Provides 20-MHz device (DEV) clock that generates the majority of the internal reference clocks for the DM388.
- Y4 – Provides 32.768-kHz auxiliary clock to the MSP430 MCU.
- Y5 – Provides 25-MHz clock to generate differential clock for the PCI and SerDes CLK.
- Y6 – Provides 27-MHz auxiliary (AUX) clock that can be used as a source for the audio, video PLLs, or both.
- Y7 – Provides 25-MHz clock for Ethernet PHY (RGMII1).
- U58 – Provides 32768-Hz clock input that is provided at the CLKIN32 pin to serve as a reference clock in place of the RTCDIVIDER clock for the following modules:
 - RTC
 - GPIO0, GPIO1, GPIO2, and GPIO3
 - TIMER1, TIMER2, TIMER3, TIMER4, TIMER5, TIMER6, and TIMER7
 - SYNCTIMER

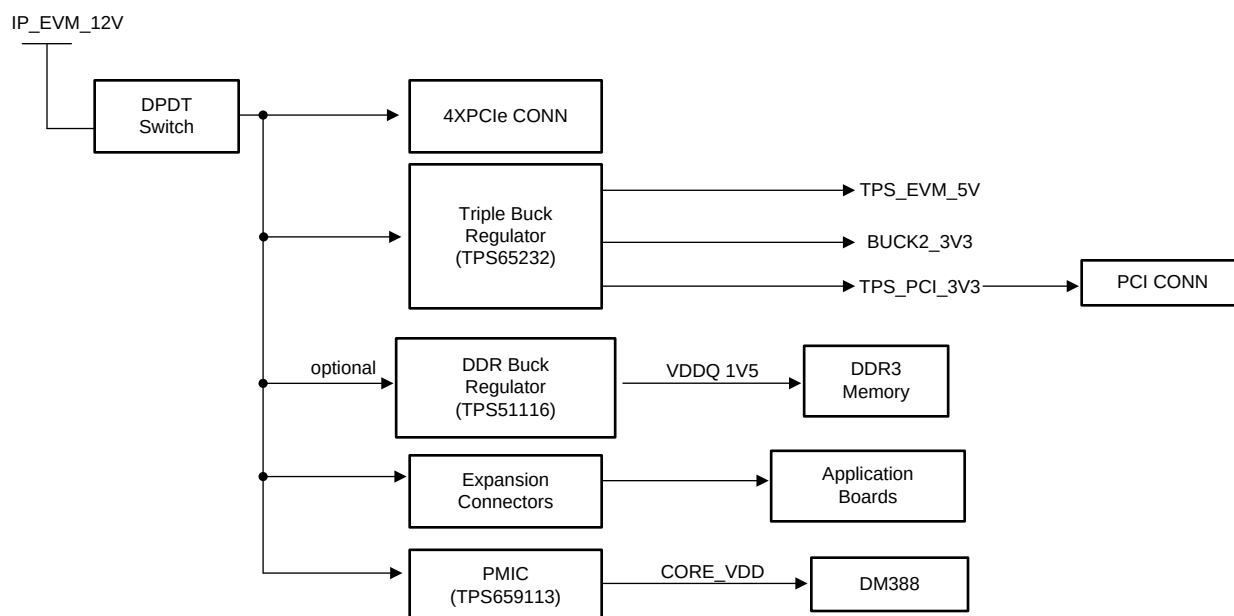
2.3 Power

The main power input for the EVM system is provided by using an external 12-V universal adapter. The other voltages required for the main board are derived by using onboard regulators on the main board. Four major switching regulators are used to derive power for the DM388 EVM.

- TPS65232 (U16) – Gives TPS_EVM_5V0, BCK2_3V3, PCI_3V3
- TPS659113 (U25) – Gives power to DM388
- TPS51116 (U46) – DDR power supply

Figure 2-2 shows the 12-V supply circuitry.

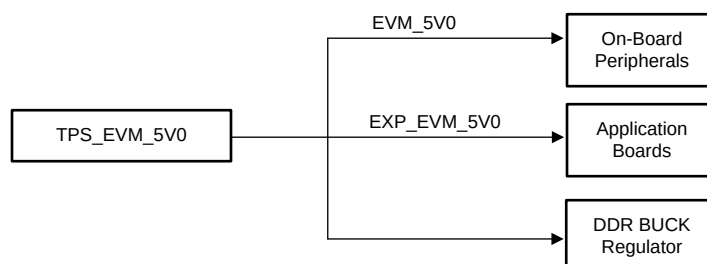
Figure 2-2. IP_EVM_12V



Copyright © 2016, Texas Instruments Incorporated

Figure 2-3- shows the TPS_EVM_5V0 supply circuitry.

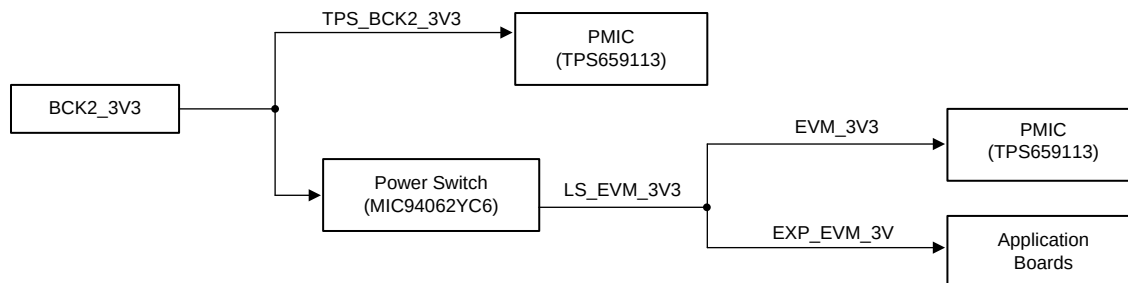
Figure 2-3. TPS_EVM_5V0



Copyright © 2016, Texas Instruments Incorporated

Figure 2-4 shows the BCK2_3V3 supply circuitry.

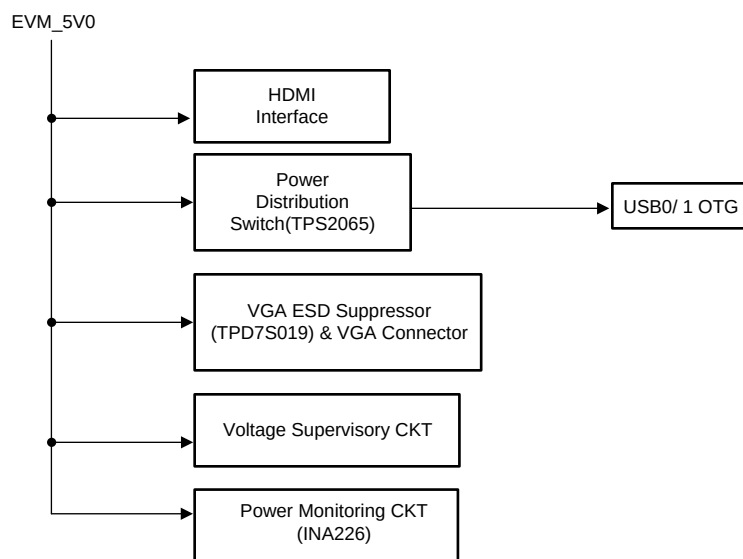
Figure 2-4. BCK2_3V3



Copyright © 2016, Texas Instruments Incorporated

Figure 2-5 shows the EVM_5V0 supply circuitry.

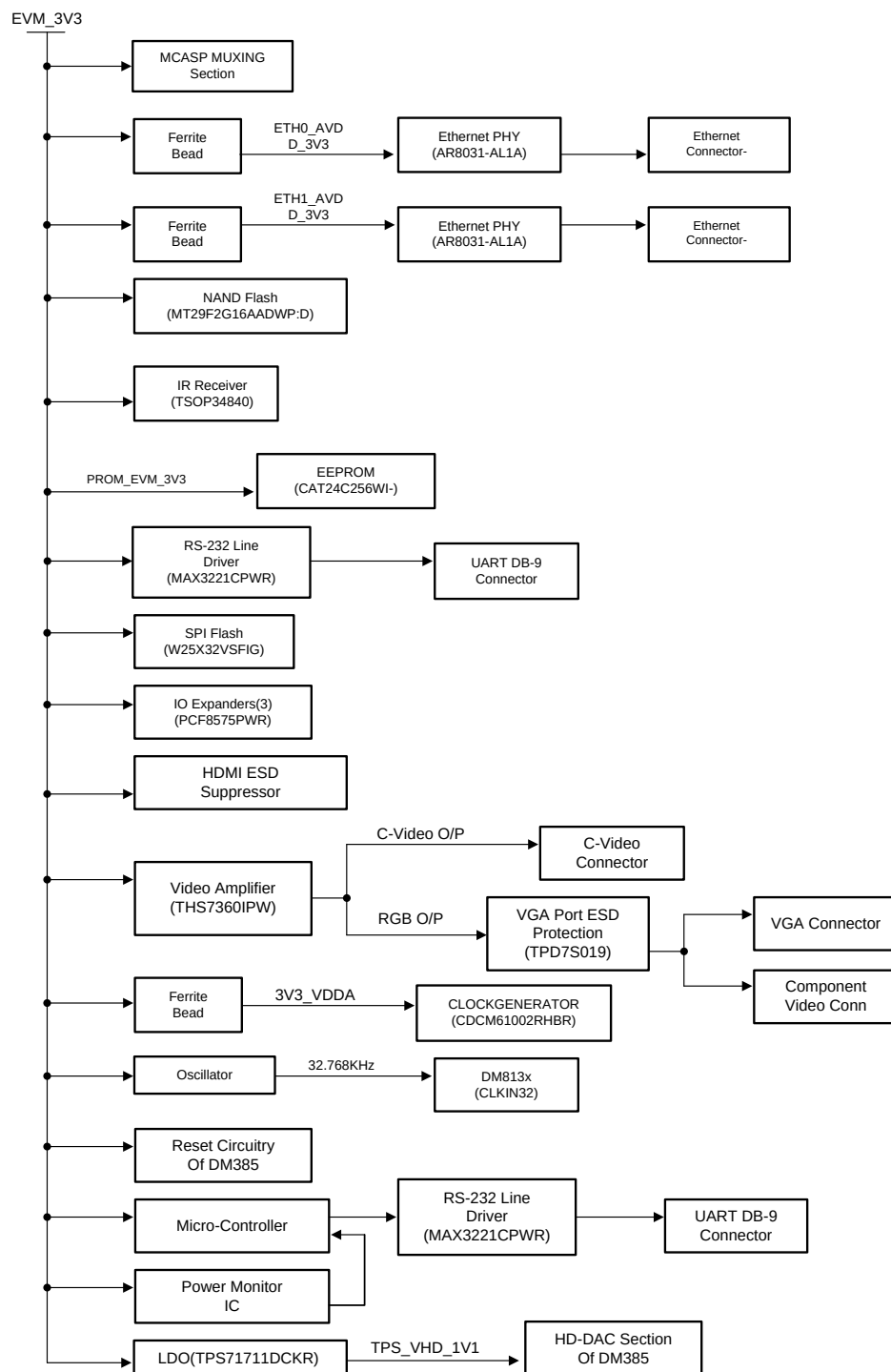
Figure 2-5. EVM_5V0



Copyright © 2016, Texas Instruments Incorporated

Figure 2-6 shows the EVM_3V3 supply circuitry.

Figure 2-6. EVM_3V3



Copyright © 2016, Texas Instruments Incorporated

2.3.1 DM388 Power From PMIC

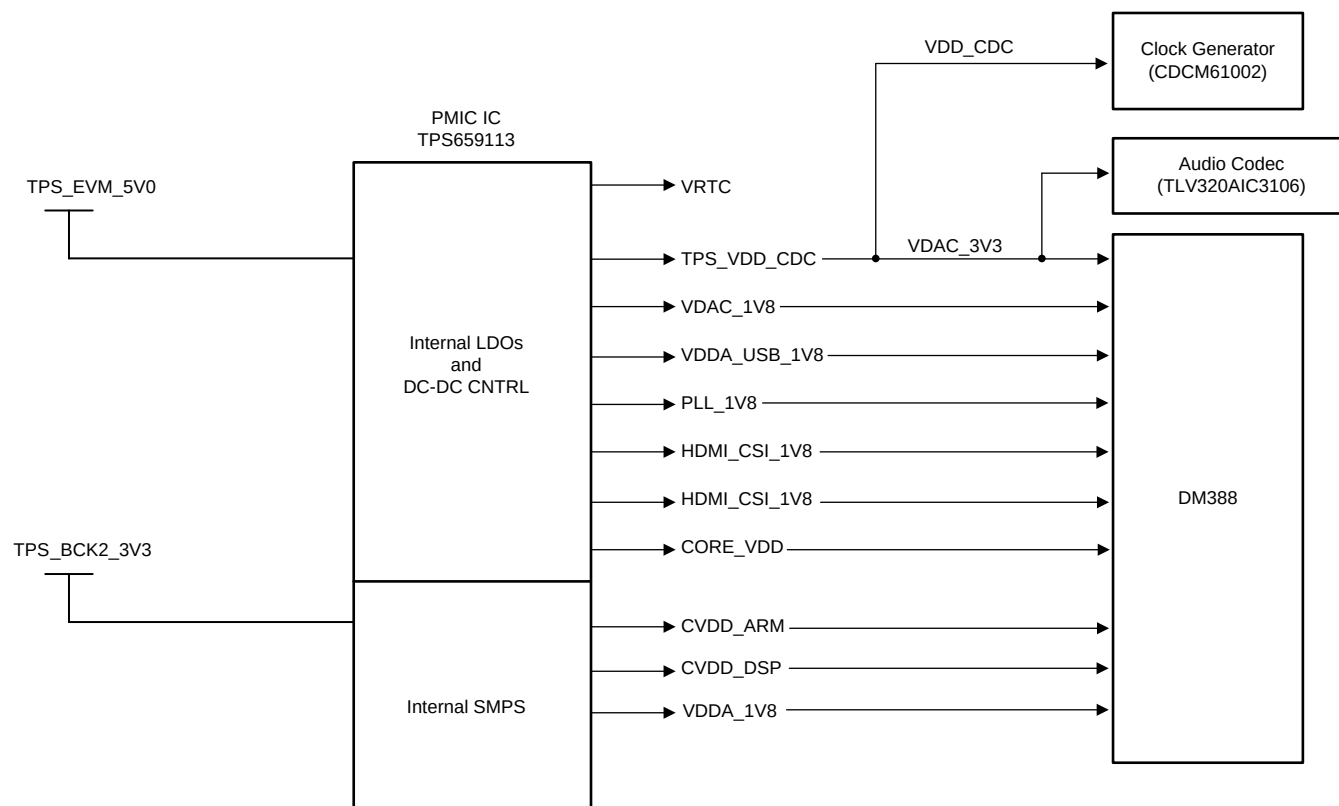
The following list provides the power requirements of the DM388 processor that the power-management IC (TPS659113 [U25]) generates and distributes.

- DM388 I/O supply: TPS_VDDA_1V8-1.8V
- DM388 core supply
 - VDD1(CVDD_ARM)-1.2V
 - VDD2 (CVDD_DSP)-1.2V
 - CORE_VDD-1.2V
- DM388 auxiliary supplies
 - DVDD_GPMC-3.3V
 - DVDD-3.3V
 - DVDD_C-3.3V
 - DVDD_SD-3.3V
 - VDDA_1V8-1.8V
 - HDMI_CSI_1V8-1.8V
 - VDDA_USB_1V8-1.8V
 - VDDQ_1V5-1.5V
- DM388 VDAC supply
 - VDAC_3V3-3.3V
 - VDAC_1V8-1.8V
- PLL supply PLL_1V8-1.8V

The input supply to the power manager is from the TPS_EVM_5V0 and TPS_BCK2_3V3 to generate different voltage rails. The TPS659113 is controlled by the I2C0 interface of the DM388 processor and the address is 0X2D.

Figure 2-7 shows the PMIC circuitry.

Figure 2-7. PMIC Circuitry



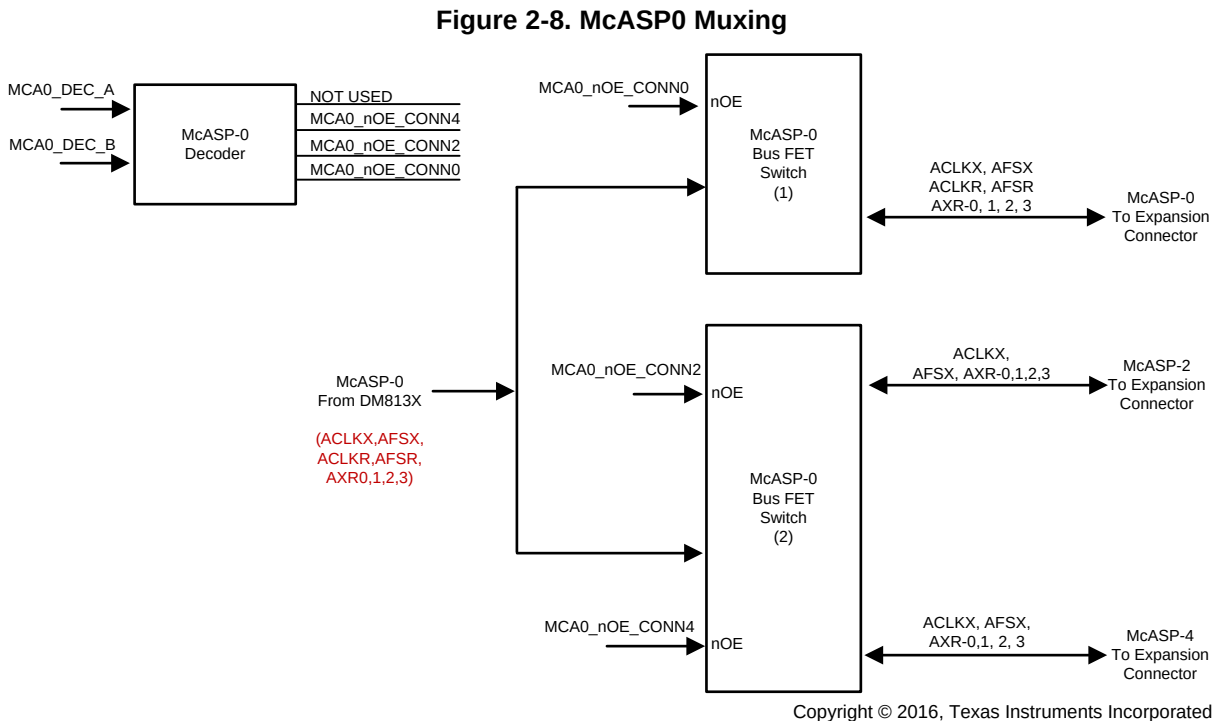
Copyright © 2016, Texas Instruments Incorporated

2.4 DM388 EVM Muxing Options

On the DM388 base Board EVM, McASP muxing has been implemented because of the shortage of McASP interfaces compared to Centaurus. In Centaurus, six McASP (McASP[0:5]) interfaces are available, and in the DM388 only two McASP (McASP[0:1]) interfaces are available. Because the DM388 EVM supports four other application boards that use the McASP[0:5], the muxing option is given for the available McASPs on the DM388 EVM.

2.4.1 McASP0 Muxing

Figure 2-8 shows the muxing of McASP0.



The McASP0 signals MCA0_ACLKX, MCA0_AFSX, and MCA0_AXR[0:3] are mapped using MUXs, and MCA0_AFSR and MCA0_CLKR are directly connected to expansion connector.

To map McASP0 exclusively to one of the McASPs (McASP0, McASP2, McASP4), a decoder has been used with the controlling inputs taken from the I/O expander GPIOs (MCA0_DEC_A and MCA0_DEC_B). By configuring these two GPIOs, McASP0 mapping is achieved (see Table 2-4).

The default state of GPIOs from the I/O expander is high (logic 1). By default, McASP0 is mapped to McASP0.

Table 2-4 shows the McASP0 mapping.

Table 2-4. McASP0 Mapping

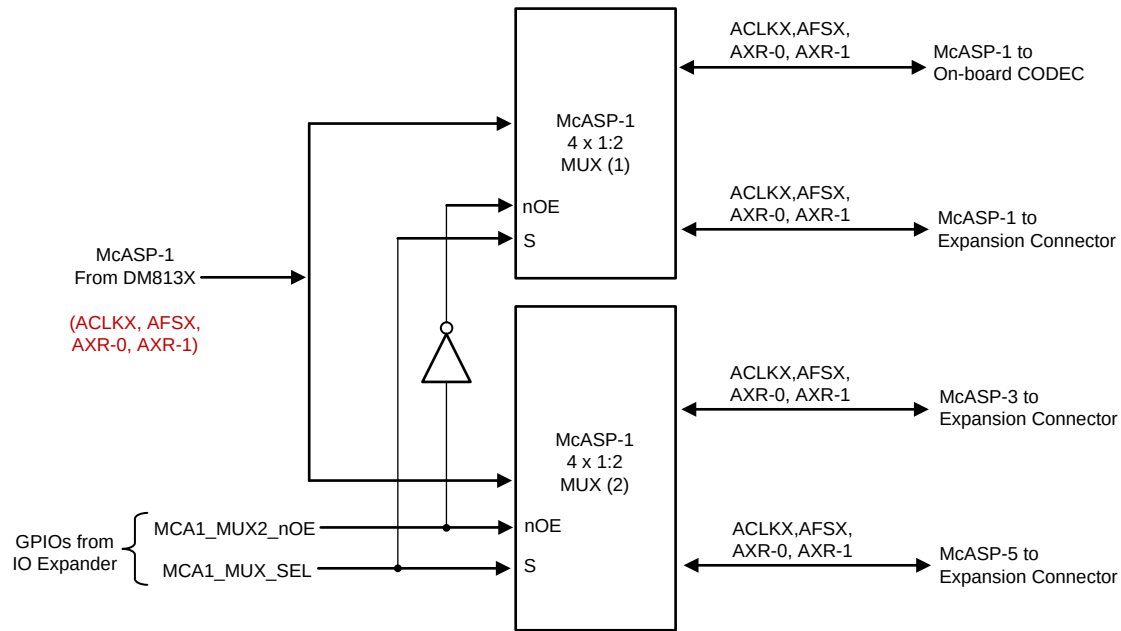
MCA0_DEC_B	MCA0_DEC_A	Output From Decoder	Mux Selected	McASP0 is Mapped to
0	0	Not used	—	—
0	1	MCA0_nOE_CONN4 is LOW	BUS FET SWITCH-2 (CH 2)	McASP4
1	0	MCA0_nOE_CONN2 is LOW	BUS FET SWITCH-2 (CH 1)	McASP2
1	1	MCA0_nOE_CONN0 is LOW	BUS FET SWITCH-1	McASP0

NOTE: Interfaces on the application boards that use McASP0, McASP2, or McASP4 cannot be tested at the same time.

2.4.2 McASP1 Muxing

Figure 2-9 shows the McASP1 muxing.

Figure 2-9. McASP1 Muxing



Copyright © 2016, Texas Instruments Incorporated

McASP1 is mapped to the onboard codec, McASP1, McASP3, McASP5. McASP1 signals MCA1_ACLKX, MCA1_AFSX, MCA1_AXR[0], and MCA1_AXR[1] are mapped to other interfaces using two 4 × [2:1] MUXs. Two GPIOs from the I/O expander are used to select the required interfaces (codec, McASP1, McASP3, McASP5) from McASP1 lines using a MUX.

GPIO MCA1_MUX2_nOE from the I/O expander is used to enable any multiplexer IC, and GPIO MCA1_MUX_SEL is used to select a particular channel (or particular interface) from the MUX that is enabled.

Table 2-5 provides the McASP1 muxing.

Table 2-5. McASP1 Muxing

MCA1_MUX2_nOE	MCA1_MUX_SEL	MUX Selected	McASP1 is Mapped to
0	0	MUX2 (CH 1)	McASP5
0	1	MUX2 (CH 2)	McASP3
1	0	MUX1 (CH 1)	McASP1 on expansion connector
1	1	MUX1 (CH 2)	Onboard codec

The default state of GPIOs from the I/O expander is high (logic 1). By default, McASP1 is mapped to the onboard codec.

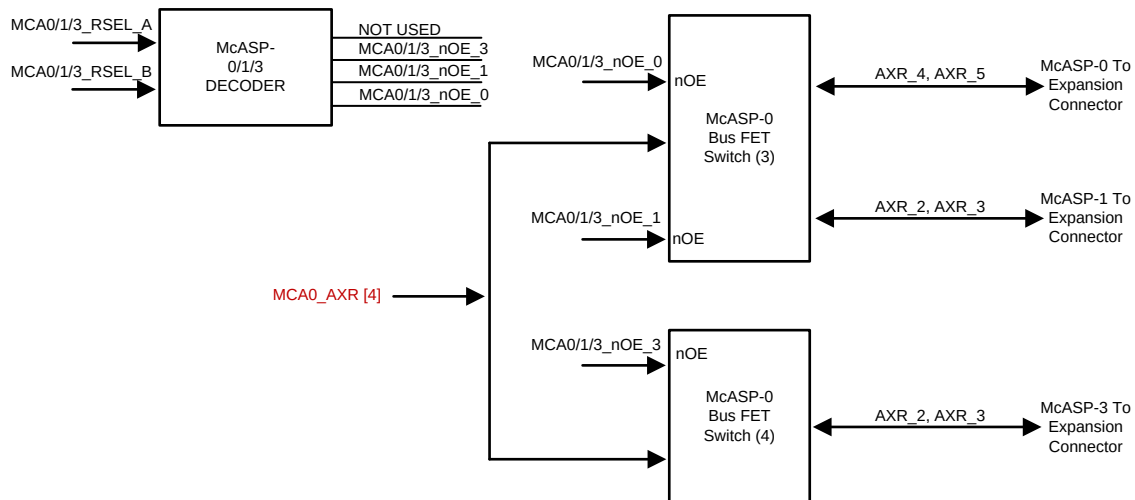
NOTE: Interfaces that use McASP1, McASP3, McASP5 cannot be tested at the same time. When McASP1 must be routed to expansion connectors to test the interfaces on the application boards, the onboard codec must be disabled.

2.4.3 McASP0_AXR [4:5] Lines Muxing

In Centaurus, McASP0 has five data channels (MCA0_AXR[0:9]), McASP1 has two data channels (MCA1_AXR[0:3]), and McASP3 also has two data channels (MCA3_AXR[0:3]). In the DM388, McASP0 has three data channels (MCA0_AXR[0:5]) and McASP1 has one data channel (MCA1_AXR[0:1]). Because McASP3 is muxed with McASP1 signals and MCA0_AXR[4:5], MCA1_AXR[2:3], and MCA3_AXR[2:3] are used on the application boards, hence the EVM provides one more muxing option to select between MCA0_AXR[4:5], MCA1_AXR[2:3], and MCA3_AXR[2:3].

Figure 2-10 shows the McASP0 muxing.

Figure 2-10. McASP0 Muxing



Copyright © 2016, Texas Instruments Incorporated

MCA0_AXR[4:5] is used as an input to MUXs, and a decoder is used to select one interface at a time. Input to the decoder is taken from the I/O expander. The following GPIOs are HIGH by default and map the inputs to McASP0_AXR[4:5] that are connected to expansion connector.

- MCA0_RSEL_A
- MCA1_RSEL_A
- MCA2_RSEL_A
- MCA0_RSEL_B

- MCA1_RSEL_B
- MCA3_RSEL_B

Table 2-6 lists the selections.

Table 2-6. McASP0_AXR Muxing

MCA0/1/3_RSEL_B	MCA0/1/3_RSEL_A	Output from decoder	MUX selected	MCA0_AXR[4:5] is Mapped to
0	0	Not used	—	—
0	1	MCA0/1/3_nOE_3	BUS FET SWITCH-4	MCA3_AXR[2:3]
1	0	MCA0/1/3_nOE_1	BUS FET SWITCH-3 (CH 2)	MCA1_AXR[2:3]
1	1	MCA0/1/3_nOE_0	BUS FET SWITCH-3 (CH 1)	MCA0_AXR[4:5]

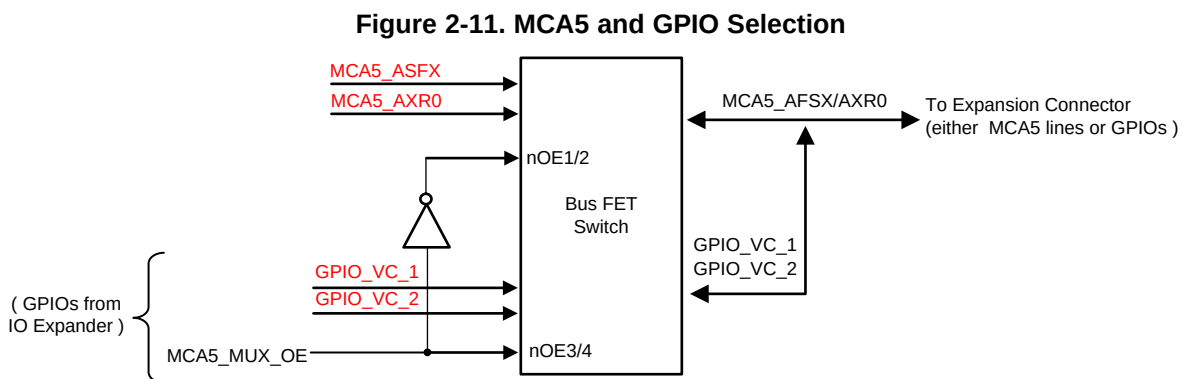
NOTE: McASP0 and McASP1 muxing must be considered before selecting the MCA0_AXR[4:5] lines. Ensure that McASP0 lines are selected by using other muxing schemes before opting for MCA0_AXR[4:5] lines to McASP0. Similarly, before opting MCA0_AXR[4:5] lines that are mapped to MCA1_AXR[2:3] and MCA3_AXR[2:3], ensure that McASP1 and McASP3 are selected using other muxing schemes.

2.4.4 McASP5 and GPIO Selection for VC Board

The McASP5 signals (MCA5_AFSX and MCA5_AXR0) are used as GPIOs on the video conference board. McASP5 signals are mapped from McASP1 on the DM388 EVM, and McASP1 lines on the DM388 cannot be configured as GPIOs. As a result, DM388 EVM provides a muxing option of McASP5 lines (MCA5_AFSX and MCA5_AXR0) that are mapped from McASP1 and two GPIOs (GPIO_VC_1 and GPIO_VC_2) from the I/O expander. The output (MCA5_AFSX_EXP and MCA5_AFSX_EXP) from the MUX stage is routed to the expansion connector.

When the VCONF board is plugged in, signals on the expansion connectors are used as GPIOs. These signals can be used as McASP5 lines when other application boards are plugged in.

Figure 2-11 shows the selection of either MCA5 lines or GPIOs from the I/O expander by using a GPIO (MCA5_MUX_OE) from the same I/O expander.



Copyright © 2016, Texas Instruments Incorporated

Table 2-7 shows the selection.

Table 2-7. Channel Selection

MCA5_MUX_OE	Channel Selected	Signals on Expansion Connector
1	CH 1	MCA5_AFSX and MCA5_AXR0
0	CH 2	GPIO_VC_1 and GPIO_VC_2

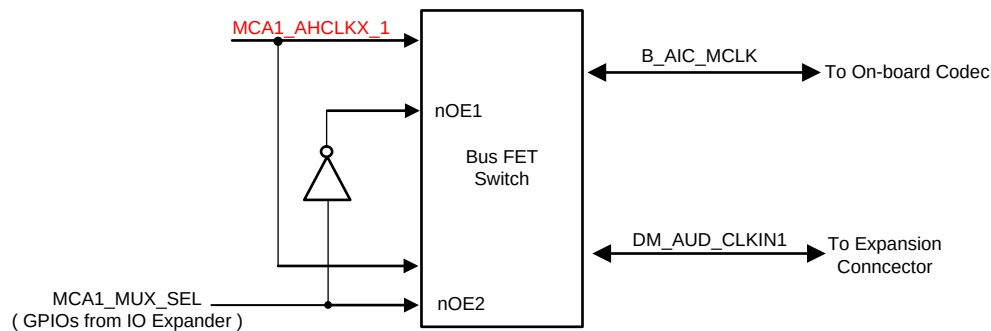
By default, MCA5_AFSX and MCA5_AXR0 are available on the expansion connector if McASP5 is enabled in the McASP1 muxing scheme.

2.4.5 MCA1_AHCLKX Muxing

MCA1_AHCLKX is used in the Centaurus EVM to provide an option to get MCLK for the onboard codec or it will be routed to the expansion connector. In the DM388, ensure that MCA1_AHCLKX provides the same option as it does in the Centaurus EVM.

GPIO MCA1_MUX_SEL from the I/O expander is used to select the required output (see Figure 2-12).

Figure 2-12. Required Output Selection



Copyright © 2016, Texas Instruments Incorporated

Table 2-8 lists the channel selection and output.

Table 2-8. Channel Selection and Output

MCA1_SEL_OE	Channel Selected	OUTPUT
1	CH 1	B_AIC_MCLK (codec)
0	CH 2	DM_AUD_CLKIN1 (expansion)

By default, MCA1_AHCLKX is connected to the onboard codec (B_AIC_MCLK) because the GPIO from the I/O expander is high.

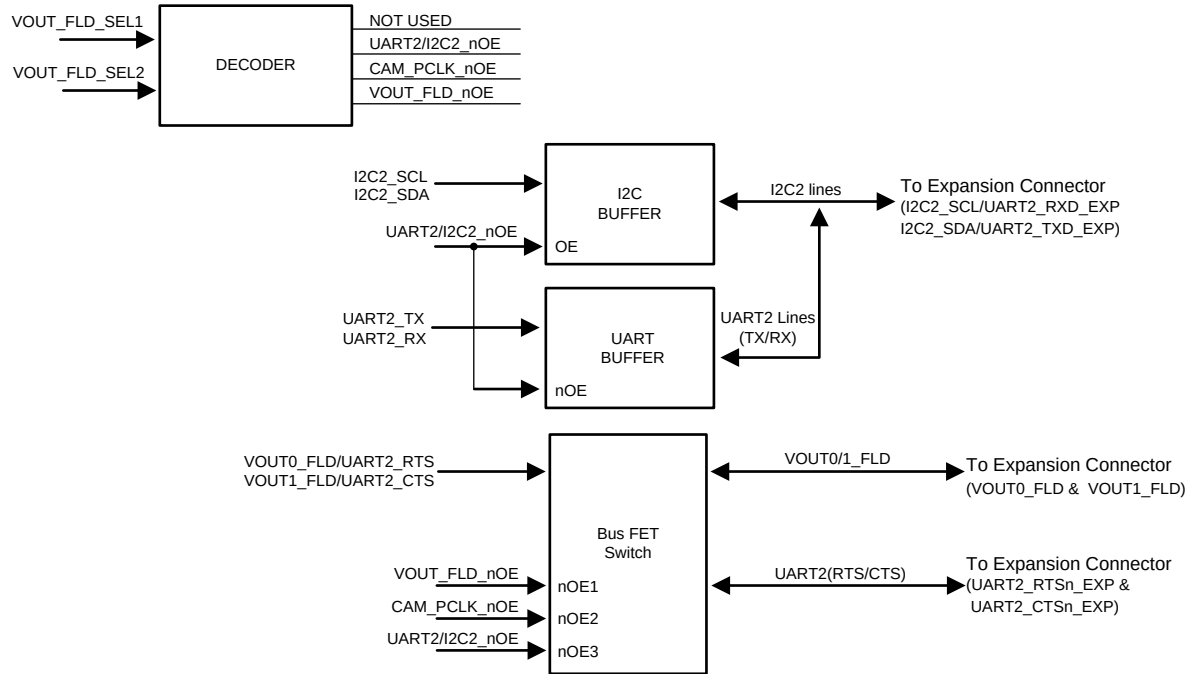
2.5 UART2, I2C2, and VOUT Muxing

In Centaurus, UART3 (TX and RX) and I2C2 (SCL and SDA) are pin multiplexed. These signals are connected to the expansion connector and are used on the application boards as UART3 or as I2C2 signals. However, the UART3 interface is not available on the DM388. Instead of UART3, UART2 signals are used on the DM388 device. Because the I2C2 signals are not pin multiplexed with UART2 signals, the DM388 EVM provides an option to select UART2 (TX and RX) or I2C2 (SCL and SDA) and route the selected signals to the expansion connector.

The UART3 (RTS and CTS) signals are pin multiplexed with UART0 (RIN and DTRn) in Centaurus. UART2 is used instead of UART3 on the DM388, and UART2 (RTS and CTS) lines are pin multiplexed with VOUT0 and VOUT1 lines.

The UART2_RTS signal is pin muxed with VOUT0_FLD and CAM_PCLK, and the UART2_CTS signal is pin muxed with VOUT1_FLD. The EVM provides a logic using a MUX, a buffer, and a decoder to get UART3 or I2C2 and VOUT0 and VOUT1 (see Figure 2-13).

Figure 2-13. UART2, I2C2, and VOUT Muxing



Copyright © 2016, Texas Instruments Incorporated

Table 2-9 lists the I/O expander GPIOs (VOUT_FLD_SEL1 and VOUT_FLD_SEL2) that are used as input-to-decoder.

By default, inputs to the decoder are high, so VOUT_FLD_nOE = LOW is selected and VOUT0_FLD and VOUT1_FLD signals are routed to the expansion connector. Because all other outputs from the decoder are high, when UART2 and I2C2_nOE are high, the I2C2 buffer is enabled. So, I2C2, VOUT0_FLD, and VOUT1_FLD lines will be enabled by default.

When UART2 and I2C2_nOE are LOW, the UART2 signals (TX, RX, RTS, and CTS) are available on the expansion connectors. I2C2 and VOUT lines are not available whenever UART2 signals are selected.

Table 2-9. I/O Expander GPIOs

VOUT_FLD_SEL2	VOUT_FLD_SEL1	Output From Decoder	Device Selected	OUTPUT
0	0	Not used	—	—
0	1	UART2/I2C2_nOE	Bus FET switch (CH 3)	UART2 signals. I2C2 buffer is disabled.
1	0	CAM_PCLK_nOE	I ² C buffer and VOUT bus FET switch (CH 2)	VOUT0_FLD as i/p (CAM_PCLK). I2C2 buffer is enabled.
1	1	VOUT_FLD_nOE	I ² C buffer and VOUT bus FET switch (CH 1)	VOUT0_FLD and VOUT1_FLD. I2C2 buffer is enabled.

Physical Description

This chapter provides information about the physical characteristics of the board.

Topic	Page
3.1 DM388 EVM Layout	38
3.2 Connectors, Switches, Headers, and Jumpers	39
3.3 Test Points	64
3.4 Expansion Connector	66

3.1 DM388 EVM Layout

The DM388 base EVM has the following dimensions:

- 317.5 mm × 187.96 mm
- 10-layer PCB
- 2-cm height (completed PCB)

Figure 3-1 shows the top view of the DM388.

Figure 3-1. TMDXEVM388 Base EVM (Top View)

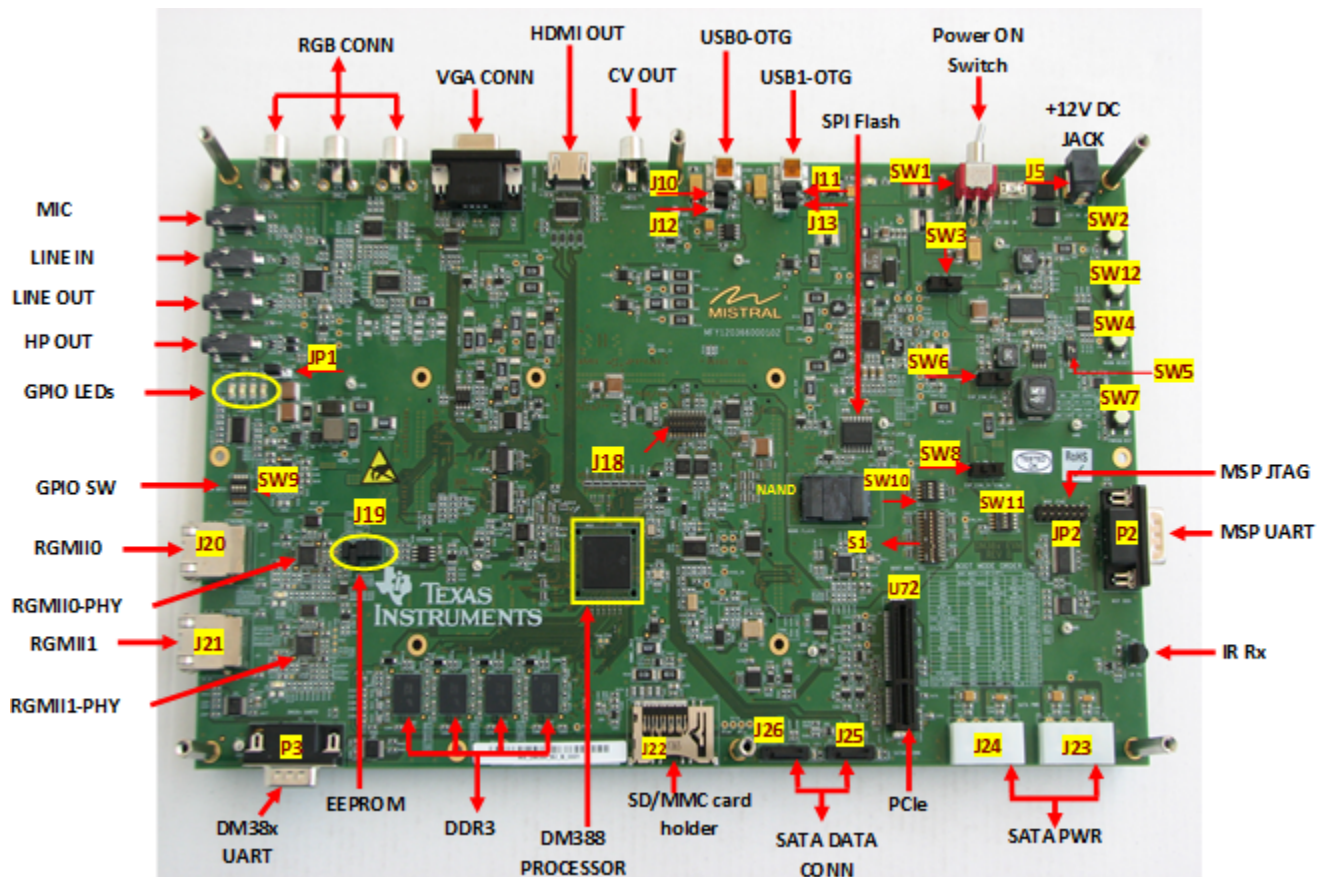
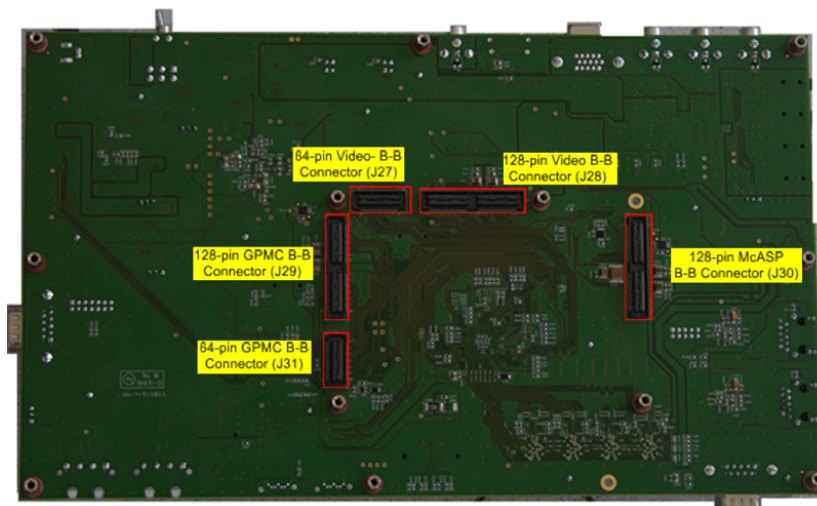


Figure 3-2 shows the bottom view of the DM388.

Figure 3-2. TMDXEVM388 Base EVM (Bottom View)



3.2 Connectors, Switches, Headers, and Jumpers

The DM388 base EVM has several connectors, switches, headers, and jumpers that serve various purposes. These components are detailed in the subsections that follow.

3.2.1 SD/MMC Card Holder

The SD/MMC card holder is a 28-pin connector that is on the top side of the board; the card holder provides an interface to a SD/MMC card. Figure 3-3 shows the location of SD/MMC connector on the base EVM.

Figure 3-3. SD/MMC Card Holder

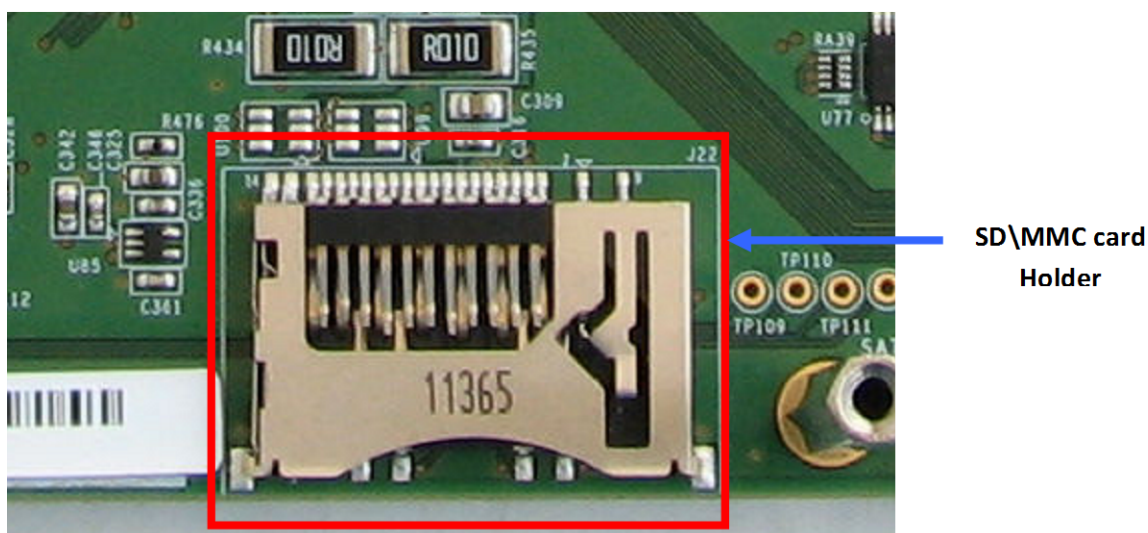


Table 3-1 provides the pinout details of the SD/MMC card holder (J22).

Table 3-1. Pinout of SD/MMC Card Holder

Pin Number	Signal Name	Pin Number	Signal Name
1	MMC1_DAT3	15	MMC1_SD_CD
2	MMC1_CMD	16	NC
3	GND	17	NC
4	VMMC	18	GND
5	MMC1_CLK	19	NC
6	GND	20	NC
7	MMC1_DAT0	21	GND
8	MMC1_DAT1	22	NC
9	MMC1_DAT2	23	NC
10	NC	24	NC
11	NC	25	NC
12	NC	26	NC
13	NC	27	GND
14	MMC1_SD_WP	28	GND

3.2.2 JTAG Header

A JTAG emulator can be used for advanced debugging by connecting it to the JTAG header on the top side of the EVM. The JTAG header has 20 pins (10 × 2, 1.27-mm pitch). If the user has a 14-pin JTAG version, then users must contact their emulator supplier for the appropriate adapter. All JTAG signal levels are 3.3 V.

Figure 3-4 shows the location of the JTAG header.

Figure 3-4. JTAG Header

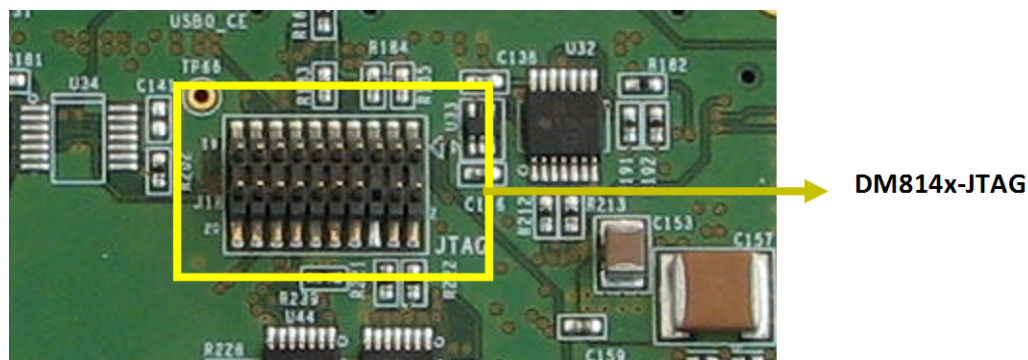


Table 3-2 provides the pinout details of the JTAG header (J18).

Table 3-2. Pinout of JTAG Header

Pin Number	Signal Name
1	TMS
2	TRSTN
3	TDI
4	TDIS
5	TVD
6	KEY
7	TDO
8	GND1
9	TCKRTN
10	GND2
11	TCLK
12	GND3
13	EMU0
14	EMU1
15	SRST
16	GND4
17	EMU2
18	EMU3
19	EMU4
20	GND5

3.2.3 Component Video Out

A T.V. or monitor that supports HD DAC inputs can be connected to the component video connectors (RGB connectors) of the base EVM board by using a component video cable. HD DAC signals from the DM388 processor are connected to the RGB connectors through video-amplifier U5. Component video connectors J7 (green), J9 (blue), and J6 (red) are 4-pin connectors (see Figure 3-5).

Figure 3-5. Component Video Connectors

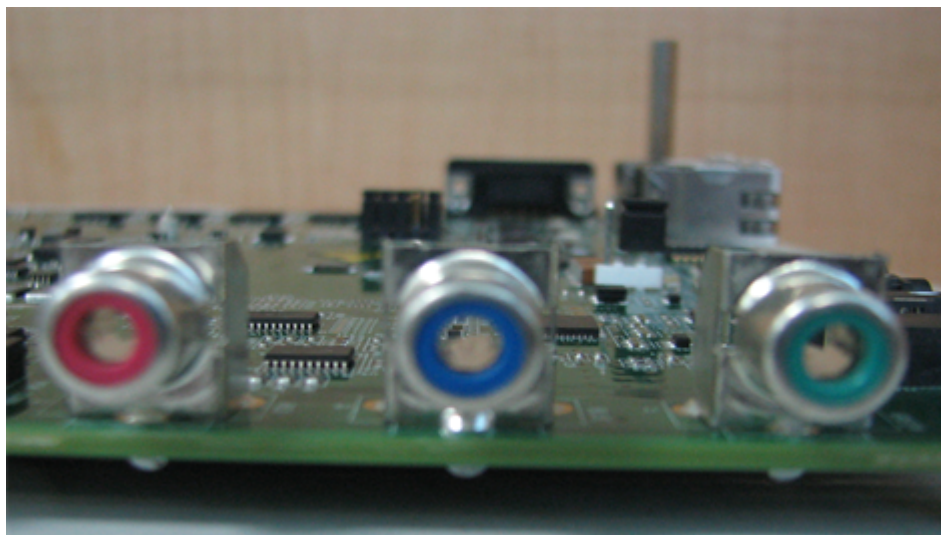


Table 3-3 provides the pinout details of the RGB connectors.

Table 3-3. Pinout of RGB Connector

Pin Number	Signal
1	VIDEO OUT
2	GND
3	GND
4	GND

Figure 3-6 shows an example of a component video cable.

Figure 3-6. Component Video Cable



3.2.4 VGA Connector

A VGA cable can be used to connect a T.V. or monitor to the DM388 EVM through the VGA connector (P1) provided on the board. HD DAC signals from the video-amplifier (U5) are shared with VGA connector P1. VGA connector P1 is a 15-pin female connector.

Signals from U5 are passed through ESD protection IC TPD7S019-15DBQR and then go to the VGA connector.

Figure 3-7 shows a top view and side view of the VGA connector.

Figure 3-7. VGA Connector

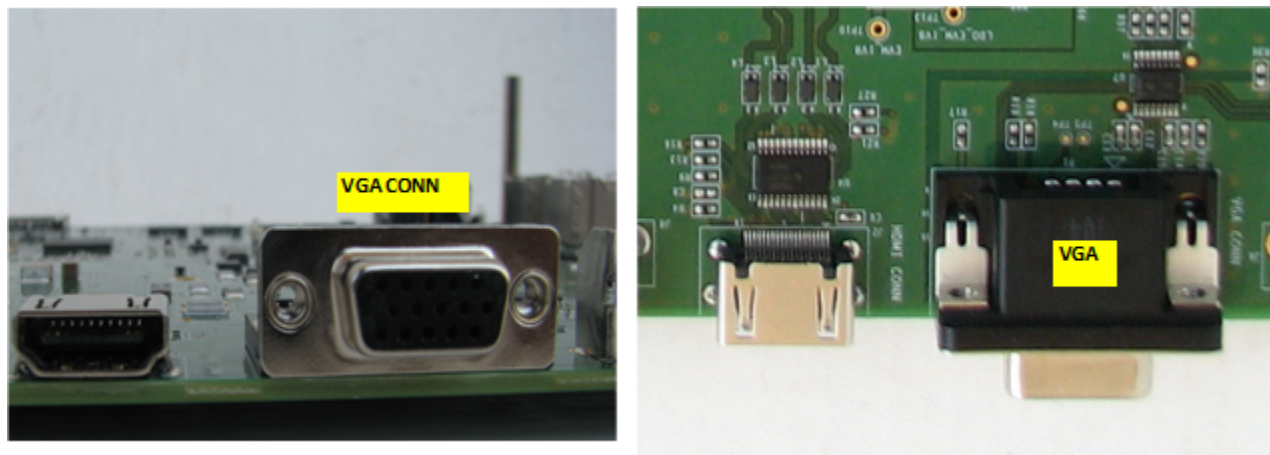


Table 3-4 provides the pinout details of the VGA connector.

Table 3-4. Pinout of VGA Connector

Pin Number	Signal Name
1	Red video
2	Green video
3	Blue video
4	NC
5	GND
6	GND
7	GND
8	GND
9	EVM_5V0
10	GND
11	NC
12	I2C2_SDA_BUF
13	VGA_HSYNC
14	VGA_VSYNC
15	I2C2_SCL_BUF

Figure 3-8 shows an example of a VGA male-to-male cable.

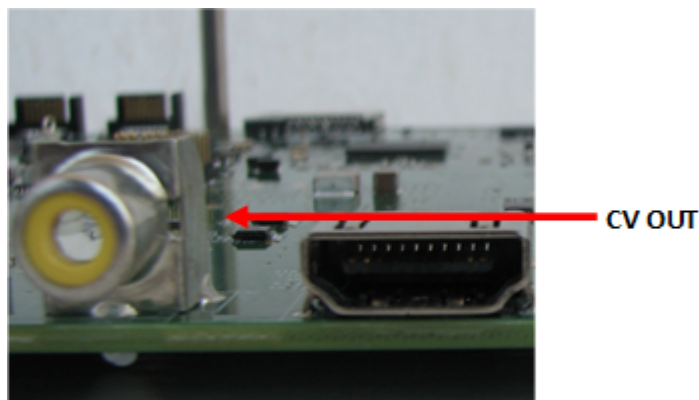
Figure 3-8. VGA Male-to-Male Cable



3.2.5 Composite Video Connector

A composite video (CV) cable is used to connect a T.V. or monitor to the base board through the RCA jack (J8) provided on the board. Figure 3-9 shows J8 as viewed from the card edge.

Figure 3-9. Composite Video Out Connector



Composite video connector J8 is a 4-pin RCA connector. Do not plug the cable into connector J8 while the board is powered on.

Table 3-5 provides the pinout details of the CV OUT on the RCA connector.

Table 3-5. CV OUT

Pin Number	Signal
1	VIDEO OUT
2	GND
3	GND
4	GND

Figure 3-10. Composite Video Cable



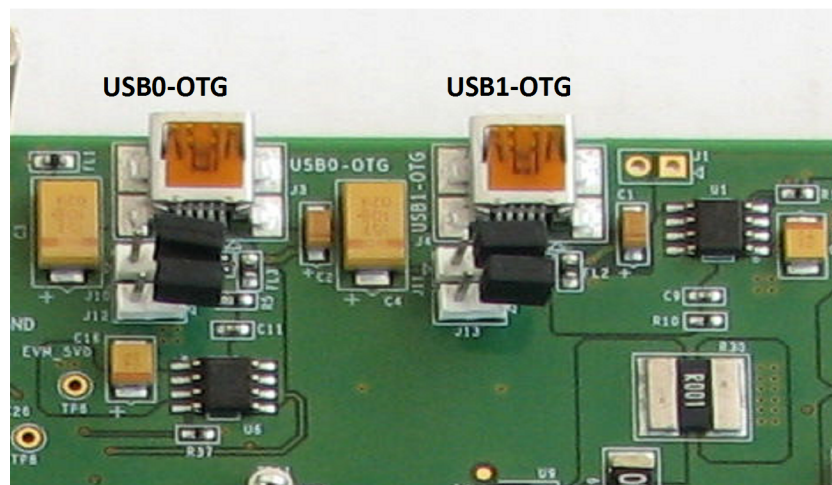
3.2.6 USB-OTG Connector

The DM388 EVM is equipped with two USB-OTG connectors (J3 and J4). Both USB interfaces are capable of dynamic role change; they can act as a host or as a device. TPD2E001DRLR ESD protection devices U2 and U3 are used for USB0 and USB1, respectively.

While configuring the OTGs in host-only mode, the header must be placed on J10 and J12 for USB0, and on J11 and J13 for USB1. Type A to mini-AB adapter is used to connect a memory stick, mouse, or other USB slave devices. The USBBx_DRV_VBUS signal from the processor is given to TPS2065DR (U6 and U1). This signal is driven high, enabling the TPS2065 IC to provide USBx_VBUS voltage to a connected slave device.

Figure 3-11 shows the connectors on the side of the board.

Figure 3-11. USB-OTG Connectors



The USB-OTG connector is a 9-pin, mini-AB connector. Table 3-6 provides the pinout details of the USB-OTG connector (J3 and J4).

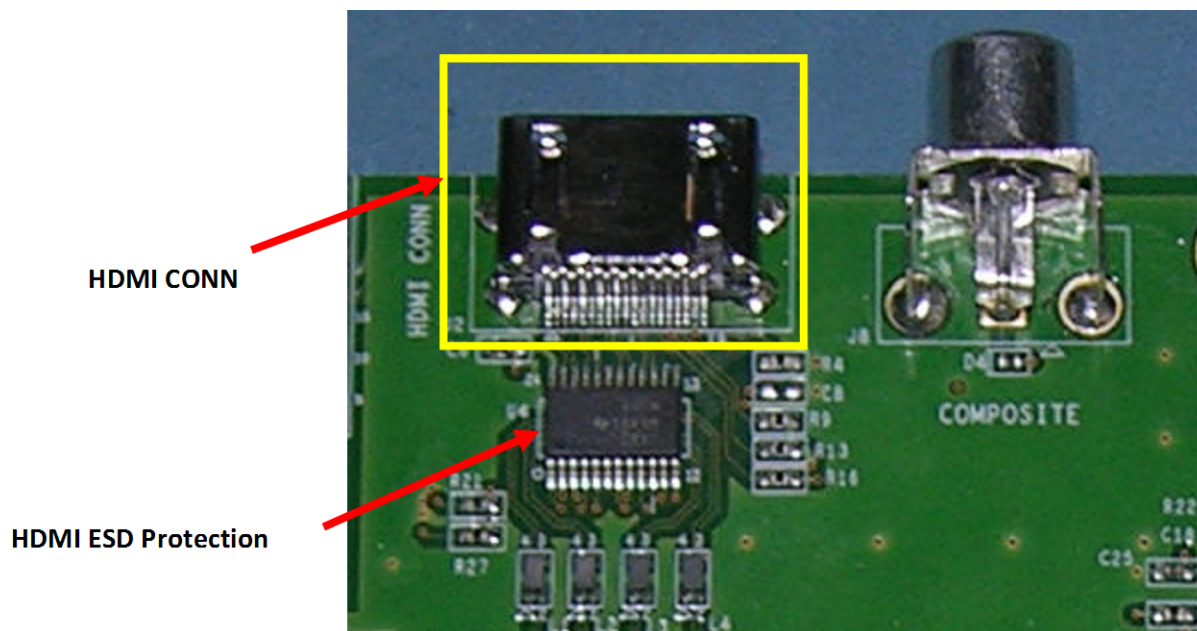
Table 3-6. Pinout of USB-OTG Connector

Pin Number	Pin Name	Pin Number	Pin Name
1	VCC	6	SH1
2	D+	7	SH2
3	D-	8	SH3
4	ID	9	SH4
5	GND		

3.2.7 HDMI OUT Connector

Any T.V. or monitor with an HDMI connection can be connected to the DM388 EVM through the HDMI connector. This connector is on the top side of the EVM. The HDMI signals from the processor are routed to the HDMI connector (J2) through an ESD protection device (TPD12S016PWR [U4]). [Figure 3-12](#) shows the HDMI connector.

Figure 3-12. HDMI Connector



The HDMI connector is a 23-pin, type-A receptacle connector. [Table 3-7](#) provides the pinout details of HDMI OUT J2.

Table 3-7. Pinout of HDMI OUT

Pin Number	Signal Name	Pin Number	Signal Name
1	HDMI_D2+	2	GND
3	HDMI_D2–	4	HDMI_D1+
5	GND	6	HDMI_D1–
7	HDMI_DO+	8	GND
9	HDMI_DO–	10	HDMI_CLK+
11	GND	12	HDMI_CLK–
13	CE_REMOTE_OUT	14	NC
15	DDC_CLK	16	DDC_DAT
17	GND	18	5V_OUT_HDMI
19	HDMI_HP_OUT	20	GND
21	GND	22	GND
21	GND	—	—

Figure 3-13 shows an example of an HDMI cable.

Figure 3-13. HDMI Cable



3.2.8 Ethernet Connector

The DM388 EVM has two RJ-45 connectors with magnetics for RGMII0 and RGMII1 interfaces. Both connectors are connected to the respective Ethernet PHY transceivers (AR8031-AL1A) through parallel termination. The AR8031-AL1A supports WoL interrupt to detect the magic packet and notify the sleeping system to wake up. The ENETx_WoL signal from U52 or U66 is given to GP0[12] of the DM388 processor through an OR gate (U53).

Figure 3-14 shows the Ethernet connectors.

Figure 3-14. Ethernet Connectors

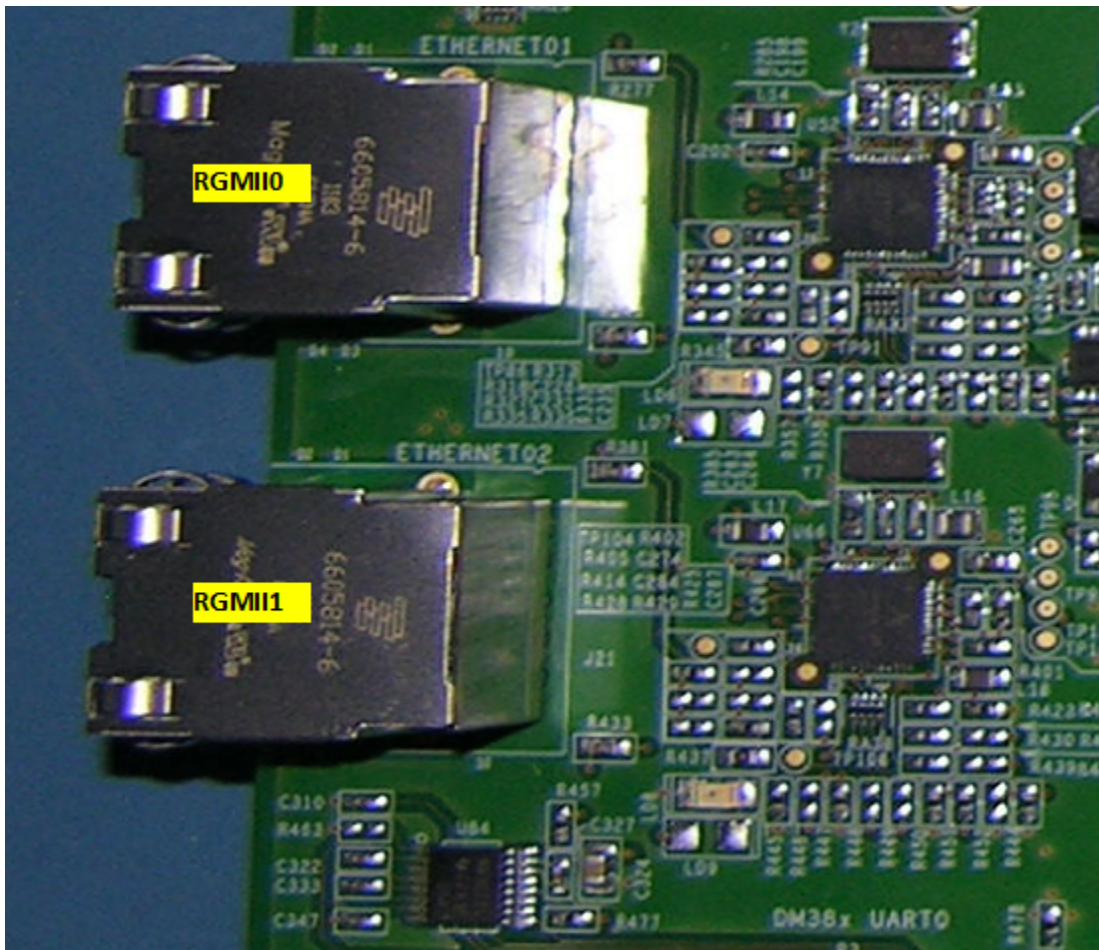


Table 3-8 provides the pinout details of the Ethernet connectors.

Table 3-8. Pinout of Ethernet Connectors

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	PHY_VDD_2V5
3	TRD[3]P	4	TRD[2]N
5	TRD[2]P	6	TRD[2]N
7	TRD[1]P	8	TRD[1]N
9	TRD[0]P	10	TRD[0]N
D1	ENET_LED_LINK	D2	GND
D3	ENET_LED_RX	D4	EVM_3V3
SH1	GND	SH2	GND

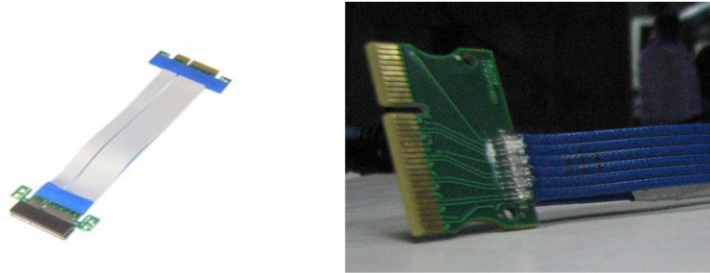
Table 3-9 provides the pinout details of the PCIe connector.

Table 3-9. Pinout of PCIe Connector

Pin Number	Pin Description	Pin Number	Pin Description
B1	IP_EVM_12V	A1	PRSNT#
B2	IP_EVM_12V	A2	IP_EVM_12V
B3	IP_EVM_12V	A3	IP_EVM_12V
B4	GND	A4	GND
B5	NC	A5	TCK
B6	NC	A6	TDI
B7	GND	A7	NC
B8	PCI_3V3	A8	TMS
B9	TRSTn	A9	PCI_3V3
B10	NC	A10	PCI_3V3
B11	NC	A11	PCI_CON_PORz
B12	NC	A12	GND
B13	GND	A13	REFCLKp
B14	CON.PCIE_TXP0	A14	REFCLKn
B15	CON.PCIE_TXN0	A15	GND
B16	GND	A16	CON.PCIE_RXP0
B17	PRSNT#	A17	CON.PCIE_RXN0
B18	GND	A18	GND
B19	NC	A19	NC
B20	NC	A20	GND
B21	GND	A21	NC
B22	GND	A22	NC
B23	NC	A23	GND
B24	NC	A24	GND
B25	GND	A25	NC
B26	GND	A26	NC
B27	NC	A27	GND
B28	NC	A28	GND
B29	GND	A29	NC
B30	NC	A30	NC
B31	PRSNT#	A31	GND
B32	GND	A32	NC

Figure 3-16 shows an example of a PCIe cable.

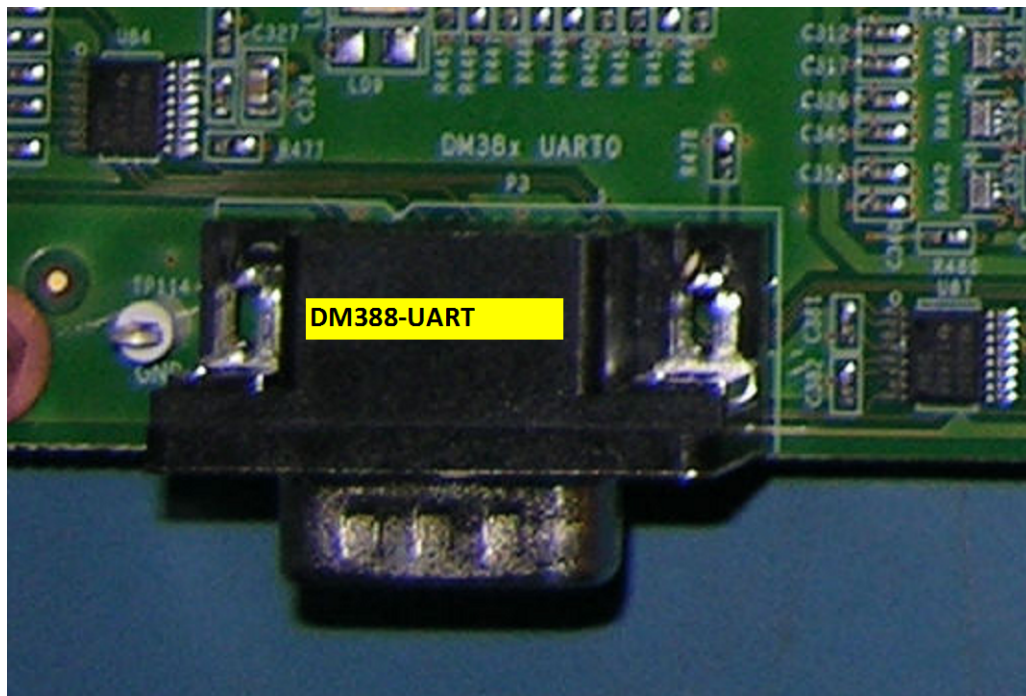
Figure 3-16. PCIe Cable



3.2.10 UART Connector

The EVM has two UART DB-9 connectors. One UART connector (P3) is connected to the DM388 through the RS-232 transceiver. The other UART connector (P2) is connected to the MSP430 MCU through the RS-232 transceiver. Figure 3-17 shows the UART connector of the DM388 device.

Figure 3-17. UART Connector



The voltage- and current-monitoring results calibrated by the MSP430 MCU can be viewed on the console through MSP430 UART connector.

Figure 3-18 shows the UART connector of the MSP430.

Figure 3-18. MSP430 UART Connector

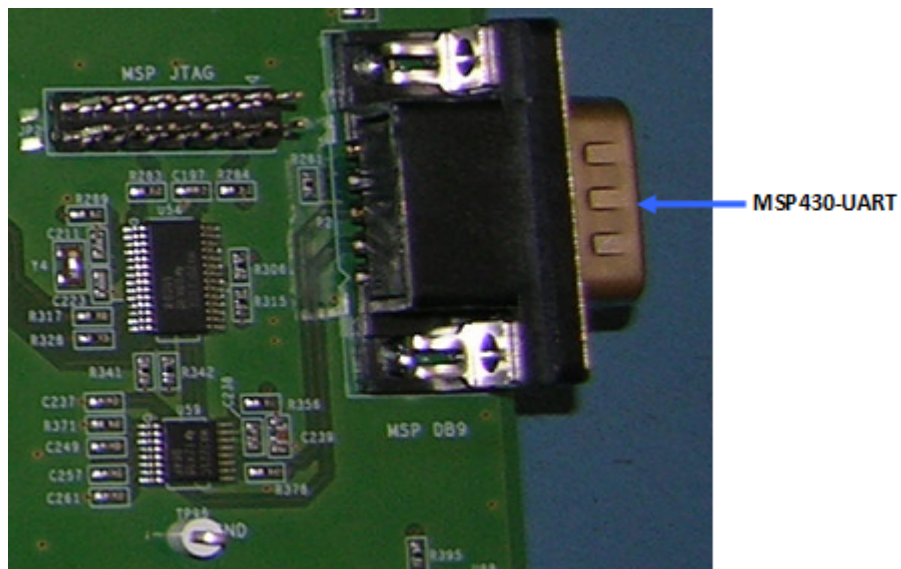


Table 3-10 provides the pinout details of the UART connectors.

Table 3-10. Pinout of UART Connectors

Pin Number	Description	Pin Number	Description
1	NC	7	RTS
2	RXD	8	CTS
3	TXD	9	NC
4	NC	10	UART_GND
5	GND	11	UART_GND
6	NC	—	—

Figure 3-19 shows a UART F-F serial cable.

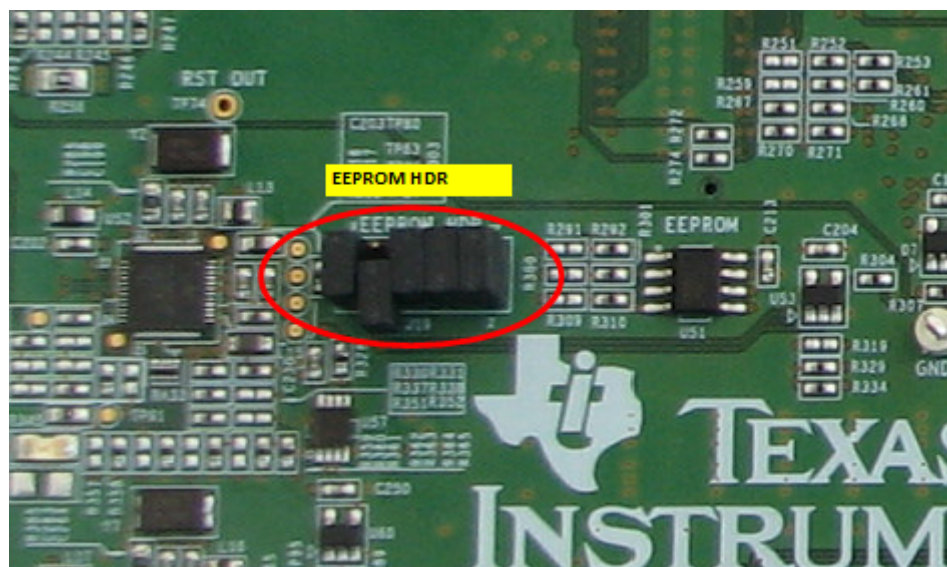
Figure 3-19. UART F-F Serial Cable



3.2.11 EEPROM Header

The DM388 EVM has five 2-pin EEPROM headers on the board. A jumper should be put on the header as shown in [Figure 3-20](#). To get the default connection from the DM388, place the jumper between pins 1 and 2, 3 and 4, 5 and 6, and 9 and 10. Do not place a jumper between pins 7 and 8. Pins 7 and 8 must be shorted for the write-protect function of EEPROM.

Figure 3-20. EEPROM Header



[Table 3-11](#) provides the pinout details of the EEPROM header.

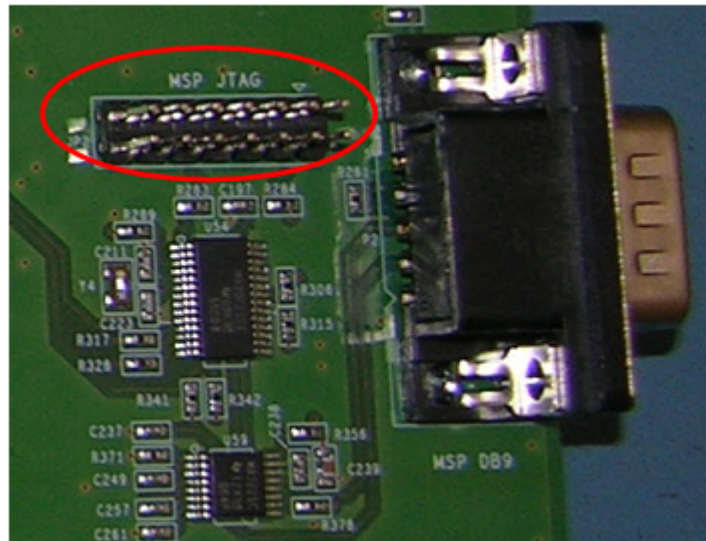
Table 3-11. Pinout of EEPROM Header

Pin Number	Description	Pin Number	Description
1	EVM_3V3	2	PROM_EVM_3V3
3	I2C0_SCL	4	PROM_I2C0_SCL
5	I2C0_SDA	6	PROM_I2C0_SDA
7	EVM_3V3	8	PROM_WP
9	GND	10	GND

3.2.12 MSP JTAG Header

The MSP430 MCU is used to monitor the voltage and current ratings on the chosen power rails that are connected to INA226 devices. INA226 devices are controlled through I2C0 lines. The MSP430 MCU must be programmed through the MSP430 emulator that is connected to the MSP JTAG header (JP2). The calibrated results can be observed on the console through the MSP-DB9 connector. [Figure 3-21](#) shows the MSP JTAG header.

Figure 3-21. MSP JTAG Header



The DM388 EVM has a 14-pin (2 × 7), 2.54-mm pitch JTAG header to access the MSP430 MCU. [Table 3-12](#) provides the pinout details of the MSP JTAG header.

Table 3-12. Pinout of MSP JTAG Header

Pin Number	Signal Name	Pin Number	Signal Name
1	MSP430_TDO/TDI	8	NC
2	NC	9	NC
3	NC	10	NC
4	EVM_3V3	11	NC
5	NC	12	NC
6	NC	13	NC
7	MSP430_TCK	14	NC

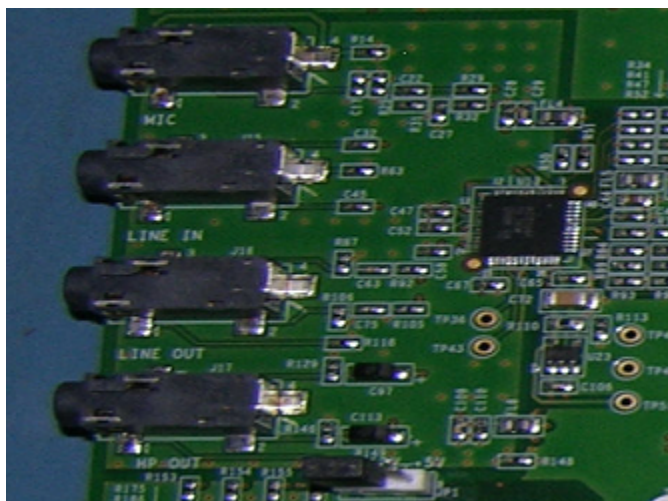
3.2.13 Audio Connectors

The DM81x and AM38x EVM includes an audio codec (TLV320AIC3106IRGZT) that is controlled through MCASP1 and I2C0 lines. The EVM has four audio connectors for different functions, such as:

- Headphone OUT (J17)
- Speaker OUT (J16)
- Audio LINE IN (J15)
- Microphone input (J14)

Figure 3-22 shows the audio codec connectors.

Figure 3-22. Audio Codec Connectors



Each connector is a 3.5-mm, 4-pin, female stereo jack that is connected to the audio codec through a coupling capacitor. Table 3-13 provides the pinout details of the audio LINE OUT connector.

Table 3-13. Pinout of Audio LINE OUT

Pin Number	Signal Name
1	GND
2	LEFT_OUT
3	RIGHT_OUT
4	NC

Table 3-14 provides the pinout details of the audio LINE IN connector.

Table 3-14. Pinout of Audio LINE IN

Pin Number	Signal Name
1	GND
2	LEFT_IN
3	RIGHT_IN
4	GND

Table 3-15 provides the pinout details of the audio MIC IN connector.

Table 3-15. Pinout of Audio MIC IN

Pin Number	Signal Name
1	GND
2	LEFT_IN
3	Shorted to pin 2
4	GND

Figure 3-23 shows examples of HP-out, mic-in, and line-in cables.

Figure 3-23. HP-Out, Mic-in, and Line-in Cables



3.2.14 Power Switches

The DM388 EVM has one DPDT switch (SW1) for main power (12-V supply) and three SPST, 3-pin slide switches for various purposes.

- SW3 (TOS65232 SW) – Connected to IP_EVM_12V when the switch position is toward the arrow mark, and off when it is away from the arrow mark.
- SW6 (EXP_EVM_3V3 SW) – Connected to EXP_EVM_3V3 when the switch position is away from the arrow mark, providing EVM_3V3 to the application board if required.
- SW8 (EXP_EVM_5V0 SW) – Connected to EXP_EVM_5V0 when the switch position is away from the arrow mark, providing EVM_5V0 to the application board if required.

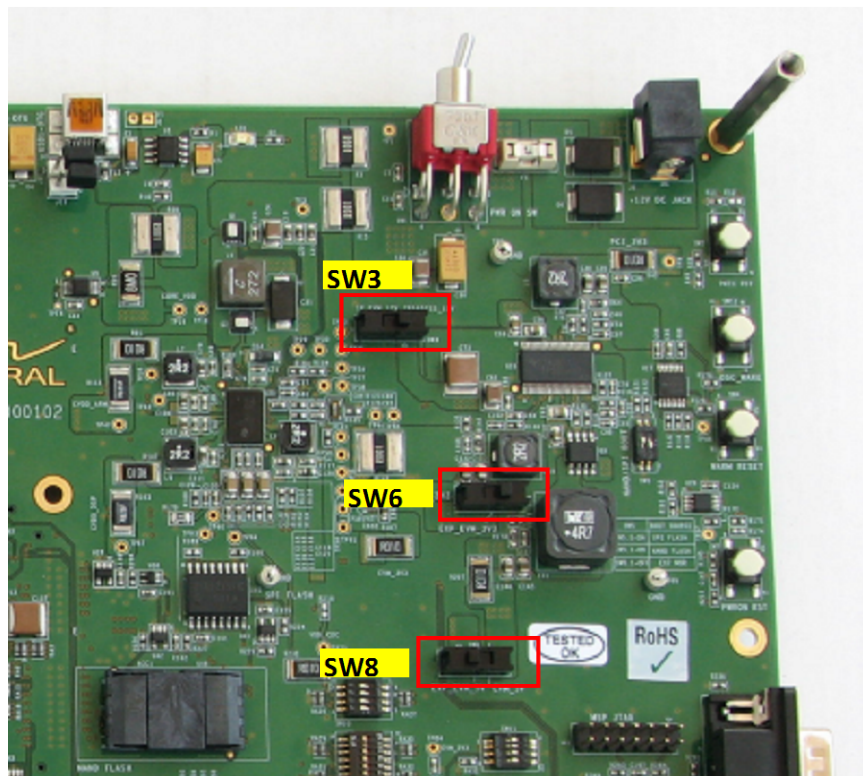
3.2.14.1 Default Switch Settings of EVM

Ensure the switches are positioned as follows when the EVM is powered on:

- SW3 – toward the arrow mark (right side)
- SW6 – toward the arrow mark (right side)
- SW8 – toward the arrow mark (left side)

Figure 3-24 shows the arrangement of the switches.

Figure 3-24. EVM Switch Arrangement



3.2.15 Boot Mode Switches

Switch positions 1 to 5 of S1 determine the order of boot modes. The first boot mode listed for each S1 [5:1] configuration is the primary boot mode. If the primary boot mode fails, the second, third, and fourth boot modes are executed in that order until a successful boot is completed.

The other positions of S1 [6:12] and SW10 [1:4] are reserved and are to be pulled down (off). The boot mode order table is silk screened on the EVM board for user convenience.

Figure 3-25 shows the boot mode switches.

Figure 3-25. Boot Mode Switches

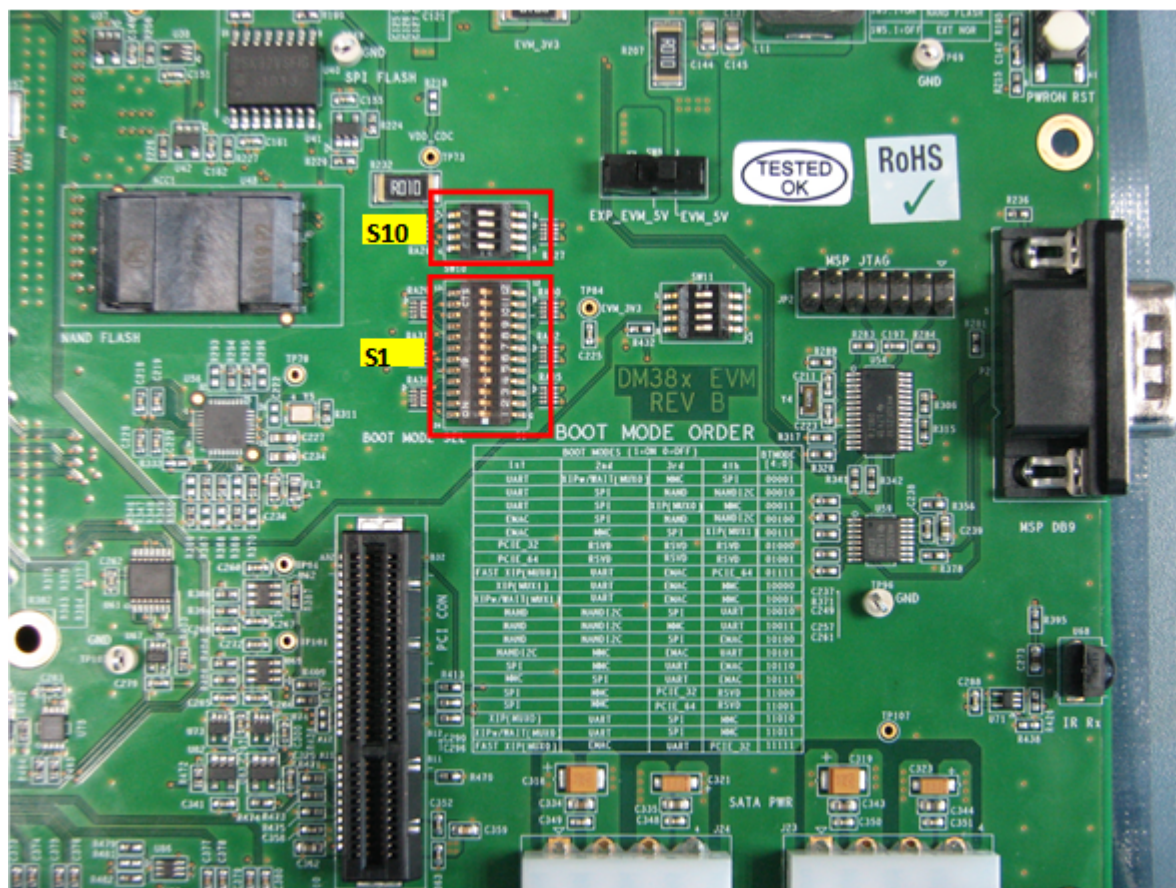


Table 3-16 provides the boot mode combinations.

Table 3-16. Boot Mode Combinations

S1.1	S1.2	S1.3	S1.4	S1.5	Boot Mode Order
0	1	0	0	1	NAND- NANDI2C- SPI- UART
1	0	0	0	0	UART-XIP/WAIT(MUX0)(1)-MMC-SPI
1	1	1	0	1	MMC-SPI –UART-EMAC
0	0	1	0	0	EMAC-SPI-NAND-NANDI2C

3.2.16 Reset Switch SW4

This switch generates a warm reset to the processor to reset all modules in the device except for the test and emulation logic and the EMAC switch. [Table 3-17](#) provides the two settings and results of the warm-reset push-button.

Table 3-17. Warm Reset Push-Button

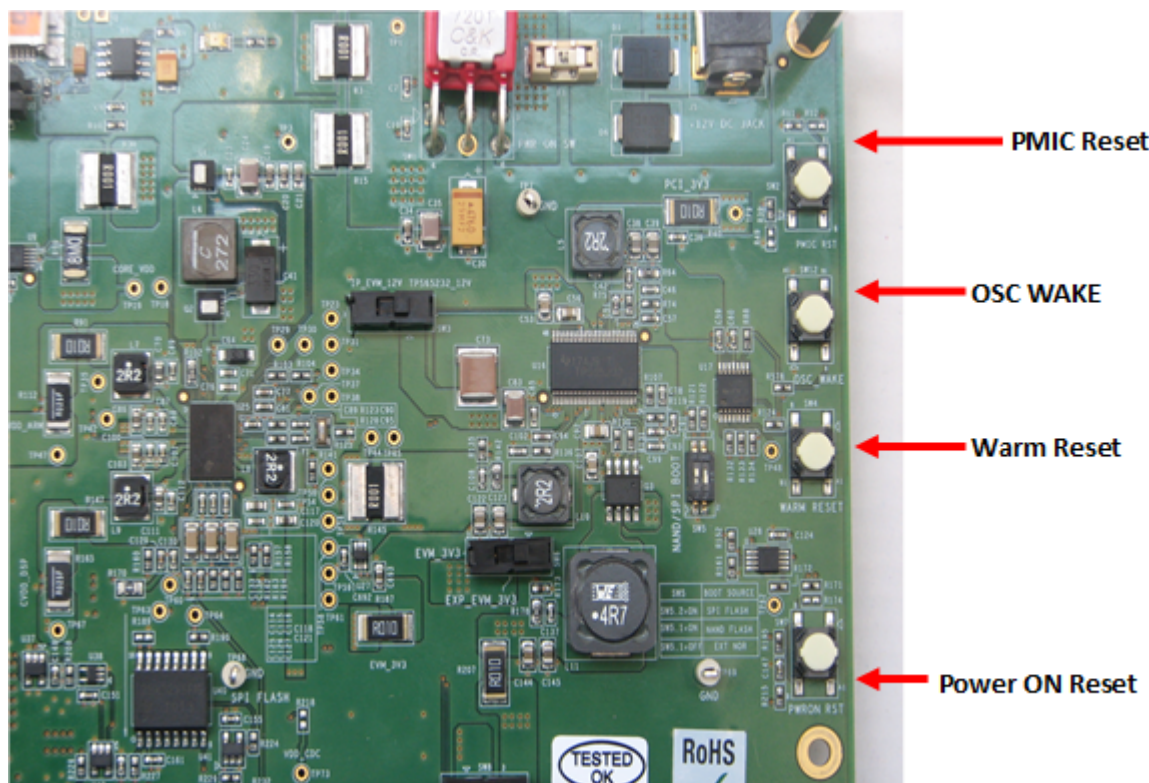
Setting	Result
Open	Normal operating condition. Open = logical 1 state
Push button closed	Active low reset signal. Closed = logical 0 state

The following sequence must be followed during a warm reset:

1. Ensure that the power supplies and input clock sources are stable.
2. Ensure that the RESET pin is asserted (low) for a minimum of 30 DEV clock cycles. The following things occur within the low period of the RESET pin:
 - All pins (except for the test and emulation pins) enter a Hi-Z mode and the associated pulls are enabled.
 - The PRCM asserts reset to all modules within the device, except for the test and emulation logic, EMAC switch, PLL, and clock configuration.
3. Deassert (drive high) the RESET pin. The following things occur when the RESET pin is deasserted:
 - All pins, except test and emulation pins, enter a Hi-Z mode and the associated pulls are enabled.
 - Reset to the ARM Cortex-A8 processor and modules without a local processor is deasserted except for the test and emulation logic, EMAC switch, PLL, and clock configuration.
 - If BTMODE[11] was latched as 0, then RSTOUT_WD_OUT is asserted for TBD DEV clock cycles.
 - The clock, reset, and power-down state of each peripheral is determined by the default settings of the PRCM.
 - The ARM Cortex-A8 processor begins executing from the boot ROM.

Figure 3-26 shows the reset switches.

Figure 3-26. Reset Switches



3.2.17 Power-On Reset Switch SW7

Switch SW7 can be used to reset the entire chip (including the test and emulation logic and the EMAC switch). PORn is also referred to as a cold reset because it must be asserted when the device goes through a power-up cycle. Table 3-18 provides the two settings and results of the cold-reset push button.

Table 3-18. Cold-Reset Push-Button

Setting	Result
Open	Normal operating condition. Open = logical 1 state
Push button closed	Active low power-on reset. Closed = logical 0 state

The following sequence must be followed during a power-on reset (POR):

1. Wait for the power supplies to reach normal operating conditions while keeping the POR pin asserted (low).
2. Wait for input clock sources DEV_CLKIN, AUX_CLKIN, and SERDES_CLKN/P to be stable (if used by the system) while keeping the POR pin asserted.

When the power supplies and the input clock sources are stable, go to Step 3.

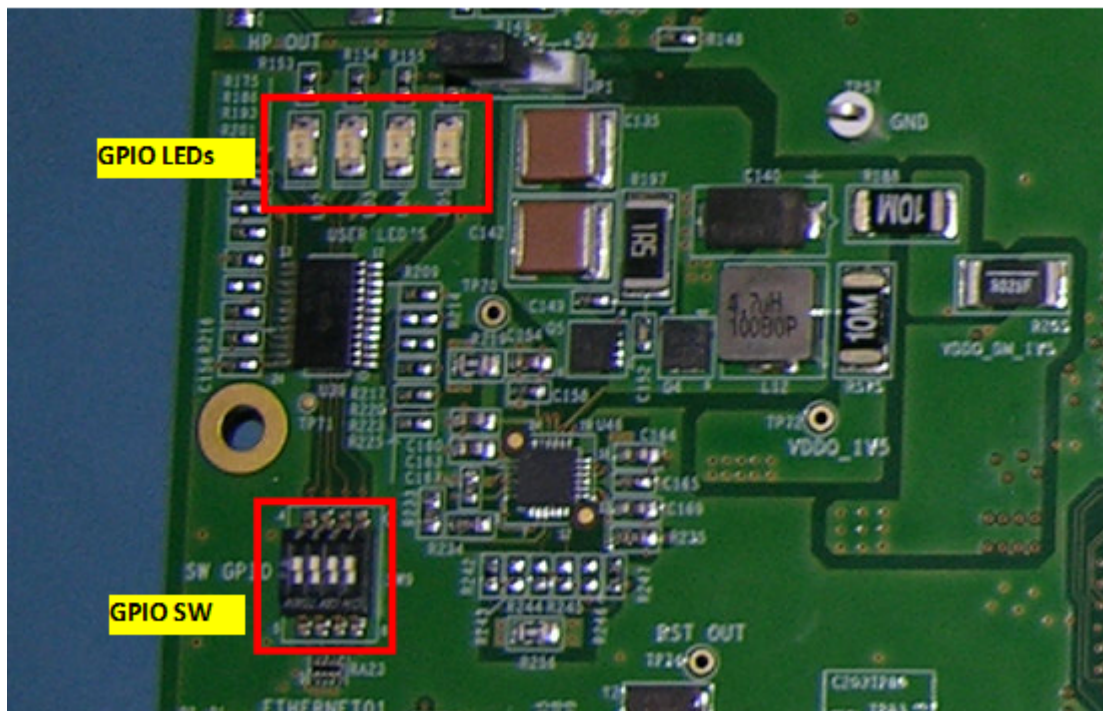
3. Ensure that the POR pin remains asserted for a minimum of two DEV clock cycles. The following things occur within the low period of the POR pin:
 - All pins (except the emulation pins) enter a Hi-Z mode and the associated pulls are enabled.
 - The PRCM asserts reset to all modules within the device.
 - The PRCM begins propagating these clocks to the chip with the PLLs in BYPASS mode.
4. Deassert (drive high) the POR pin. The followings things occur when the POR pin is deasserted:

- The BTMODE[15:0] pins are latched.
- Reset to the ARM Cortex-A8 processor and modules without a local processor is deasserted.
- If BTMODE[11] was latched as 0, then RSTOUT_WD_OUT is briefly asserted.
- The clock, reset, and power-down state of each peripheral is determined by the default settings of the PRCM.
- The ARM Cortex-A8 processor begins executing from the boot ROM.

3.2.18 GPIO Switches and LEDs

The DM388 EVM includes four LEDs and a GPIO switch (SW9) controlled by an I/O expander (PCF8575PWR [U39]) through an I2C0 interface. [Figure 3-27](#) shows the GPIO switch and LEDs.

Figure 3-27. GPIO Switch and LEDs



3.2.19 Fuses

The DM388 EVM has a fuse (F1) near switch SW1. One end of F1 is connected to a Schottky barrier rectifier and transient voltage suppressors. The other end of F1 is connected to switch SW1. The current rating of F1 is 4 A and the voltage rating is 125 VDC.

3.3 Test Points

The DM388 EVM has many test points. All test points are available on the top side of the board. [Figure 3-28](#) shows the position of each major test point.

Figure 3-28. Major Test Points

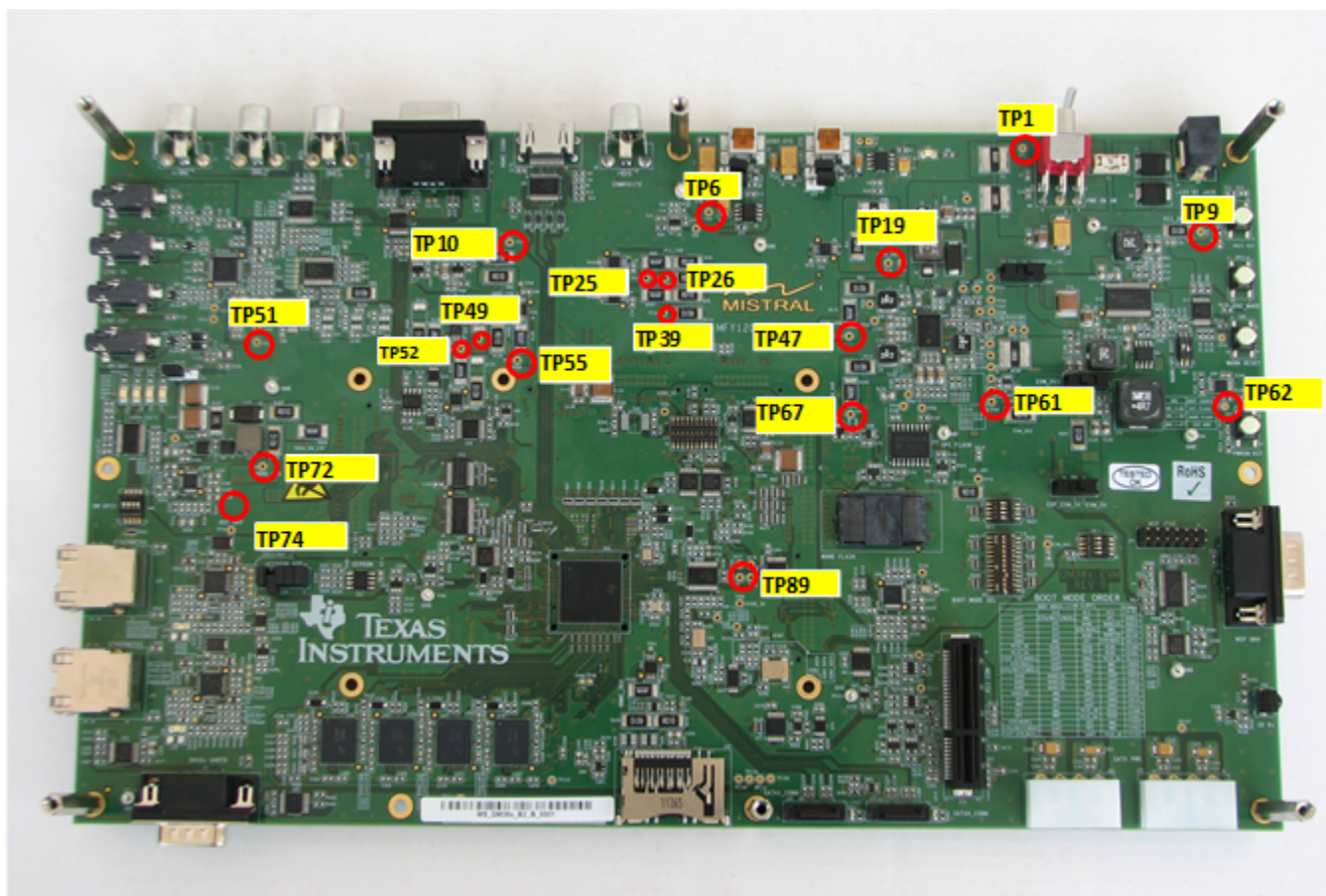


Table 3-19 lists each test point signal.

Table 3-19. Test Point Signals

Signal Number	Supply	Reference
1	IP_EVM_12V	TP1
2	EVM_5V0	TP6
3	LS_EVM_3V3	TP61
4	PCI_3V3	TP9
5	VDDQ_1V5	TP72
6	CORE_VDD	TP19
7	CVDD_ARM	TP47
8	CVDD_DSP	TP67
9	VDDA_1V8	TP49
10	PLL_1V8	TP25
11	VDDA_USB_1V8	TP39
12	VDAC_1V8	TP26
13	DVDD	TP55
14	DVDD_GPMC	TP52
15	DVDD_SD	TP89
16	EVM_1V8	TP10
17	VAIC_1V8	TP51
18	RSTOUTn	TP74
19	PORz	TP62

3.4 Expansion Connector

[Table 3-20](#) provides the pinout details of the 64-pin, board-to-board video expansion connector (J27) of the EVM.

Table 3-20. 64-Pin Video Expansion Connector (J27)

Pin Number	Pin Description	Pin Number	Pin Description
1	VIN0_DE0	2	NC
3	GND	4	GND
5	VIN0_HSYNC	6	NC
7	NC	8	NC
9	GND	10	GND
11	VIN0_VSYNC	12	NC
13	NC	14	VIN0_DE1
15	GND	16	GND
17	NC	18	NC
19	NC	20	VIN0_FLD0
21	GND	22	GND
23	NC	24	CS12_DX4
25	NC	26	CS12_DY4
27	GND	28	GND
29	NC	30	CS12_DX3
31	NC	32	CS12_DY3
33	GND	34	GND
35	SPI1_SCLK	36	CS12_DX2
37	SPI1_MISO	38	CS12_DY2
39	GND	40	GND
41	SPI1_MOSI	42	CS12_DY1
43	SPI1_nCS0	44	CS12_DX1
45	GND	46	GND
47	NC	48	CS12_DY0
49	NC	50	CS12_DX0
51	GND	52	GND
53	NC	54	NC
55	NC	56	NC
57	GND	58	GND
59	NC	60	NC
61	GND	62	GND
63	GND	64	GND

Table 3-21 provides the pinout details of the 128-pin, board-to-board video expansion connector (J28) of the EVM.

Table 3-21. 128-Pin Video Expansion Connector (J28)

Pin Number	Pin Description	Pin Number	Pin Description
1	VIN0_DE0	2	VIN0_D0
3	GND	4	GND
5	VIN0_FLD0	6	VIN0_D2
7	VIN0_CLK1	8	VIN0_D9
9	GND	10	GND
11	VIN0_D1	12	VOUT0_G_Y_YC2
13	VIN0_D4	14	VOUT0_G_Y_YC6
15	GND	16	GND
17	VIN0_D11	18	VOUT0_R_CR4
19	VIN0_D5	20	VIN0_D6
21	GND	22	GND
23	VIN0_D12	24	VIN0_D8
25	VIN0_D10	26	VIN0_D3
27	GND	28	GND
29	VIN0_D14	30	VIN0_D7
31	VIN0_D13	32	VOUT0_G_Y_YC4
33	GND	34	GND
35	VIN0_D15	36	VOUT0_B_CB_C8
37	VOUT0_CLK	38	VOUT0_G_Y_YC5
39	GND	40	GND
41	VOUT0_G_Y_YC8	42	VOUT0_B_CB_C6
43	VOUT0_G_Y_YC7	44	VOUT0_B_CB_C5
45	GND	46	GND
47	EXP_EVM_3V3	48	IP_EVM_12V
49	EXP_EVM_3V3	50	IP_EVM_12V
51	GND	52	GND
53	EXP_EVM_5V0	54	IP_EVM_12V
55	EXP_EVM_5V0	56	IP_EVM_12V
57	GND	58	GND
59	VOUT0_B_CB_C9	60	VOUT0_B_CB_C3
61	VOUT0_R_CR2	62	VOUT0_B_CB_C7
63	GND	64	GND
65	VOUT0_R_CR6	66	VOUT0_G_Y_YC3
67	VOUT0_R_CR5	68	VOUT0_G_Y_YC9
69	GND	70	GND
71	VOUT0_R_CR9	72	VIN0_CLK0
73	VOUT0_HSYNC	74	VOUT0_B_CB_C4
75	GND	76	GND
77	VIN0_D16	78	VOUT0_B_CB_C2
79	VIN0_D17	80	VOUT0_R_CR3
81	GND	82	GND
83	VIN0_D18	84	VIN0_D19
85	VOUT0_VSYNC	86	VIN0_D20
87	GND	88	GND
89	NC	90	NC

Table 3-21. 128-Pin Video Expansion Connector (J28) (continued)

Pin Number	Pin Description	Pin Number	Pin Description
91	NC	92	VIN0_D21
93	GND	94	GND
95	VOUT0_AVID	96	VIN0_D22
97	NC	98	VOUT0_R_CR7
99	GND	100	GND
101	VIN0_FLD1	102	VOUT0_R_CR8
103	USB1_CE	104	VIN0_D23
105	GND	106	GND
107	NC	108	NC
109	NC	110	USB0_CE
111	GND	112	GND
113	PM_I2C_SCL	114	NC
115	PM_I2C_SDA	116	NC
117	GND	118	GND
119	NC	120	NC
121	GND	122	GND
123	GND	124	GND
125	GND	126	GND
127	GND	128	GND

Table 3-22 provides the pinout details of the 128-pin board-to-board GPMC expansion connector (J19).

Table 3-22. 128-Pin GPMC Expansion Connector (J19)

Pin Number	Pin Description	Pin Number	Pin Description
1	McA5_AXR0_EXO	2	PM_I2C_SCL
3	GND	4	GND
5	GPMC_nCS3	6	PM_I2C_SDA
7	EXP_GPMC_nCS0	8	OSC_WAKE
9	GND	10	GND
11	GPMC_nCS2	12	GPMC_A22
13	GPMC_nCS1	14	GPMC_A23
15	GND	16	GND
17	GPMC_WEN	18	GPMC_nCS4
19	McA5_AXR1	20	VOUT1_R_CR0
21	GND	22	GND
23	GPMC_OEN_REN	24	VOUT1_R_CR1
25	GPMC_nBE1	26	MMC2_DAT1
27	GND	28	GND
29	VOUT1_G_Y_YC1	30	MMC2_DAT2
31	MMC2_DAT0	32	MMC2_DAT3
33	GND	34	GND
35	VOUT1_B_CB_C1	36	VOUT1_B_CB_C2
37	VOUT1_B_CB_C0	38	MMC2_CLK
39	GND	40	GND
41	VOUT1_FLD_EXP	42	GPMC_WAIT0
43	GPMC_D0	44	McA5_AFSX_EXP
45	GND	46	GND

Table 3-22. 128-Pin GPMC Expansion Connector (J19) (continued)

Pin Number	Pin Description	Pin Number	Pin Description
47	EXP_EVM_3V3	48	IP_EVM_12V
49	EXP_EVM_3V3	50	IP_EVM_12V
51	GND	52	GND
53	EXP_EVM_5V0	54	IP_EVM_12V
55	EXP_EVM_5V0	56	IP_EVM_12V
57	GND	58	GND
59	GPMC_D2	60	VOUT1_G_Y_YC0
61	GPMC_D5	62	GPMC_nBE0_YC0
63	GND	64	GND
65	GPMC_D7	66	GPMC_D4
67	GPMC_D9	68	GPMC_D3
69	GND	70	GND
71	GPMC_D12	72	GPMC_D1
73	GPMC_D11	74	McA5_ACLKX
75	GND	76	GND
77	GPMC_D10	78	GPMC_nADV_ALE
79	GPMC_CLK	80	GPMC_D6
81	GND	82	GND
83	GPMC_D15	84	GPMC_D8
85	NC	86	GPMC_D13
87	GND	88	GND
89	NC	90	NC
91	AUXOSC_MXI	92	NC
93	GND	94	GND
95	NC	96	MMC0_DAT0
97	UART2_CTSn_EXP	98	MMC0_DAT1
99	GND	100	GND
101	SPI0_nCS0	102	GPMC_D14
103	SPI0_SCLK	104	MMC0_DAT2
105	GND	106	GND
107	GPMC_A21	108	SPI0_MOSI
109	SPI0_nCS1	110	SPI0_MISO
111	GND	112	GND
113	MMC0_CLK	114	DCAN0/UART2_RX
115	MMC0_CMD	116	MMC0_DAT3
117	GND	118	GND
119	EXP_UART0_RXD	120	DCAN0/UART2_TX
121	GND	122	GND
123	GND	124	GND
125	GND	126	GND
127	GND	128	GND

Table 3-23 shows the pinout details of the 128-pin board-to-board MCASP expansion connector (J30).

Table 3-23. 128-Pin MCASP Expansion Connector

Pin Number	Pin Description	Pin Number	Pin Description
1	PM_I2C_SCL	2	I2C2_SDA/UART2_TXD_EXP
3	GND	4	GND
5	PM_I2C_SDA	6	I2C2_SCL/UART2_RXD_EXP
7	EXP_MCA2_AXR0	8	I2C0_SDA
9	GND	10	GND
11	MCA1_AXR2	12	I2C0_SCL
13	EXP_MCA2_AXR1	14	I2C1_SDA
15	GND	16	GND
17	MCA1_AXR3	18	I2C1_SCL
19	EXP_MCA2_ACLKX	20	MCA0_AXR3
21	GND	22	GND
23	MCA2_AXR2	24	MCA0_AXR2
25	EXP_MCA2_AFSX	26	NC
27	GND	28	GND
29	AUD_CLKIN2	30	AUD_CLKIN0
31	MCA2_AXR3	32	MCA0_AFSR
33	GND	34	GND
35	MCA1_AXR1	36	MCA0_ACLKX
37	MCA1_AXR0	38	MCA0_AFSX
39	GND	40	GND
41	VOUT1_G_Y_YC8	42	MCA1_AFSX
43	VOUT1_B_CB_C9	44	MCA0_AXR1
45	GND	46	GND
47	EXP_EVM_3V3	48	IP_EVM_12V
49	EXP_EVM_3V3	50	IP_EVM_12V
51	GND	52	GND
53	EXP_EVM_5V0	54	IP_EVM_12V
55	EXP_EVM_5V0	56	IP_EVM_12V
57	GND	58	GND
59	AUD_CLKIN1	60	VOUT1_G_Y_YC4
61	MDIO_MDIO	62	MCA0_AXR5
63	GND	64	GND
65	MDIO_MDCLK	66	MCA0_AXR4
67	MCA1_ACLKX	68	MCA0_AXR0
69	GND	70	GND
71	COU1_B_CB_C3	72	MCA1_ACLKR
73	VOUT1_B_CB_C4	74	NC
75	GND	76	GND
77	COU1_B_CB_C6	78	MCA1_AFSR
79	VOUT1_B_CB_C5	80	VOUT1_G_Y_YC7
81	GND	82	GND
83	VOUT1_B_CB_C8	84	VOUT1_R_CR7
85	VOUT1_B_CB_C7	86	VOUT1_VSYNC
87	GND	88	GND
89	VOUT1_G_Y_YC3	90	VOUT1_R_CR8
91	VOUT1_G_Y_YC5	92	NC

Table 3-23. 128-Pin MCASP Expansion Connector (continued)

Pin Number	Pin Description	Pin Number	Pin Description
93	GND	94	GND
95	VOUT1_G_Y_YC6	96	MCA0_AXR9
97	VOUT_G_Y_YC9	98	VOUT1_HSYNC
99	GND	100	GND
101	VOUT1_R_CR4	102	NC
103	VOUT1_R_CR6	104	MCA0_ACLKR
105	GND	106	GND
107	VOUT1_R_CR5	108	NC
109	VOUT1_CLK	110	NC
111	GND	112	GND
113	VOUT1_R_CR9	114	VOUT1_AVID
115	NC	116	NC
117	GND	118	GND
119	NC	120	NC
121	GND	122	GND
123	GND	124	GND
125	GND	126	GND
127	GND	128	GND

Table 3-24 shows the pinout details of the 64-pin board-to-board GPMC expansion connector (J31).

Table 3-24. 64-Pin GPMC Expansion Connector

Pin Number	Pin Description	Pin Number	Pin Description
1	VOUT1_R_CR3	2	MCA3_ACLKX
3	GND	4	GND
5	EXP_UART0_TXD	6	GPMC_A20
7	MCA3_AXR0	8	GPMC_A18
9	GND	10	GND
11	VOUT1_R_CR2	12	GPMC_A19
13	MCA3_AXR1	14	GPMC_A17
15	GND	16	GND
17	MMC2_DAT7	18	MMC2_DAT5
19	MMC2_DAT6	20	VOUT1_G_Y_YC2
21	GND	22	GND
23	VOUT0_FLD_EXP	24	MCA3_AXR2
25	IO_EXP2_GP3	26	MCA3_AXR3
27	GND	28	GND
29	CLK32OUT	30	MCA3_AFSX
31	MCA4_ACLKX	32	EXP_UART0_CTSn
33	GND	34	GND
35	NC	36	EXP_UART0_RTSn
37	NC	38	GPMC_A16
39	GND	40	GND
41	NC	42	UART2_RTSn_EXP
43	NC	44	RSTOUTn
45	GND	46	GND
47	NC	48	IO_EXP2_GP1

Table 3-24. 64-Pin GPMC Expansion Connector (continued)

Pin Number	Pin Description	Pin Number	Pin Description
49	GPIO_VS_1	50	IO_EXP2_GP2
51	GND	52	GND
53	MCA4_AXR0	54	MCA4_AXR1
55	EXP_WARM_RESET	56	MCA4_AFSX
57	GND	58	GND
59	APP_PORz	60	MMC2_DAT4
61	GND	62	GND
63	GND	64	GND

Schematics

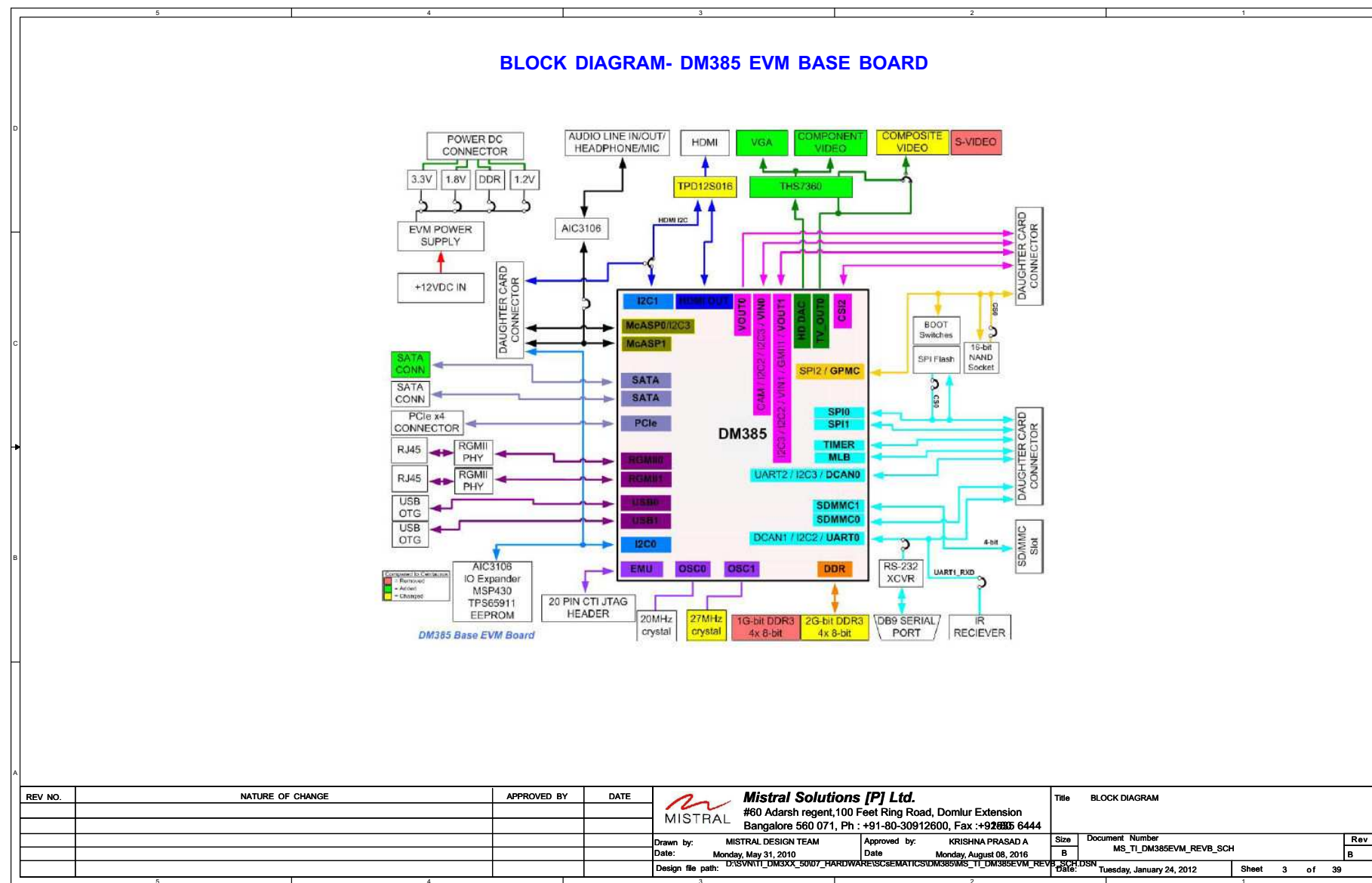
[Figure A-1](#) through [Figure A-38](#) show the schematics of the DM385 device.

Figure A-1. Version History

VERSION HISTORY					
VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	02/01/2012	SCHEMATICS "MS_TI_DM385EVM_REVA_SCH(VERSION 1.06)" IS TAKEN AS REFERENCE AND CHANGES ARE MADE FOR REV8 AS LISTED BELOW	MISTRAL DESIGN TEAM	MANJUNATHA BM	KRISHNA PRASAD A
0.02	14/01/2012	1) MIC94060YC6 (U27 & U70) ICs ARE REPLACED WITH MIC94062YC6. 2) THE ESD PROTECTION ICs TPD2E007DCKR (U95,U96,U97) IS ADDED NEAR THE LINE-IN,LINE-OUT & HP-OUT JACK. 3) THE ESD PROTECTION ICs ESDALC6V1P6 (D12 & D13) IS ADDED ALONG THE MMC CONNECTOR LINES. 4) SWITCH IC SN74CB3Q3257PWR (U98) IS ADDED FOR GPIC ADDRESS PIN MUXING. TP71 REMOVED 5) A DECOUPLING CAPACITOR(C688) IS INCLUDED ON PIN B7(HDDDA_VREF) IN TMS320DM385. 6) NAME OF PIN B7 IN TMS320DM385 IS CORRECTED AS HDDMC_VREF FROM HDDDA_VREF. 7) R273 IS MADE IN TO DNI. 8) R250 IS CHANGED TO 2.67K. 9) R44, R45, R46 ARE CHANGED TO 165OHM. 10) R481 IS MADE IN TO DNI AND R241 IS MADE IN TO 0 OHM. 11) A PUSH BUTTON SWITCH (SW12) IS INCLUDED FOR OSC_WAKE.	MISTRAL DESIGN TEAM	MANJUNATHA BM	KRISHNA PRASAD A
0.03	20/01/2012	1) R43 VALUE CHANGED TO 46.7K 2) R579 VALUE CHANGED TO 26.7K 3) U98 OE SIGNAL AND UNUSED INPUTS PULLED DOWN TO GND 4) ESDALC6V1P6 DEVICE(D12 & D13) DELETED AND ADDED TPD4E001(U99 & U100) ON MMC LINES 5) R26 AND R43 MADE AS DNI AND R58 IS MOUNTED 6) C689, C690 AND C691 ARE ADDED FOR U70 7) C692 AND C693 ADDED FOR U27 8) C694 ADDED FOR U98 9) SWAPPED THE MMC1 SIGNALS ON U99 AND U100 FOR ROUTING CONVENIENCE	MISTRAL DESIGN TEAM	MANJUNATHA BM	KRISHNA PRASAD A
1.00	24/01/2012	1) Baseline as 1.00	MISTRAL DESIGN TEAM	MANJUNATHA BM	KRISHNA PRASAD A
1.01	07/03/2012	THE RoHS NON COMPLIANT COMPONENTS ARE REPLACED WITH THE ALTERNATIVES THAT ARE RoHS COMPLIANT: 1) T494A106M016AS (C321,C323) ARE REPLACED BY T494A106M016AT. 2) SC06031A2212FKHFT (R64,R142,R178) ARE REPLACED BY RCD603FR-0722K1L. 3) SC04021A10K01LHF3 (R65,R89,R90,R94) ARE REPLACED BY ERJ-2GE1100X. 4) TDA04H0SK1 (SW9,SW10,SW11) ARE REPLACED BY GDH04S04.	MISTRAL DESIGN TEAM	MANJUNATHA BM	KRISHNA PRASAD A
1.02	09/05/2016	SATA INTERFACE DNI'd (J23,J24,J25,J26,U86,C310,C350,C343,C323,C351,C344,C318,C349,C334,C321,C348,C335,C683,R479,R486,R485,R482,LD10,LD11)	MISTRAL DESIGN TEAM	KRISHNA PRASAD A	KRISHNA PRASAD A

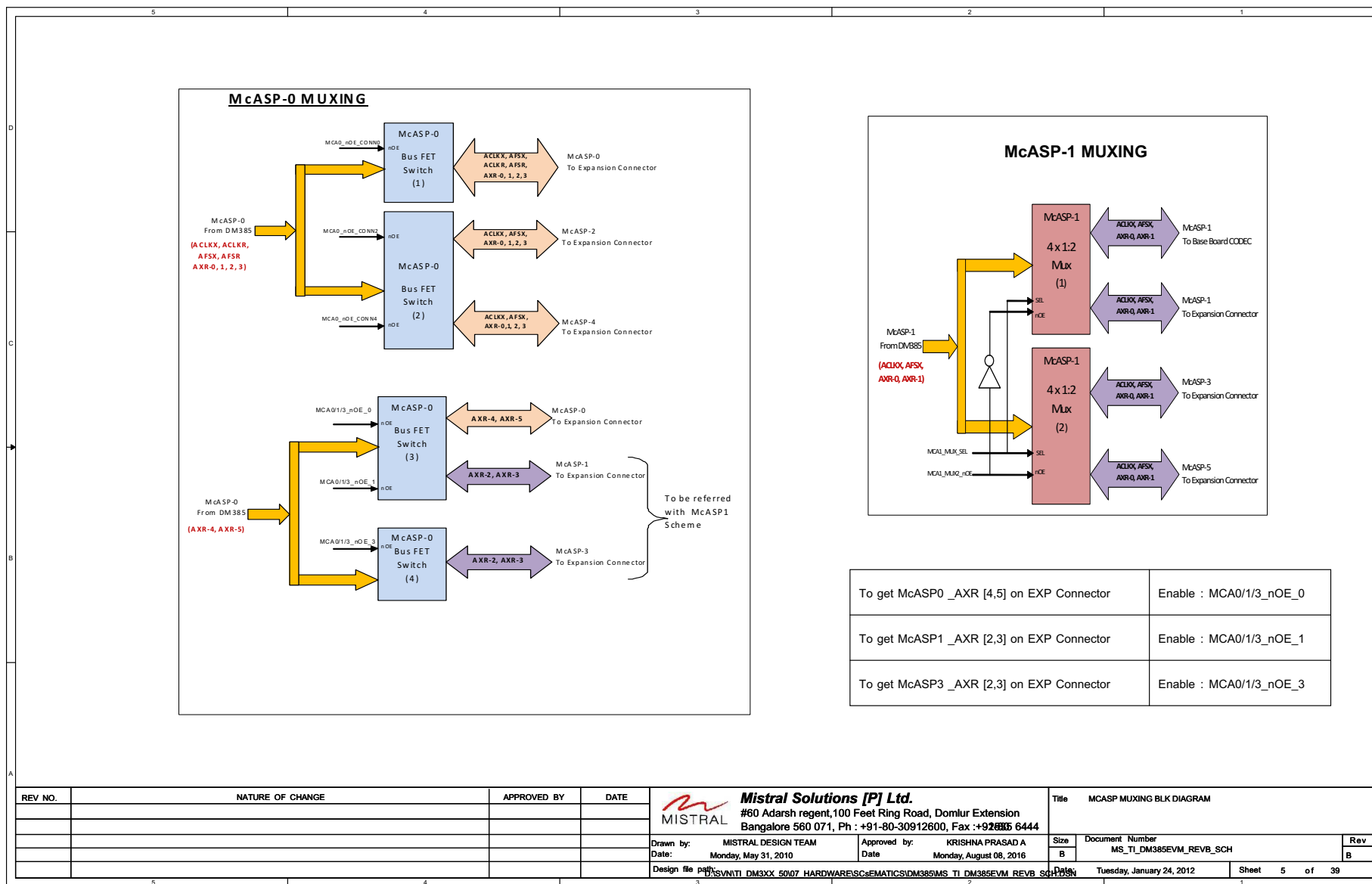
REV NO.	NATURE OF CHANGE	APPROVED BY	DATE	Mistral Solutions [P] Ltd.		Title	
				 Mistral Solutions [P] Ltd. #80 Adarsh regent,100 Feet Ring Road, Domtur Extension Bangalore 560 071, Ph: +91-90-309212600, Fax: +91-90-2635 6444		VERSION HISTORY	
				Drawn by: MISTRAL DESIGN TEAM	Approved by: KRISHNA PRASAD A	Size	Document Number
				Date: Monday, May 21, 2010	Date: Monday, August 08, 2016	C	MS_TI_DM385EVM_REVA_SCH
				Design file path: D:\SV\NTI_DM385_5007_HARDWARE\SCHEMATICS\DM385EVM_TI_DM385EVM_REVA_SCH.DGN		Date: Monday, August 08, 2016	Sheet 2 of 39

Figure A-2. DM385 Block Diagram



MEMORY MAP TO BE UPDATED					GPIO ASSIGNMENT(SAME AS CENTAURUS)					GPIO ASSIGNMENT (NEWLY ADDED)									
ETHERNET-GPMC					GPIO NAME		SOURCE	PURPOSE			GPIO NAME		SOURCE	PURPOSE					
NAND-GPMC					ENET_INT		GP1[10]	ETHERNET			ENET_WoL_INT		GP0[12]	WoL INTERRUPT					
DDR-0					PCF8575_INT_IO1		GP1[4]	I INTERRUPT			HDMI_CT_HPD		PCF8575 DEVICE -3	ENABLING LOAD SWITCH					
SPI FLASH					TPS_INT1		TPS659113-- INT 1	INTERRUPT FROM PMIC			HDMI_LS_OE		PCF8575 DEVICE -3	ENABLING LEVEL SHIFTER					
I2C DEVICES					EN_BCK2_LS		TPS659113-- GPIO 7	ENABLING LOAD SWITCH			DISABLE_SD		PCF8575 DEVICE -3	SD AND SF CHANNEL CONTROL OF VIDEO AMPLIFIER					
I2C0- AUDIO CODEC		0011000			EN_TP562350 (REMOVED)		TPS659113-- GPIO 6	ENABLING CVDD_HDVICP			DISABLE_SF		PCF8575 DEVICE -3						
I2C0- EEPROM		1010000			EN_BCK3_TPS65232		TPS659113-- GPIO 2	ENABLING PCI_3V3			BYPASS_SD		PCF8575 DEVICE -3	TO BYPASS LPF OF SD AND SF IN VA					
I2C0- PCF8575-1		0100000			EN_TPS51116		TPS659113-- GPIO 0	ENABLING DDR SUPPLY			BYPASS_SF		PCF8575 DEVICE -3						
I2C0- PCF8575-2		0100011			MSP430_INT		PCF8575 DEVICE-1	INTERRUPT FOR MSP430			FILTER1		PCF8575 DEVICE -3	SELECTABLE FILTER FOR SF CHANNELS					
I2C1- HDMI					EXP_ETH_RESET		PCF8575 DEVICE-1	ETHERNET RESET			FILTER1		PCF8575 DEVICE -3						
I2C2- PCF8575-3		0100000			TPS_SLEEP		PCF8575 DEVICE-1	SLEEP FOR TPS659113			IO_EXP2_GP1		PCF8575 DEVICE -2	GPIO USED IN CATLOG					
PMI2C					PCI_SW_RESETn		PCF8575 DEVICE-1	PCI RESET			IO_EXP2_GP2		PCF8575 DEVICE -2	GPIO USED IN CATLOG					
I2C POWER MONITORS--MSP430					IR_REMOTE_OFF		PCF8575 DEVICE-1	IR SENSOR CONTROLLING			MCA0_DEC_A MCA0_DEC_B		PCF8575 DEVICE -2	MCA5P0 DECODER SELECT LINES					
PM_I2C ADDRESS					UART0_OFF		PCF8575 DEVICE-1	UART-0 CONTROLLING			MCA1_MUX_SEL		PCF8575 DEVICE -2	MCA5P1 MUX SELECT LINES					
PLL_1V8		1000000			GPMC_ADD_SELn		PCF8575 DEVICE-1	TO SELECT EITHER GPMC OR HDMI LINES.			MCA0/I13_RSEL_A MCA0/I13_RSEL_B		PCF8575 DEVICE -2	MCA5P0/I13 R DECODER SELECT LINES					
HDMI_CSI_1V8		1000001			SW_VOUT_EN		TDAA04H0SK1 DEVICE	VIDEO SW ENABLE			PCF8575_INT_IO2		GP0[13]	INTERRUPT					
CVDD_ARM		1000010			GPMC_nWP		TDAA04H0SK1 DEVICE	GPMC WRITE PROTECT			MCA0_AXR9		PCF8575 DEVICE -2	GPIO USED IN VC BOARD					
VDDQ_DM_1V5		1000011			RESET_GPIO		TDAA04H0SK1 DEVICE	ENABLING PCI POR BUFFER			IO_EXP2_GP3		PCF8575 DEVICE -2	GPIO USED IN VC BOARD					
VDDA_1V8		1000101																	
DVDD_GPMC		1000110																	
CVDD_DSP		1001001																	
CORE_VDD		1001000																	

Figure A-4. McASP Muxing



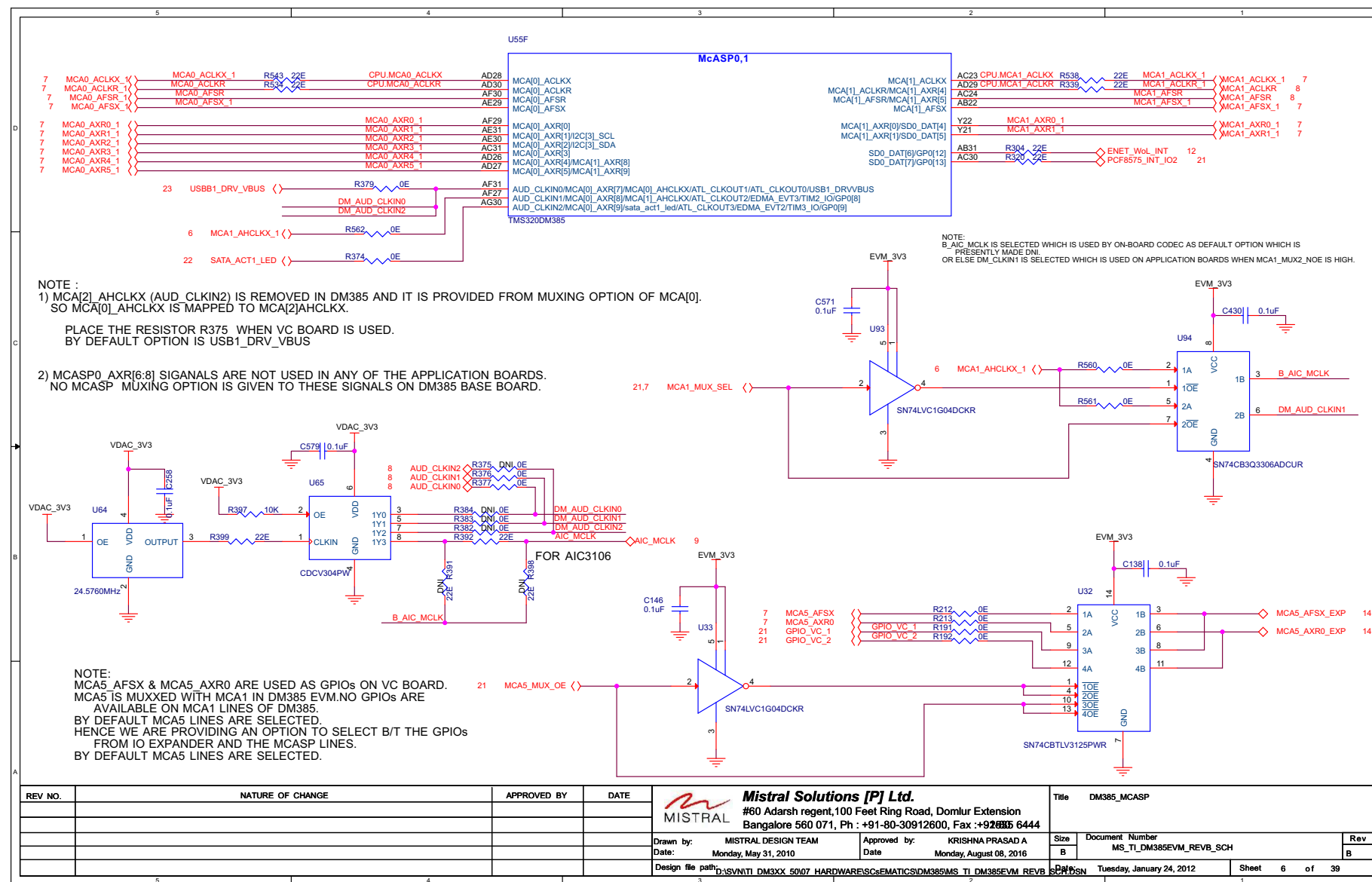


Figure A-6. McASP Muxing and Decoders

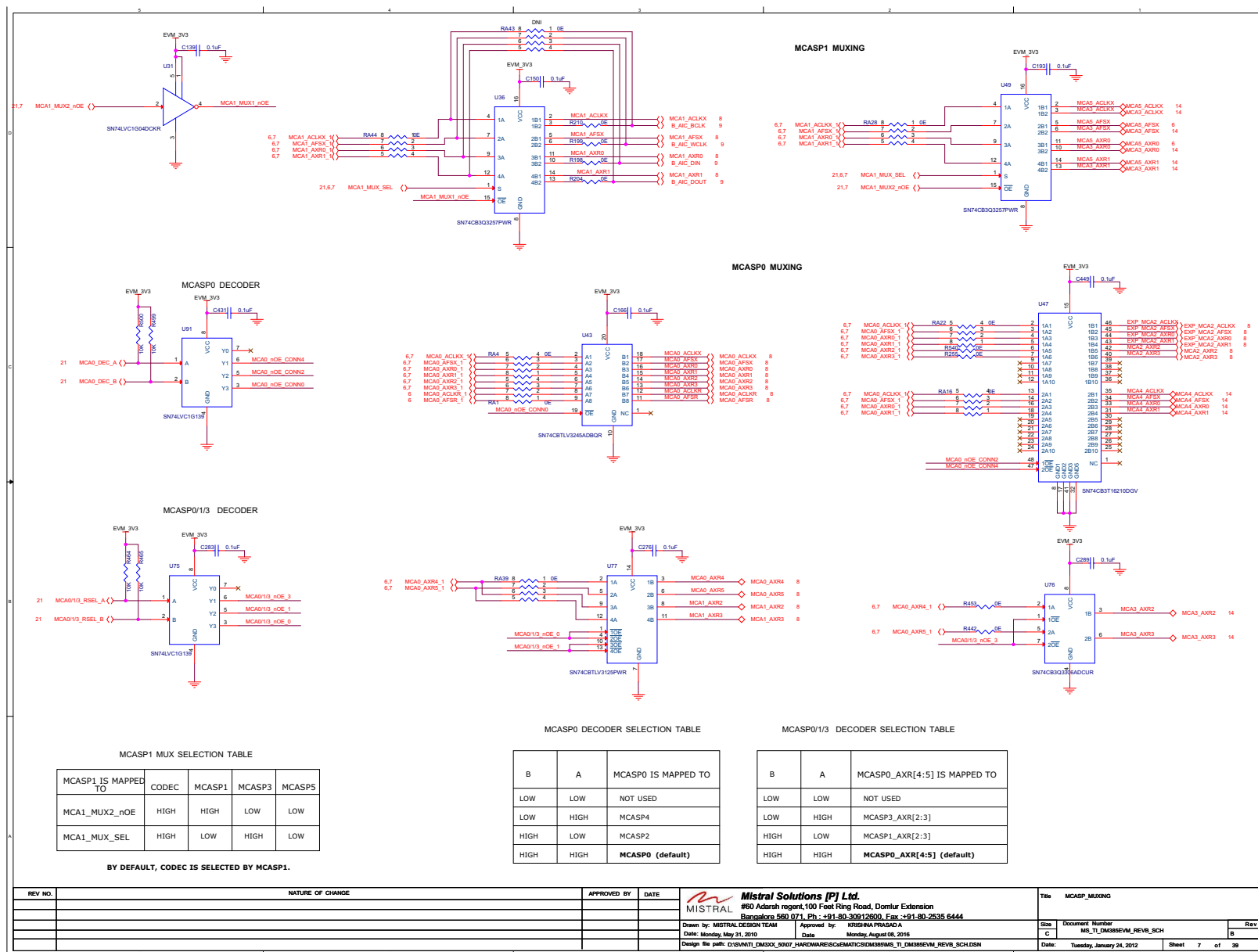
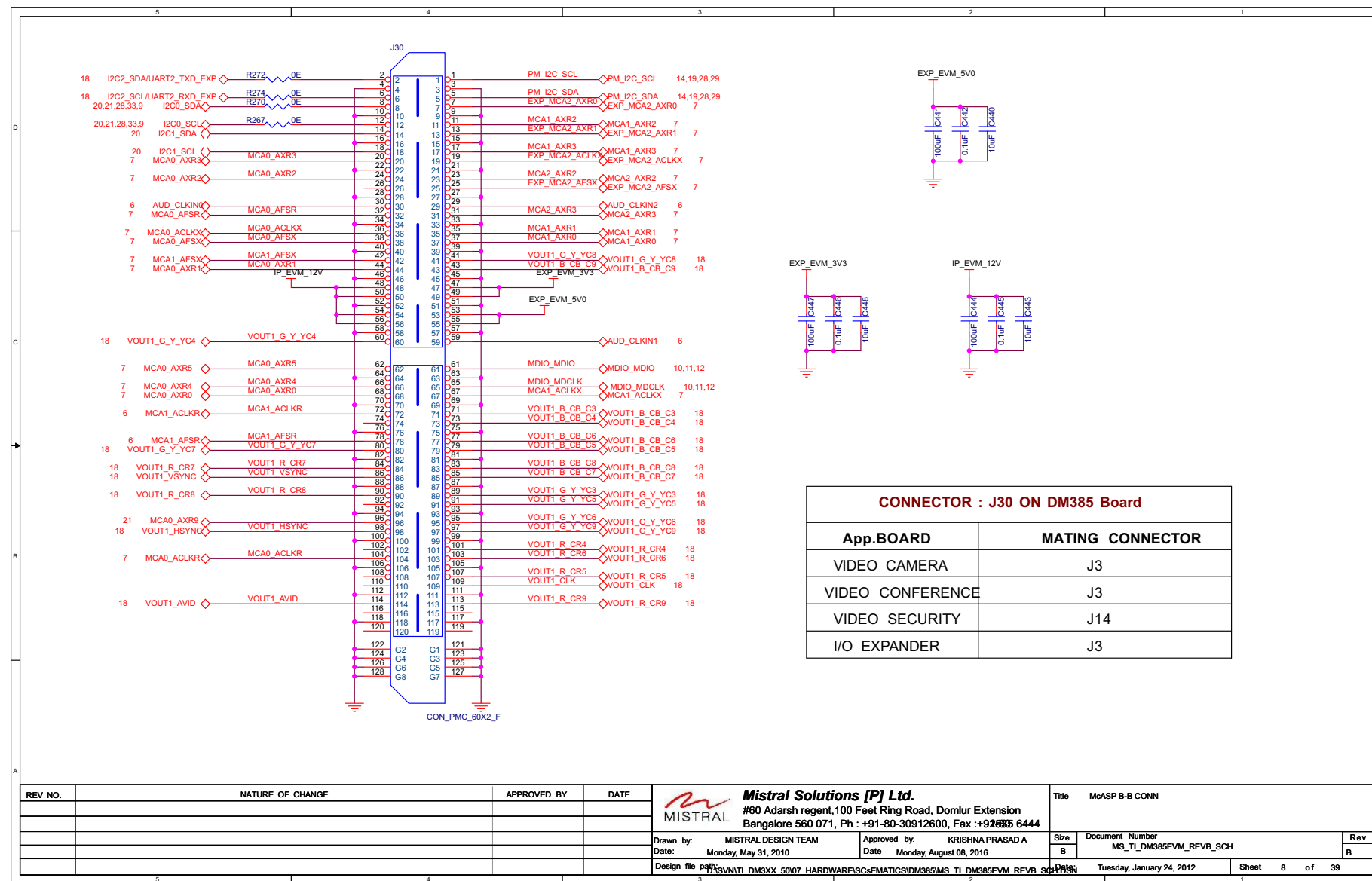


Figure A-7. McASP B-B Connection



GMII0 INTERFACE

Signals and Connections:

- RGMII0_RXC:** Connected to RGMII0_RXC (AG4), RGMII1_RXC (AL6), and RGMII1_RXD[2] (AF8).
- RGMII1_RXD[3]:** Connected to RGMII1_RXD[3] (AK6), CRGMII1_TXD[1] (AJ7), and CRGMII1_TXD[0] (AE4).
- RGMII1_TXD[0]:** Connected to RGMII1_TXD[0] (AK7), CRGMII1_TXD[2] (AK8), and RGMII1_TXC (R548).
- RGMII1_TXC:** Connected to RGMII1_TXC (R548), RGMII1_RXD[0] (AH8), and CRGMII1_TXD[3] (AG8).
- MDIO_MDI_O:** Connected to MDIO_MDI_O (R329), MDIO_MDI_O (R334), and MDIO_MDI_O (AG2).
- MDIO_MDI_O:** Connected to MDIO_MDI_O (R329), MDIO_MDI_O (R334), and MDIO_MDI_O (AG3).

Internal Connections:

- EMAC[0]:** Connected to EMAC[0]_MTCLK/VIN[1]B_D[0] (SPI[3]_SCS[3]nI2C[2]_SDA/GP3[23]/RGMII0_RXC), EMAC[0]_GMTCLK/GPMC_A[6] (SPI[2]_D[1]/RGMII1_RXC), EMAC[0]_MTXEN/EMAC[1]_RMTXEN/GPMC_A[15] (UART1_RTn/RGMII1_RXD[2]), EMAC[0]_MRXD[0]/VIN[1]B_D[5] (EMAC[0]_RMTXD[0]/GP3[28]/RGMII0_TXD[0]), EMAC[0]_MRXD[1]/VIN[1]B_D[6] (EMAC[0]_RMTXD[1]/GP3[29]/RGMII0_RXD[0]), EMAC[0]_MRXD[2]/VIN[1]B_D[7] (EMAC[0]_RMTXEN/GP3[30]/RGMII0_RXD[1]), EMAC[0]_MRXD[3]/GPMC_A[27] (GPMC_A[26]/GPMC_A[0]/RGMII1_RXCTL), EMAC[0]_MRXD[4]/GPMC_A[1] (RGMII0_RXD[3]), EMAC[0]_MRXD[5]/GPMC_A[2] (RGMII0_TXD[3]), EMAC[0]_MRXD[6]/GPMC_A[3] (RGMII0_TXD[2]), EMAC[0]_MRXD[7]/GPMC_A[4] (SPI[2]_SCS[3]n/RGMII0_TXD[1]), EMAC[0]_MRXD[0]/GPMC_A[5] (SPI[2]_CLK/RGMII1_RXD[1]), EMAC[0]_MRXD[1]/B_D[3] (EMAC[0]_RMRXR/GP3[26]/RGMII0_TXCTL), EMAC[0]_MRXD[2]/GPMC_A[12] (UART1_RXD/RGMII1_TXC), EMAC[0]_MRXD[3]/GPMC_A[13] (UART1_TXD/RGMII1_RXD[0]), EMAC[0]_MRXD[4]/GPMC_A[14] (UART1_CTn/RGMII1_TXD[0]), EMAC[0]_MRXD[5]/GPMC_A[15] (UART1_CTn/RGMII1_TXD[0]), EMAC[0]_MRXD[6]/GPMC_A[16] (UART1_CTn/RGMII1_TXD[0]), EMAC[0]_MRXD[7]/GPMC_A[17] (UART1_CTn/RGMII1_TXD[0]).

Summary Table:

Signal	Internal Connection	Pin
RGMII0_RXC	EMAC[0]_MTCLK/VIN[1]B_D[0] (SPI[3]_SCS[3]nI2C[2]_SDA/GP3[23]/RGMII0_RXC)	AG4
RGMII1_RXC	EMAC[0]_GMTCLK/GPMC_A[6] (SPI[2]_D[1]/RGMII1_RXC)	AL6
RGMII1_RXD[2]	EMAC[0]_MTXEN/EMAC[1]_RMTXEN/GPMC_A[15] (UART1_RTn/RGMII1_RXD[2])	AF8
RGMII1_RXD[3]	EMAC[0]_MRXD[0]/VIN[1]B_D[5] (EMAC[0]_RMTXD[0]/GP3[28]/RGMII0_TXD[0])	AK6
CRGMII1_TXD[1]	EMAC[0]_MRXD[1]/VIN[1]B_D[6] (EMAC[0]_RMTXD[1]/GP3[29]/RGMII0_RXD[0])	AJ7
CRGMII1_TXD[0]	EMAC[0]_MRXD[2]/VIN[1]B_D[7] (EMAC[0]_RMTXEN/GP3[30]/RGMII0_RXD[1])	AE4
RGMII1_TXD[0]	EMAC[0]_MRXD[3]/GPMC_A[27] (GPMC_A[26]/GPMC_A[0]/RGMII1_RXCTL)	AK7
RGMII1_TXC	EMAC[0]_MRXD[4]/GPMC_A[1] (RGMII0_RXD[3])	AK8
RGMII1_RXD[0]	EMAC[0]_MRXD[5]/GPMC_A[2] (RGMII0_TXD[3])	R548
CRGMII1_TXD[3]	EMAC[0]_MRXD[6]/GPMC_A[3] (RGMII0_TXD[2])	AH8
MDIO_MDI_O	EMAC[0]_MRXD[7]/GPMC_A[4] (SPI[2]_SCS[3]n/RGMII0_TXD[1])	AG2
MDIO_MDI_O	EMAC[0]_MRXD[0]/GPMC_A[5] (SPI[2]_CLK/RGMII1_RXD[1])	AG3
MDIO_MDI_O	EMAC[0]_MRXD[1]/B_D[3] (EMAC[0]_RMRXR/GP3[26]/RGMII0_TXCTL)	AG2
MDIO_MDI_O	EMAC[0]_MRXD[2]/GPMC_A[12] (UART1_RXD/RGMII1_TXC)	AG3
MDIO_MDI_O	EMAC[0]_MRXD[3]/GPMC_A[13] (UART1_TXD/RGMII1_RXD[0])	AG2
MDIO_MDI_O	EMAC[0]_MRXD[4]/GPMC_A[14] (UART1_CTn/RGMII1_TXD[0])	AG3
MDIO_MDI_O	EMAC[0]_MRXD[5]/GPMC_A[15] (UART1_CTn/RGMII1_TXD[0])	AG2
MDIO_MDI_O	EMAC[0]_MRXD[6]/GPMC_A[16] (UART1_CTn/RGMII1_TXD[0])	AG3
MDIO_MDI_O	EMAC[0]_MRXD[7]/GPMC_A[17] (UART1_CTn/RGMII1_TXD[0])	AG2

Copyright © 2016, Texas Instruments Incorporated



Figure A-11. Ethernet Controller 1

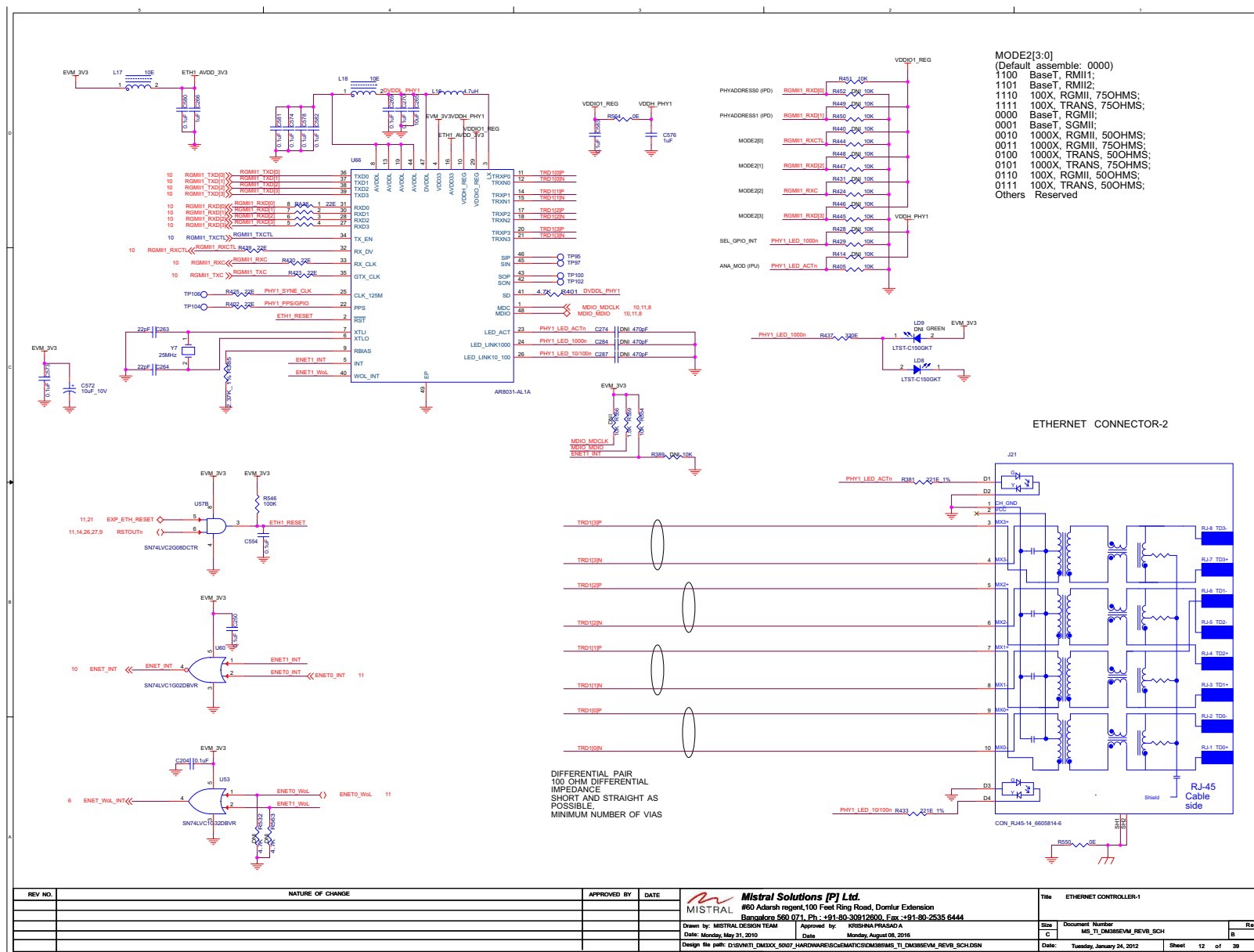
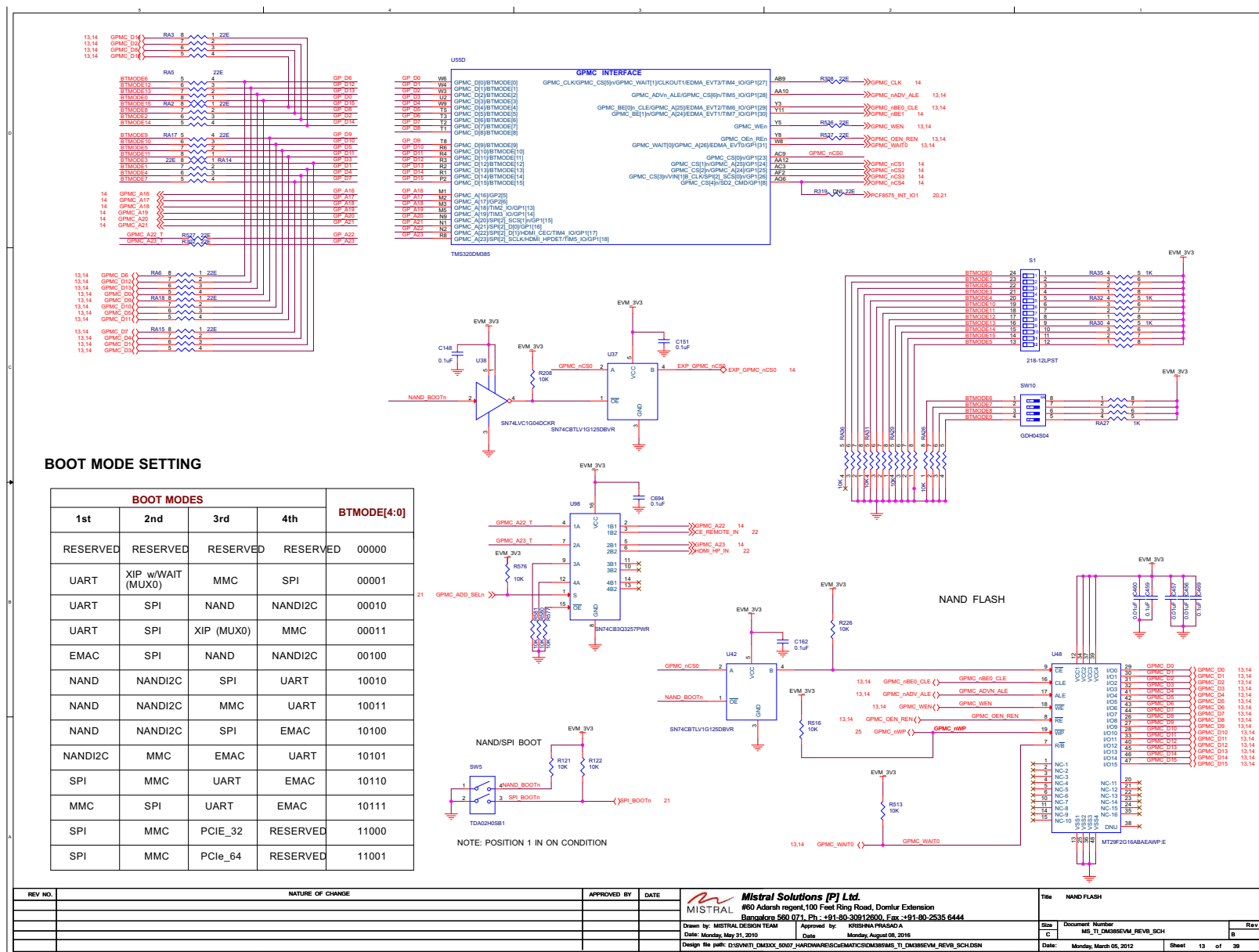


Figure A-12. NAND Flash



CONNECTOR : J29 ON DM385 Board

App.BOARD	MATING CONNECTOR
VIDEO CAMERA	J4
VIDEO CONFERENCE	J4
VIDEO SECURITY	J13
I/O EXPANDER	J4

CONNECTOR : J31 ON DM385 Board

App.BOARD	MATING CONNECTOR
VIDEO CAMERA	J5
VIDEO CONFERENCE	J5
VIDEO SECURITY	J15
I/O EXPANDER	J5

NOTE: MLB SIGNALS ARE NOT AVAILABLE IN DM385, TWO MLB SIGNALS WHICH ARE USED AS GPIOs ON THE CATLOG BOARD ARE GIVEN FROM IO EXPANDER-2

Figure A-14. DM385 MMC0, MMC1, and MMC2

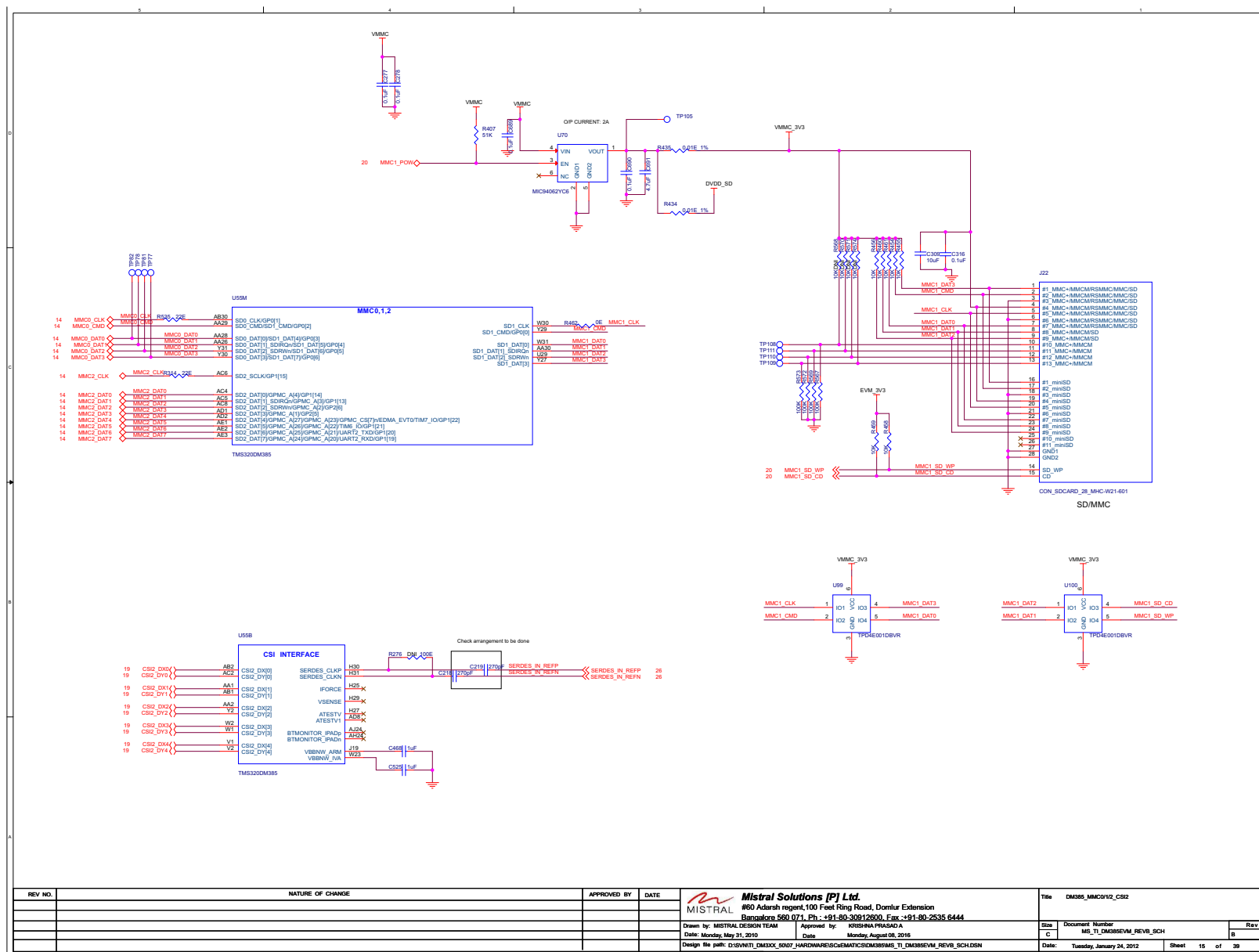


Figure A-15. DM385 DDR0 Terminations

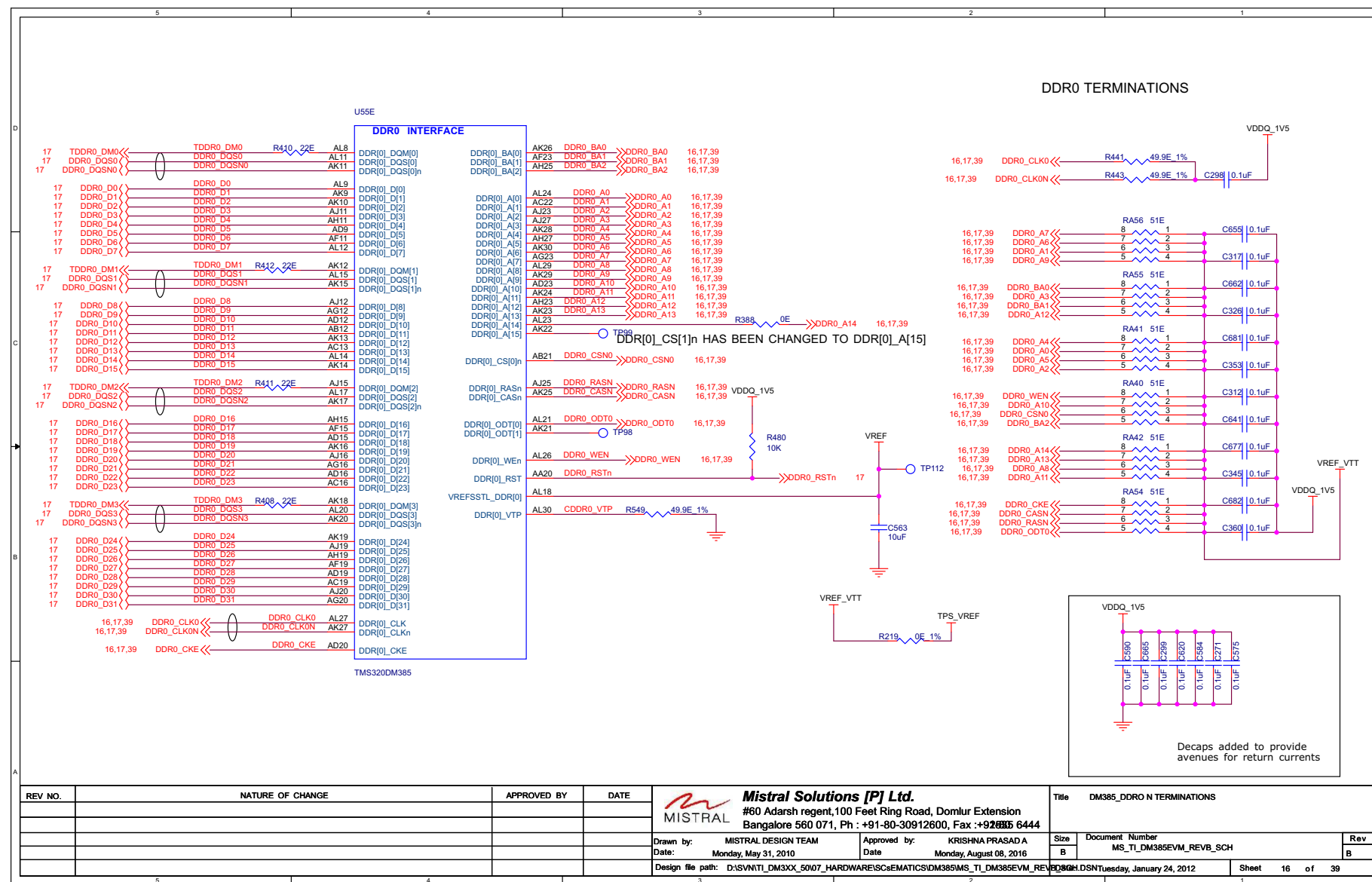


Figure A-16. DDR0-0, DDR0-1, DDR0-2, and DDR0-3

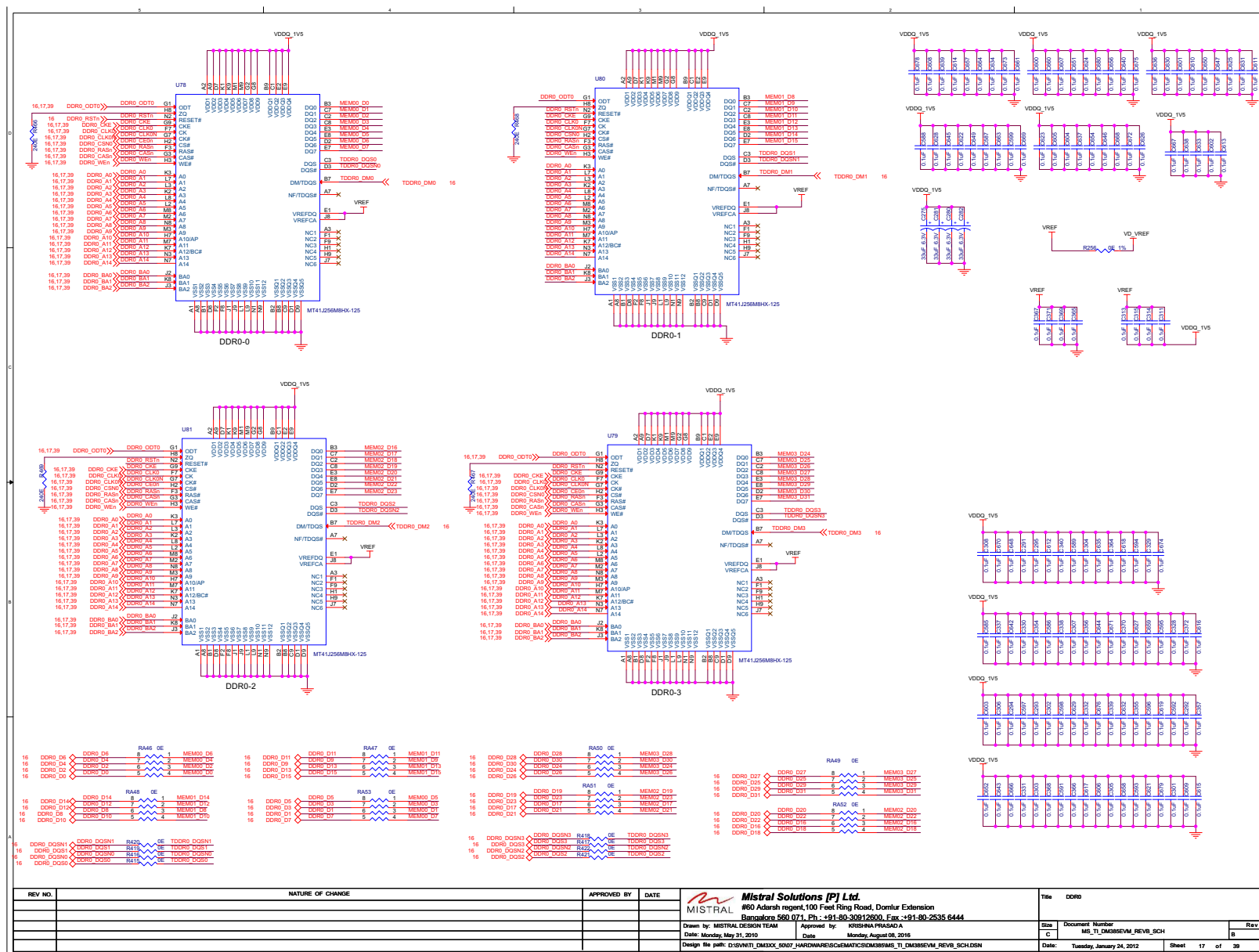


Figure A-17. DM385 VIN0, VOUT0, and VOUT1

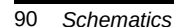


Figure A-18. Video B-B Connector

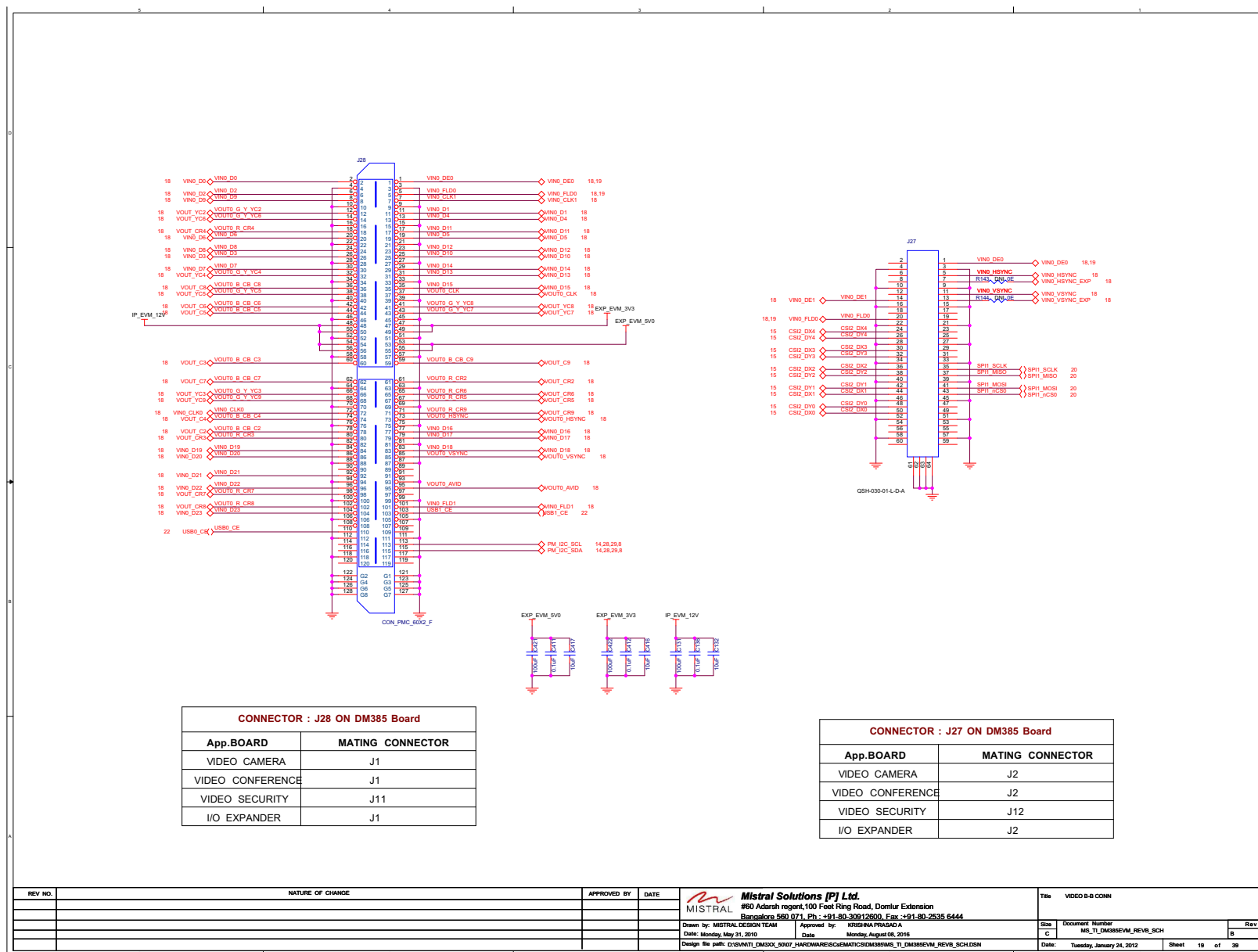


Figure A-19. DM385 Serial Interfaces

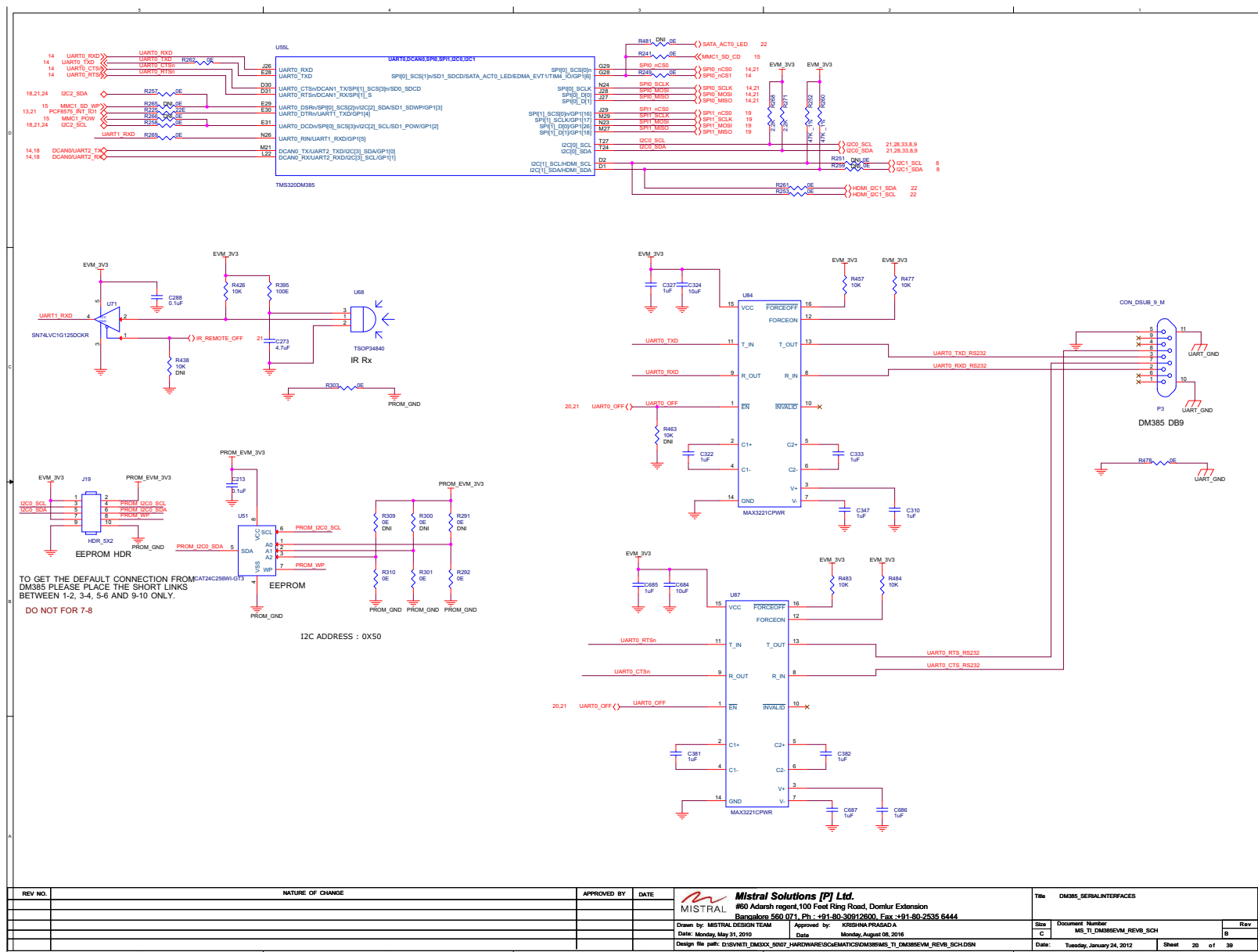


Figure A-20. SPI Flash

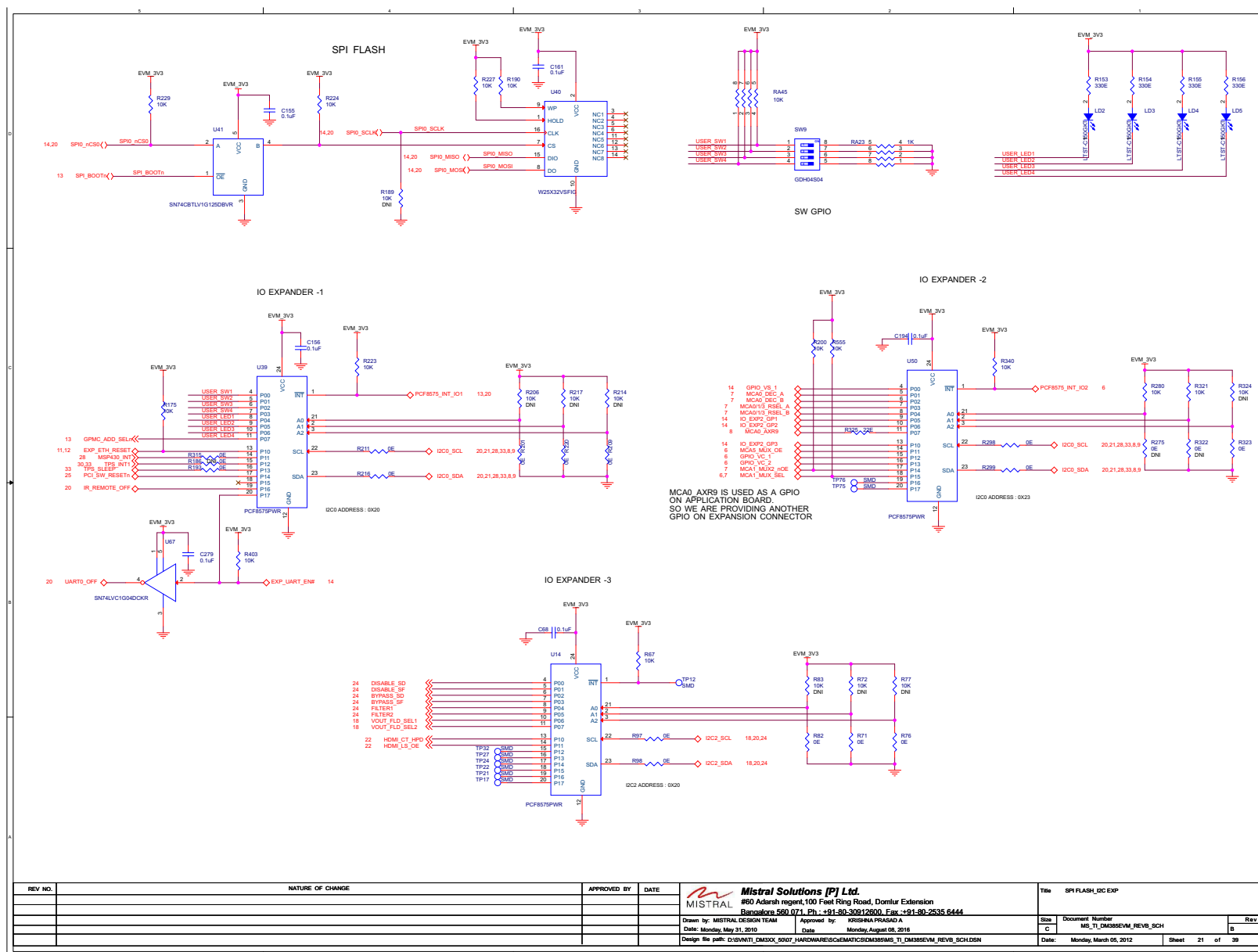


Figure A-21. DM385 HDMI, SATA, USB0, and USB1

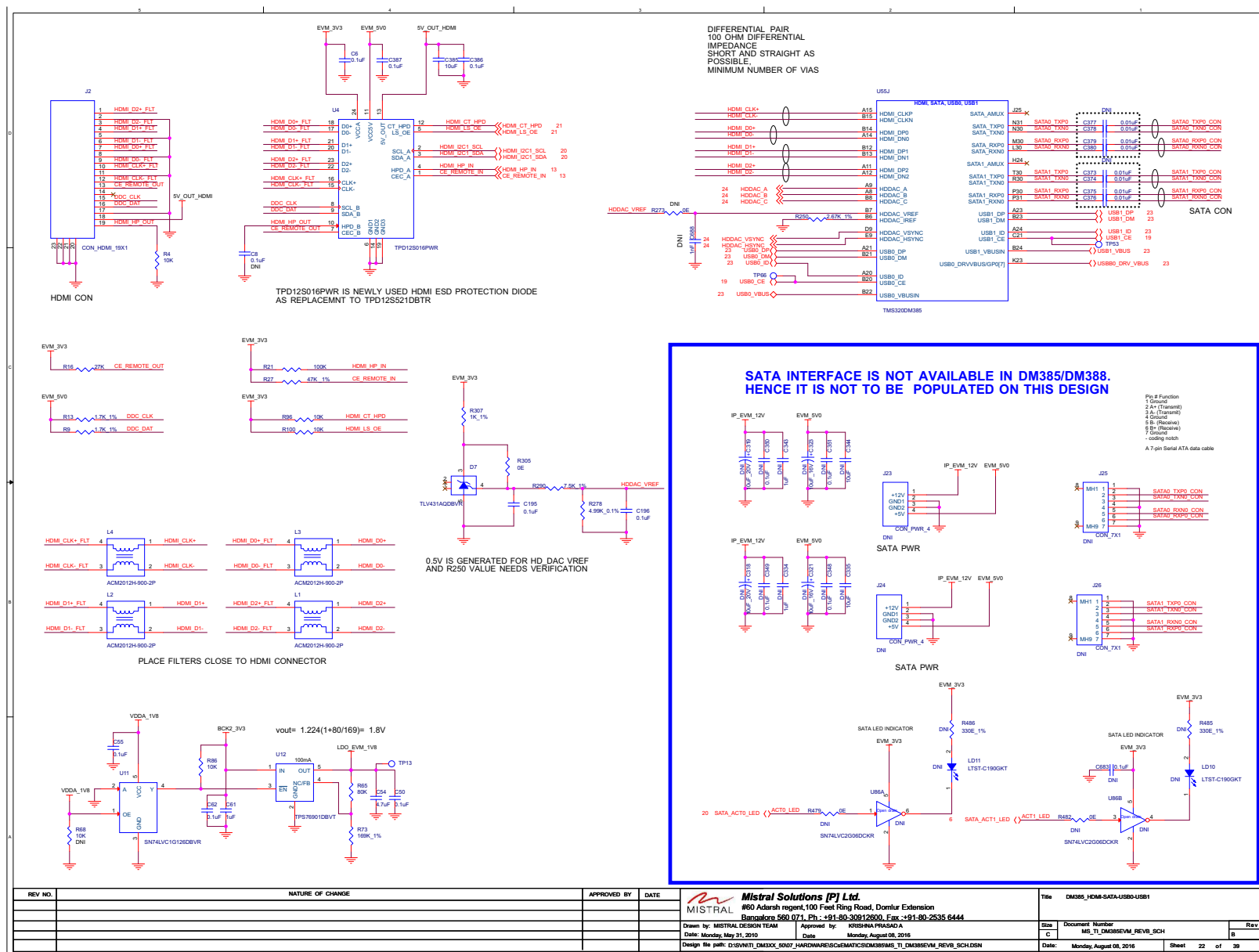
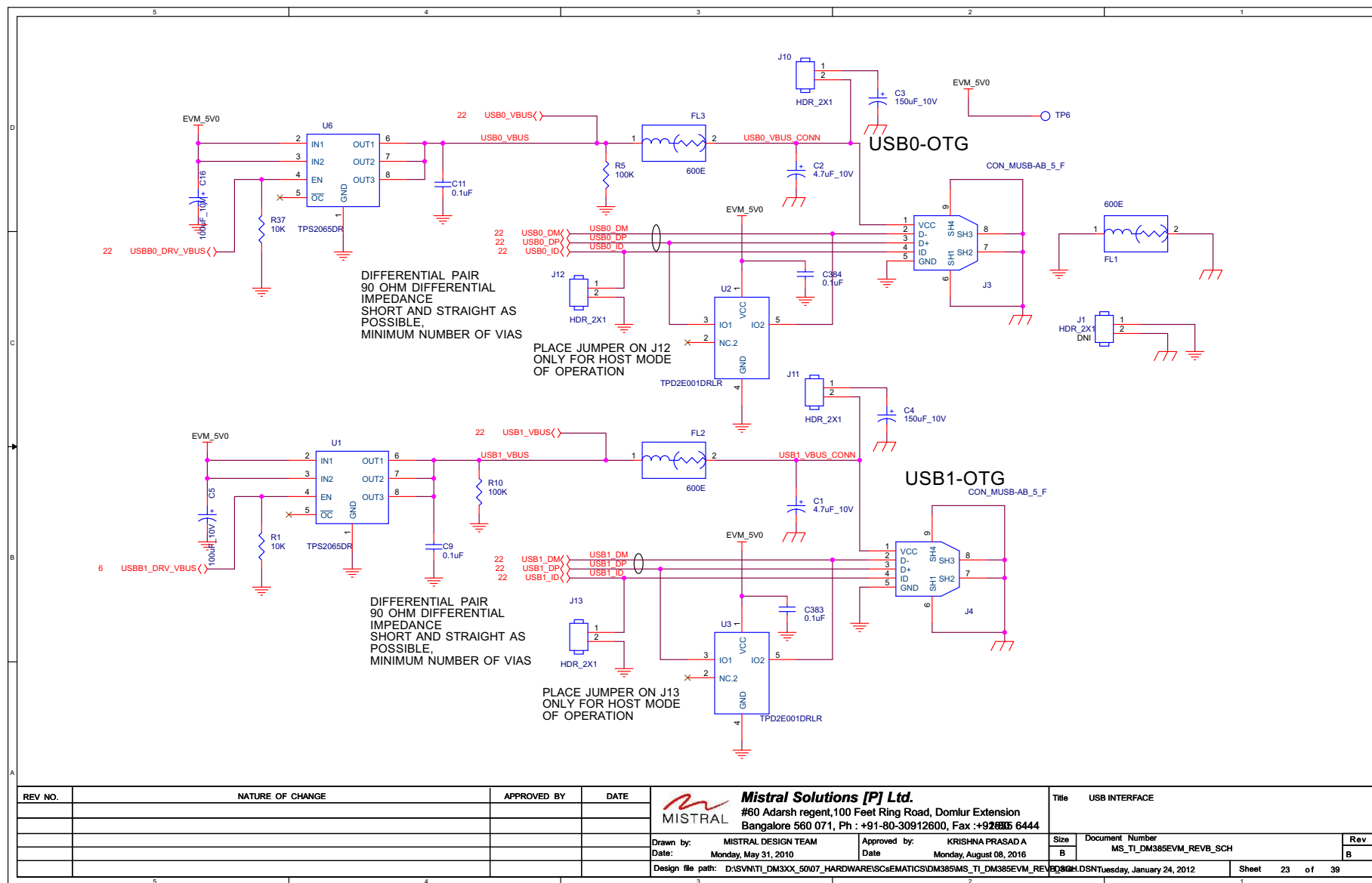


Figure A-22. USB Interface



PCIE AND JTAG

VIDEO AMPLIFIER

COMPOSITE

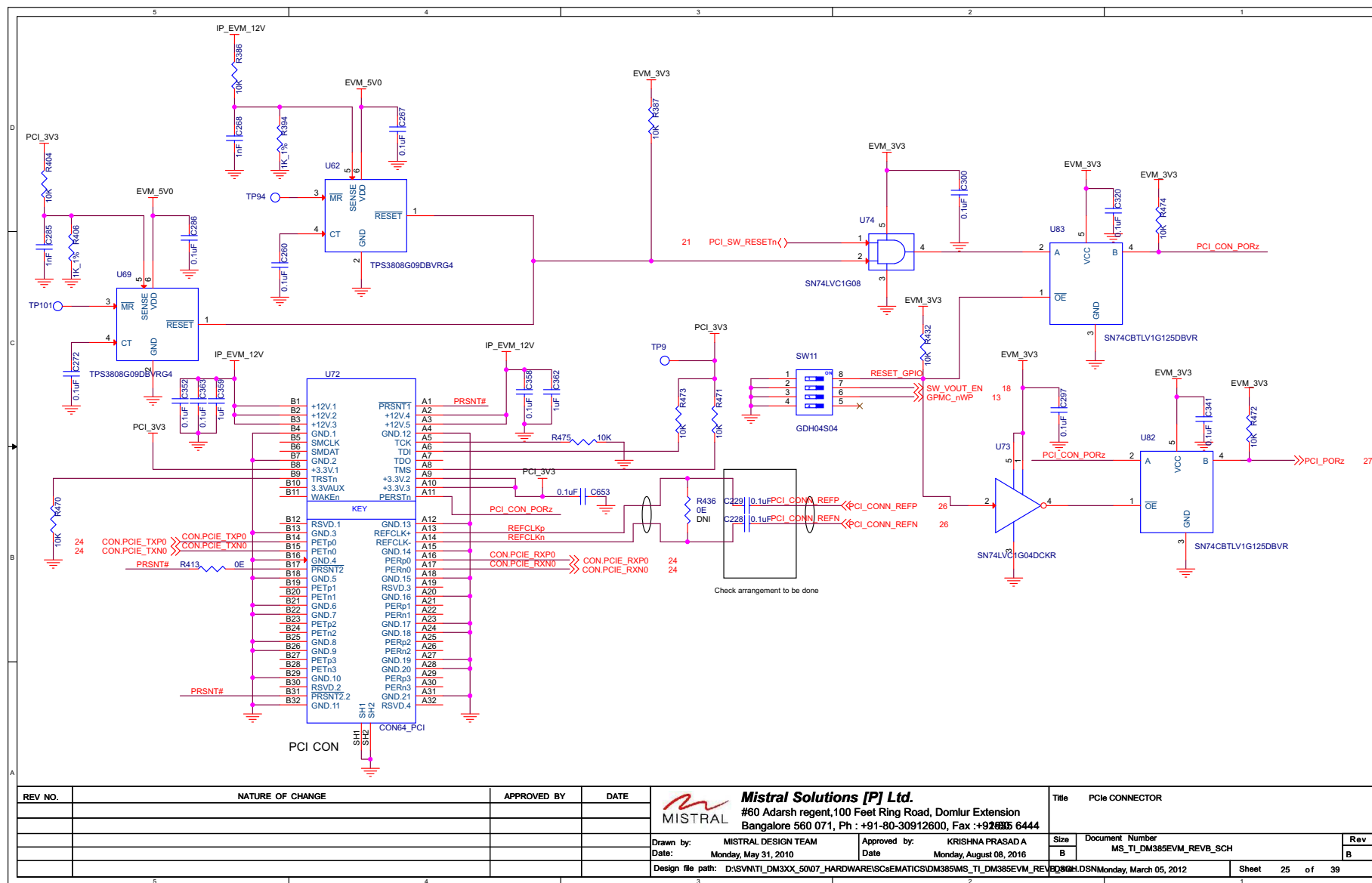
VGA

DDC

JTAG HDR

EMU0,1,2,3,4 SHOULD MATCH THE TRACE LENGTH TO REDUCE SKEW...

Figure A-24. PCIe Connector



DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

REV NO.	NATURE OF CHANGE	APPROVED BY	DATE

Mistral Solutions [P] Ltd.
 #60 Adarsh regent, 100 Feet Ring Road, Domlur Extension
 Bangalore 560 071, Ph : +91-80-30912600, Fax : +91-80-30912601

Drawn by: MISTRAL DESIGN TEAM
 Date: Monday, May 31, 2010

Approved by: KRISHNA PRASAD A
 Date: Monday, August 08, 2016

Design file path: D:\S\WTL_DM3XX_5007_HARDWARE\SCHEMATICS\DM385\MS_TL_DM385EVM_REV_B\DM385EVM_REV_B.SCH

Title: SERDES CLOCKS
 Document Number: MS_TL_DM385EVM_REV_B_SCH
 Date: Tuesday, January 24, 2012

Sheet 26 of 39

Figure A-26. DM385 Clocks

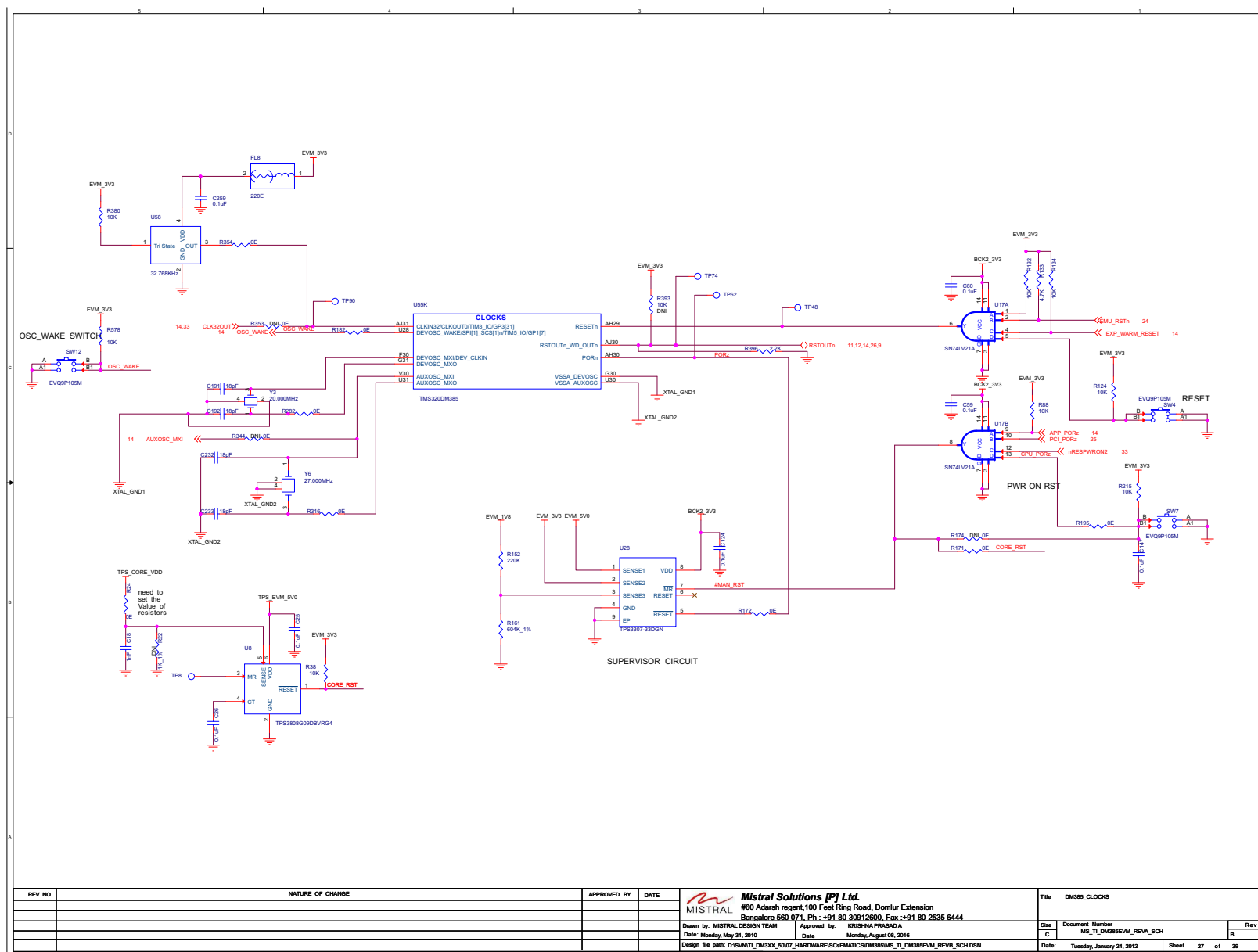


Figure A-27. Power Monitor CPU

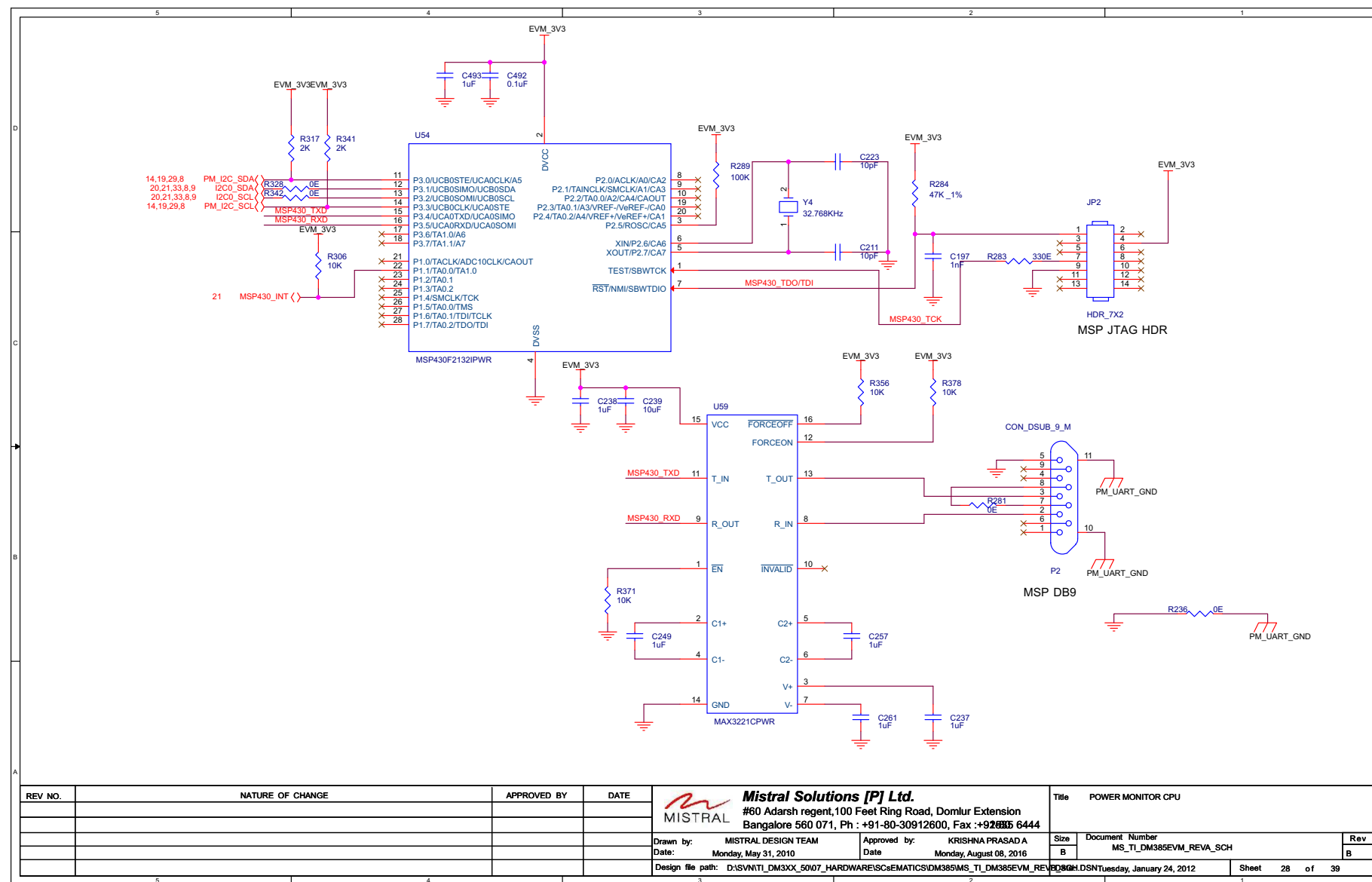
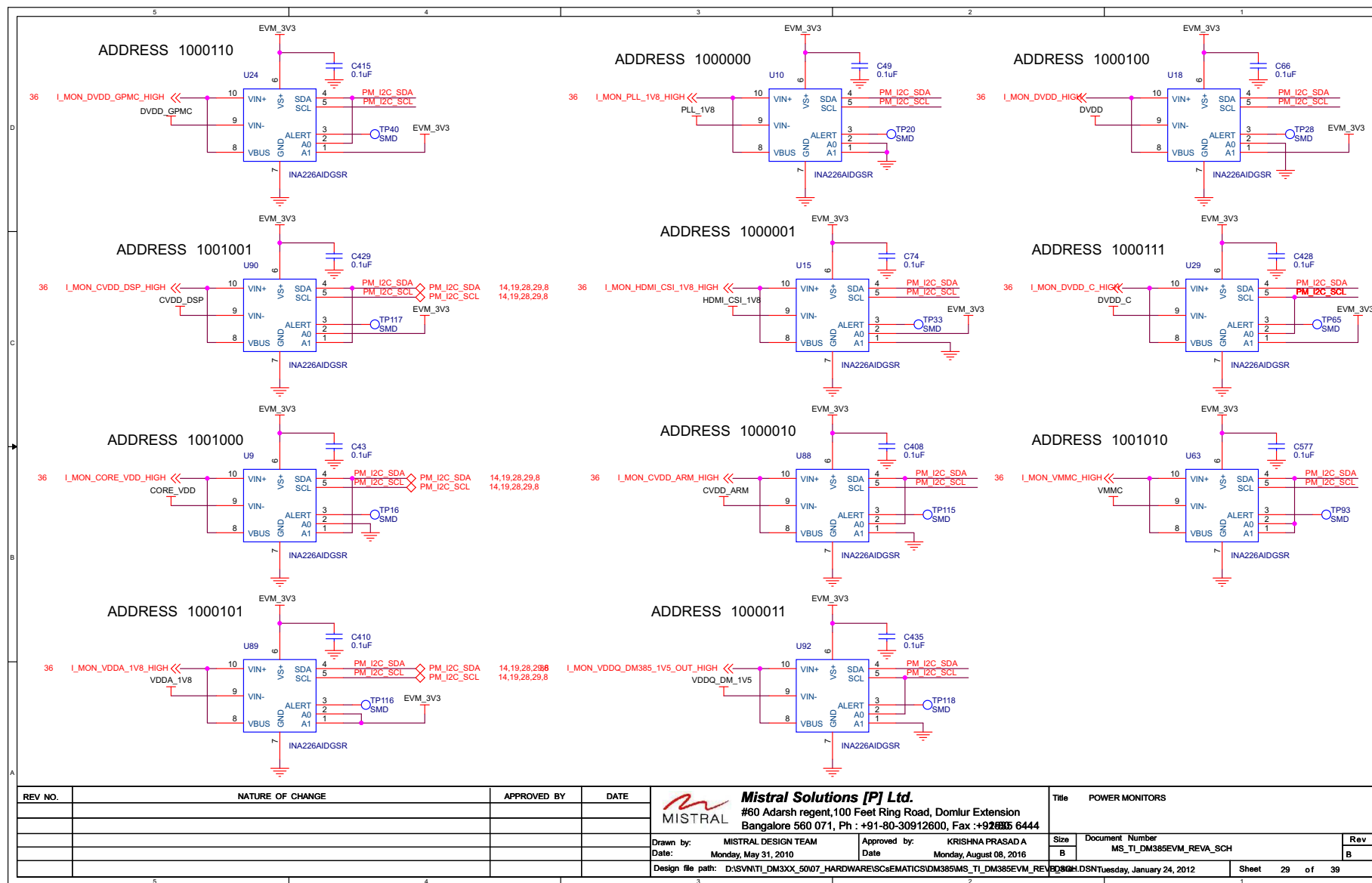


Figure A-28. Power Monitors



[illegible]

Figure A-30. DM385 VSS

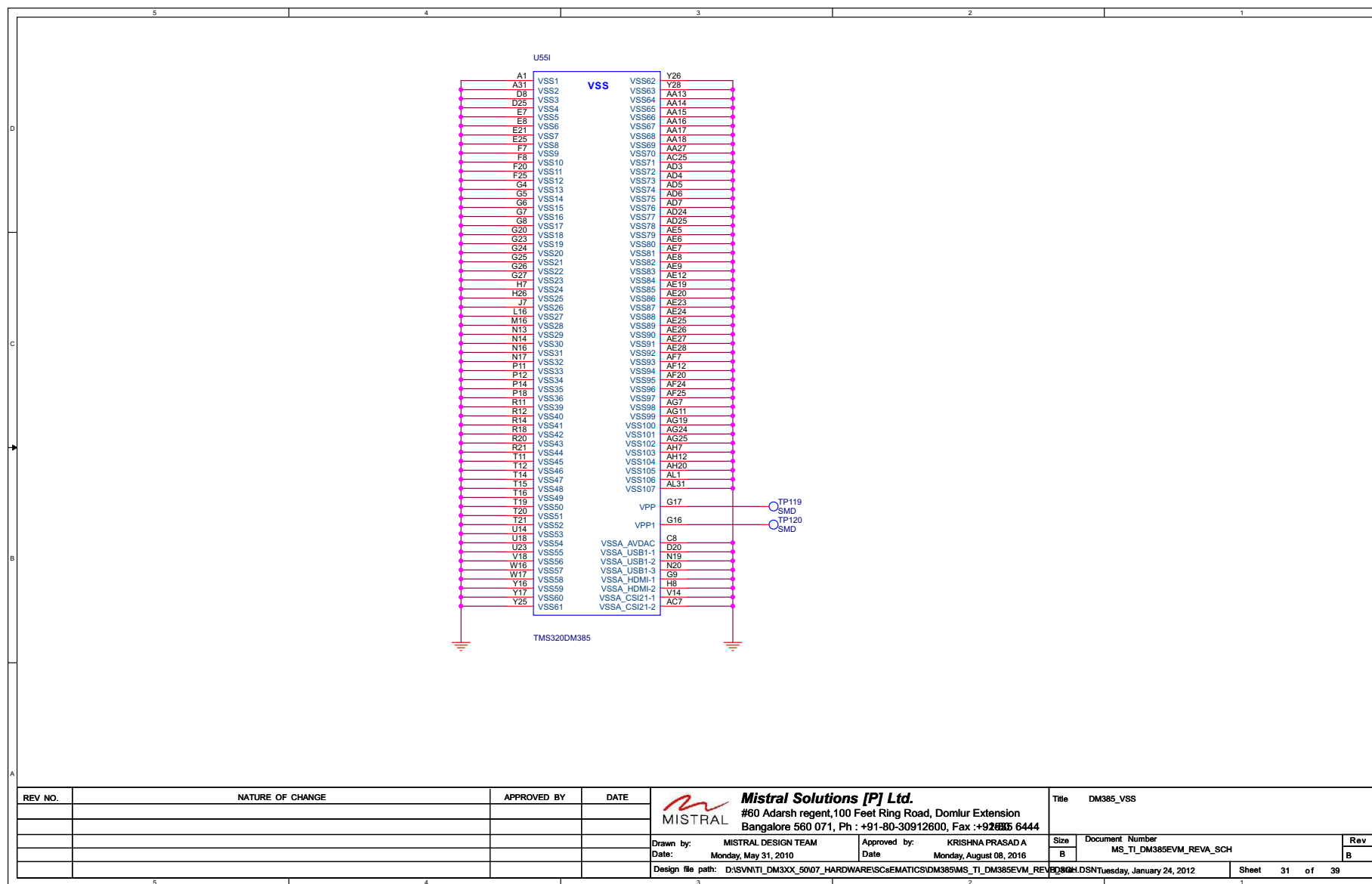


Figure A-31. TPS659113-A

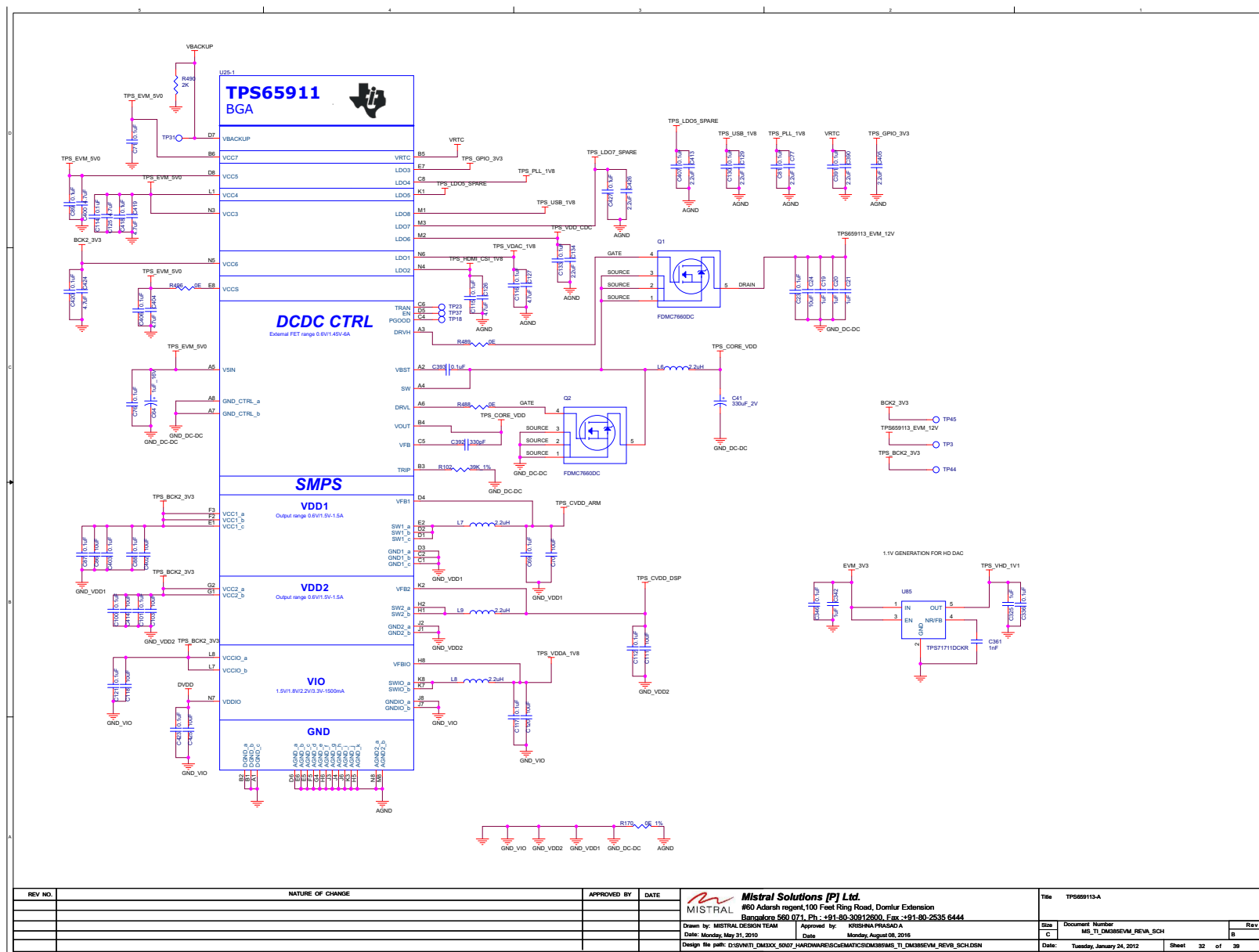
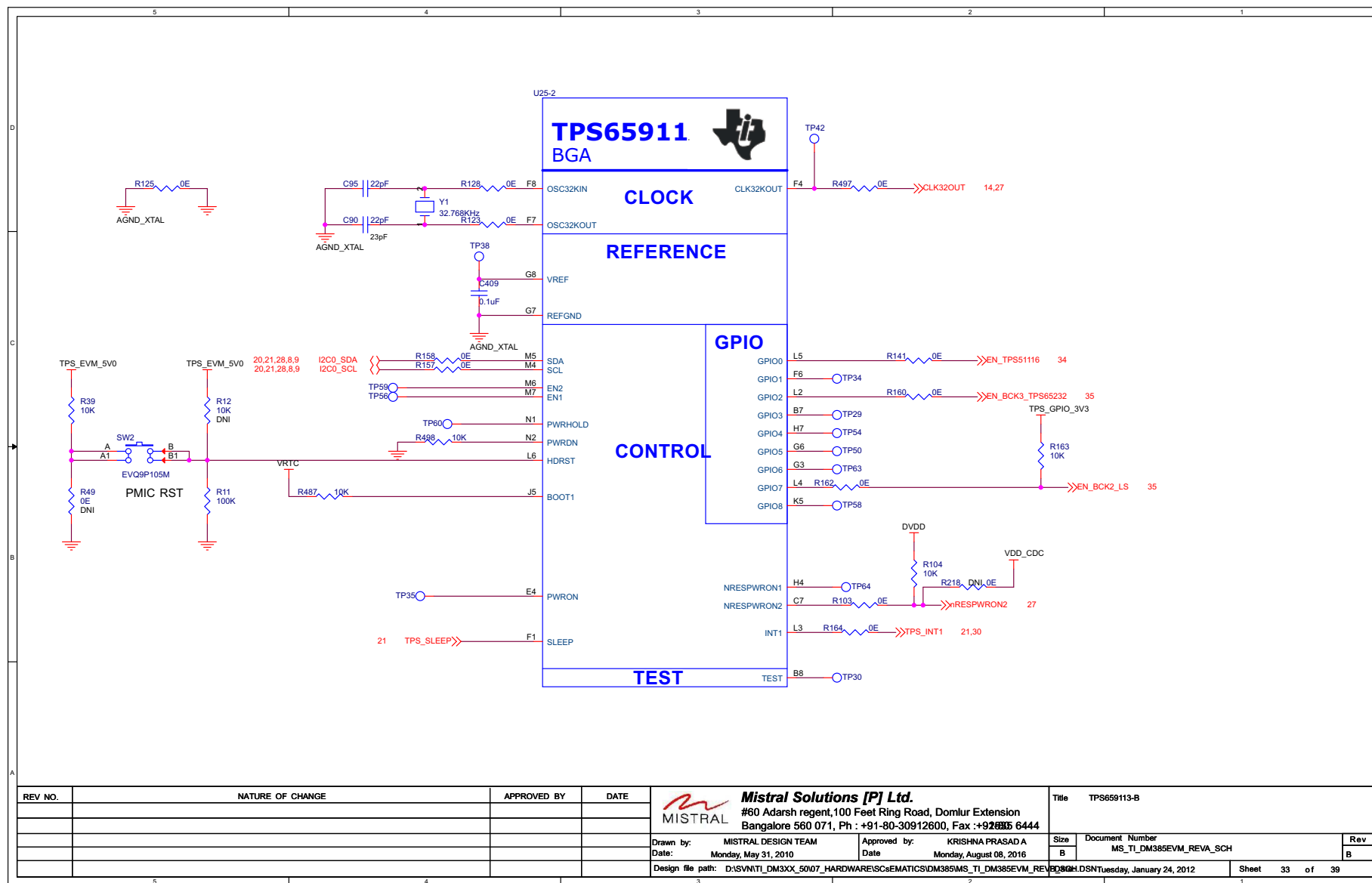


Figure A-32. TPS659113-B



The schematic diagram illustrates the internal circuitry of the TPS65232 evaluation board (EVM). Key components and their connections include:

- Power Management:** The board features three main power input sections:
 - TPS_BCK2_3V3:** A 3.3V input with a 6.98K resistor (R135) and a 1nF capacitor (C108).
 - TPS_EVM_5V0:** A 5V input with a 100pF capacitor (C397) and a 100pF capacitor (C73).
 - TPS65232_EVM_12V:** A 12V input with a 100pF capacitor (C73) and a 100pF capacitor (C83).
- Signal Processing:** The board includes a signal path with a 2.2uH inductor (L19) and a 100pF capacitor (C94), connected to a 100pF capacitor (C399) and a 100pF capacitor (C73).
- Control Logic:** The board contains a 12V input section with a 100pF capacitor (C73) and a 100pF capacitor (C83), connected to a 100pF capacitor (C73) and a 100pF capacitor (C83).
- Output Stages:** The board includes a 3.3V output section with a 100pF capacitor (C73) and a 100pF capacitor (C83), connected to a 100pF capacitor (C73) and a 100pF capacitor (C83).
- Other Components:** The board includes a 100pF capacitor (C73) and a 100pF capacitor (C83), connected to a 100pF capacitor (C73) and a 100pF capacitor (C83).

The diagram also shows the internal components of the TPS65232, including the 12V input section, the 3.3V output section, and the 5V output section. The board is designed to be used with a 12V input and a 3.3V output, and it includes a 5V output section for the TPS65232.

REV NO.	NATURE OF CHANGE	APPROVED BY	DATE
1	Initial Release		Monday, May 31, 2010

Mistral Solutions [P] Ltd.
 #60 Adarsh regent, 100 Feet Ring Road, Domlur Extension
 Bangalore 560 071, Ph : +91-80-30912600, Fax : +91-80-30912601

Design file path: D:\SV\WTL_DM3XX_5007_HARDWARE\SCHEMATIC\DM385\MS_TL_DM385EVM_REV_B.SCH

Sheet 35 of 39

[illegible]

Figure A-36. Power In

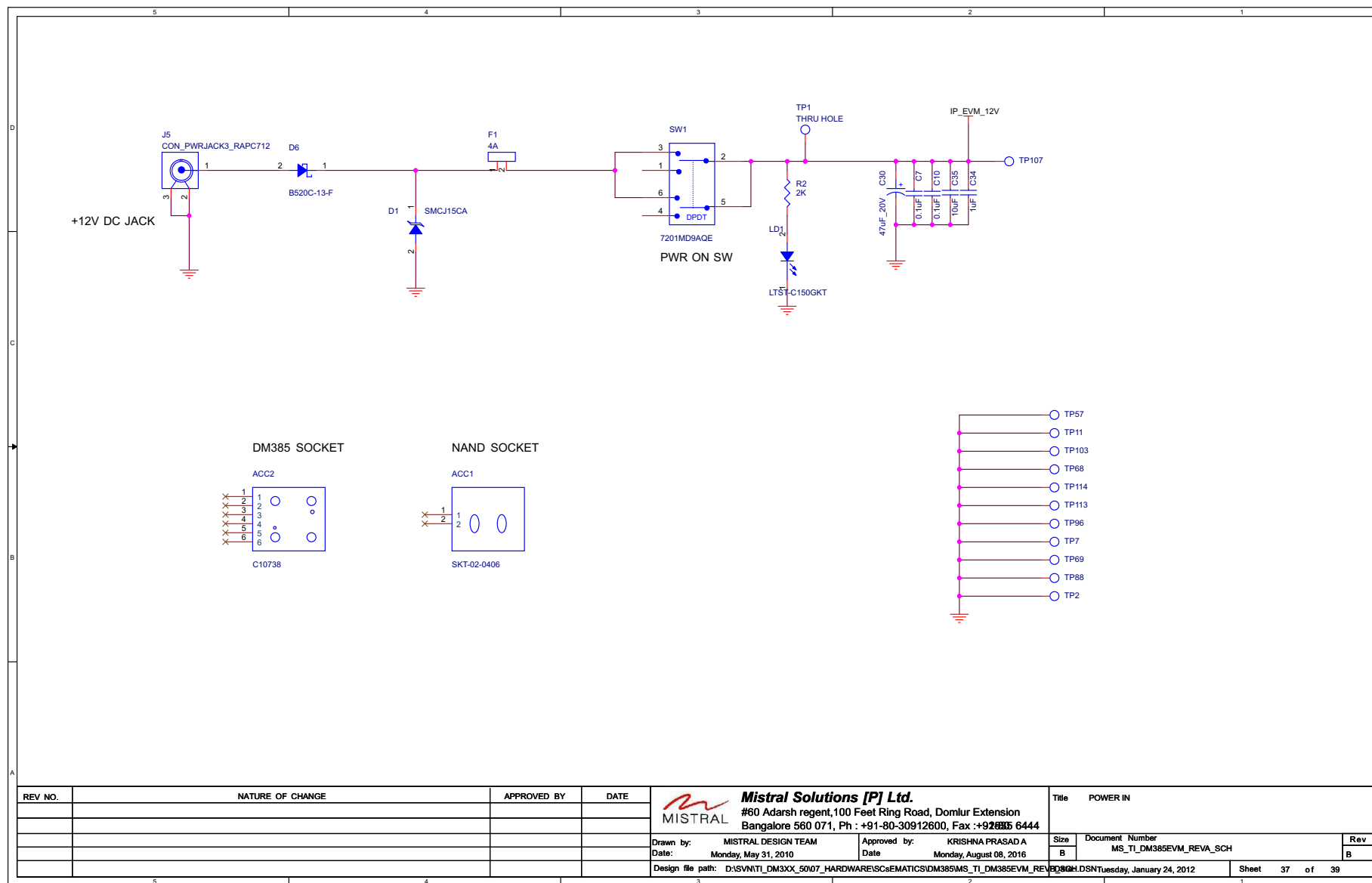
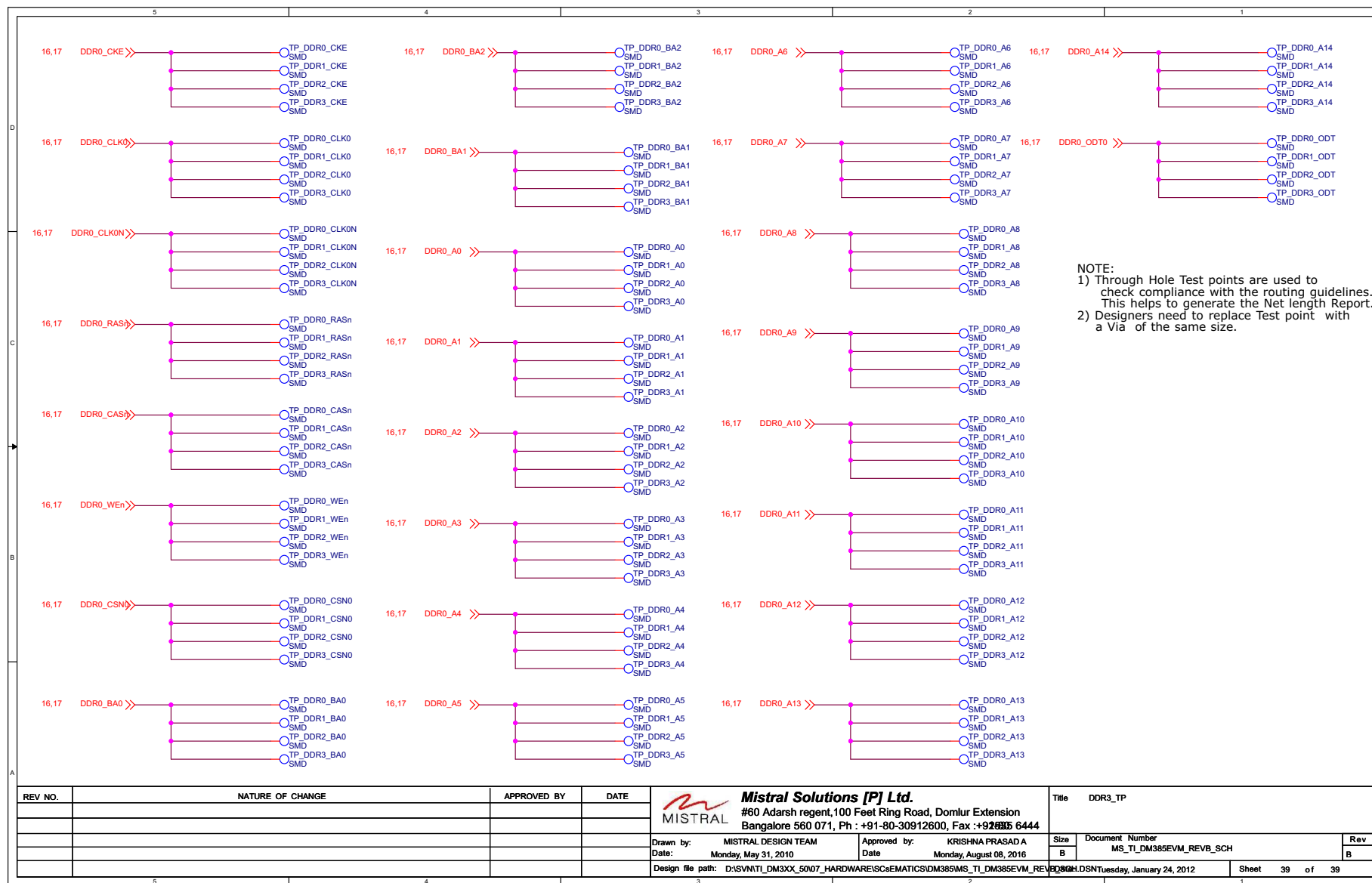


Figure A-37. Changes in Schematics

SL NO#	CHANGES IN THE SCHEMATICS COMPARED TO CENTAURUS.	SL NO#	CHANGES IN THE SCHEMATICS COMPARED TO CENTAURUS.
1	MLB SIGNALS ARE REMOVED.	39	CLOCK DRIVER IC IDT74FCT3807SDCG(U65) IS CHANGED TO CDCV304PW.
2	ONE MORE SATA (SATA1) CONNECTOR ADDED.	40	CODEC SIGNALS FROM MCASP MUXING STAGE IS PASSED THROUGH BUFFER ICs SN74AVCH1T45DBVR (U19,U20,U21) & SN74AVCH2T45DCTR (U22). BUFFER ICs ARE MADE DNI.OE RESISTOR OPTION IS GIVEN TO BYPASS THE BUFFER STAGE.
3	S-VIDEO SIGNALS REMOVED.	41	RESISTOR DIVIDER CKT TO GET VREF FOR DDR INTERFACE IS REMOVED AND VD_VREF IS TAKEN FROM TPS51116(PIN 5) DIRECTLY.
4	NEW DDR PART IS ADDED(ONLY FOR DDR0). DDR1 IS REMOVED.	42	A15 & B15 SIGNALS ARE SWAPPED.N30 & N31 SIGNALS ARE SWAPPED.P20 & P21 ARE CHANGED FROM VSS TO VDD5_OSC1 & VDD5_OSC0 respectively.
5	COMPOSITE VIDEO SIGNALS ARE TAKEN THROUGH VIDEO AMPLIFIER IC PROVIDING OPTION FOR DIRECT CONNECTION.	43	TESTPOINTS TP128,TP129 & TP130 ARE REMOVED AND J25,H24 & H28 OF DM385 IS MADE NC.
6	HDDAC SIGNALS ARE CONNECTED TO VIDEO AMPLIFIER THS7360IPW AND THEN THE OUTPUT ARE CONNECTED TO VGA CONN AND ALSO TO COMPONENT VIDEO CONNECTORS(RGB).	44	GPIO_VS_1 FROM IO EXPANDER-2 IS ADDED TO COMPENSATE FOR MLBP_CLK SIGNAL ON CENTAURUS. THIS SIGNAL IS USED AS GPIO ON VS BOARD.
7	27 MHZ CRYSTAL IS ADDED INSTEAD OF 22.579MHZ.	45	AN OR-GATE(U53) IS ADDED TO ENABLE THE WAKE-on-LAN FUNCTIONALITY OF ATHEROS CHIP. PCF8575_INT_VA INTERRUPT FROM IO EXPANDER-3 IS TERMINATED TO A TESTPOINT.INSTEAD OF THIS SIGNAL, ENET_WOL_INT INTERRUPT IS CONNECTED TO GP0[12] OF DM385.
8	IO EXPANDER-3 WITH I2C ADDRESS 0X20 IS ADDED. INTERRUPT PCF8575_INT_VA FROM THIS IC IS GIVEN TO SDO_DAT[6]/GP0[12].	46	C64 IS CHANGED TO PART NO# F93IC105MAA. RJ-45 SYMBOL UPDATED. FL10,FL11,FL12,FL13 (TCE1210) IS REPLACED WITH TCM1210.
9	HDMI ESD SUPPRESSOR TPD12S016KTR IS ADDED INSTEAD OF TPD12S521DBTR. HDMI_CT_HPD AND HDMI_LS_OE SIGNALS ARE TAKEN FROM NEWLY ADDED IO EXPANDER-2 WHOSE INTERRUPT IS CONNECTED TO SDO_DAT[7]/GP0[13].	47	TPD2E001(U122) ESD PROTECTION DEVICE FOR COMPOSITE VIDEO SIGNAL IS ADDED. TPD3E001(U123) ESD PROTECTION DEVICE FOR COMPONENT VIDEO SIGNALS IS ADDED.
10	MCASP0 AND MCASP1 MUXING IS ADDED. 2-4 DECODER IS USED TO ENABLE SWITCHING. IO EXPANDER-2 IS USED TO ENABLE DECODER.	48	R59 IS CHANGED TO 8mE.
11	EXPANSION CONNECTOR(DRI) TO GET POWER TO THE B8 IS REMOVED. POWER SELECTION SECTION IS MODIFIED ACCORDINGLY.	49	INA226 DEVICES ARE ADDED TO MONITOR DVDD,DVDD_C AND VMHC.
12	OPTION TO SELECT I2C2 OR UART2 SIGNALS IS PROVIDED.BUFFERS USED ARE ENABLED BY I2C2/UART2_SEL SIGNAL FROM IO EXPANDER-1.	50	PLL_1V8,HDMI_CSI_1V8 & DVDD_GPMC POWER LINES ARE MONITORED INSTEAD OF BCK2_3V3,EVM_SV0 & VDDQ_1V5 POWER LINES USING U10,U15 & U24 RESPECTIVELY.
13	SINCE THE MLB_DAT AND MLB_SIG IS NOT AVAILABLE IN DM385 TWO GPIOs FROM IO EXPANDER -2 IS GIVEN TO EXPANSION CONNECTOR WHICH ARE USED AS GPIOs ON THE CATLOG BOARD.	51	20MHz CRYSTAL (Y3) IS CHANGED TO SMALLER SIZE PACKAGE CRYSTAL WITH PN# 403C11A20M00000.
14	POWER VDDQ_CENT_1V5 IS CHANGED TO VDDQ_DM_1V5	52	L6 IS CHANGED FROM 2.7uH TO 2.2uH. Q1 & Q2 IS CHANGED TO FDMC7660DC FROM FDS8812NZ.
15	SATA INDICATOR LED IS ADDED.	53	R179 & R427 ARE REMOVED FROM THE DESIGN.
16	MCA_AXR[6:8] SIGNALS ARE REMOVED FROM THE CONNECTOR SIDE.		
17	MCA_AXR[9] SIGNAL WHICH IS USED AS GPIO IN VC BOARD IS TAKEN FROM IO EXPANDER-2		
18	BUS FET SWITCH IS ADDED THROUGH WHICH UART0 SIGNALS ARE CONNECTED TO EXPANSION CONNECTOR.		
19	I2C2 BUFFER IS ADDED AND SIGNALS ARE GIVEN TO IO EXPANDER-3 AND VGA CONNECTOR.		
20	POWER MONITORING IC INA220 IS UPDATED WITH INA226.		
21	SN74CBTLV3384PW(U3 & U40) ICs ARE REPLACED WITH SN74CB3Q3257PWR.DECODER USED FOR MCASP1 MUXING IS REMOVED.		
22	R399,R392,R254,R248,R522 ---OE RESISTORS ARE REPLACED WITH 22E. R579,R494 ARE REMOVED.		
23	PCA9306(U85 & U102) ICs ARE REPLACED WITH TCA4311A.		
24	OPTION FOR SELECTING MCAS_AFSR/AXR0 OR GPIOs FOR VC BOARD FROM IO EXPANDER-2 IS PROVIDED USING MUX.		
25	GPIO (IO_EXP2_GP3) FROM IO EXPANDER-2 IS PROVIDED TO COMPENSATE FOR MLB_CLK SIGNAL.		
26	OE OPTION IS GIVEN FOR VIN[0]A_VSYNC/GP2[4](C13).OE OPTION IS GIVEN FOR VIN[0]A_HSYNC/GP2[3] (D13)		
27	IO EXPANDER-1 INTERRUPT PCF8575_INT_I01 IS CHANGED FROM GP1[8] TO GP1[4].		
28	MUXING OPTION IS GIVEN TO SELECT DIFFERENT FUNCTIOS OF VOUT0/I_FLD PINS.ONE MORE DECODER IS ADDED TO SELECT ONE FUNCTION AT A TIME.		
29	I2C2/UART2_SEL SIGNAL IS REMOVED FROM THE IO EXPANDER-1 & IS TAKEN FROM DECER WHICH BY DEFAULT SELECT VOUT0/I_FLD SIGNAL.		
30	IO EXPANDER-1 INTERRUPT IS TAKEN FROM GP1[4] INSTEAD OF GP[8].		
31	U68 & ITS BIASING CIRCUITRY (1.2V FOR TPS_CVDD_HDVICP) OF CENTARAUS IS REMOVED AND ALSO U22(INA226) IS REMOVED		
32	TPS71711DCKR IS ADDED NEWLY TO GENERATE 1.1V FOR HD DAC		
33	TPD6E001 ESD SUPPRESSOR IS ADDED		
34	INA220 IS UPDATED TO INA226		
35	U80,U81,U106 & U112 ARE DELETED.TPD75019 (U7) IS ADDED.		
36	RAB6 IS REPLACED WITH 0E SERIES RESISTORS. R476 PACKAGE ISCHANGED TO 0402.		
37	EN_TPS62350 SIGNAL FROM TPS659113 IS REMOVED AS WE HAVE HAVE REMOVED TPS62350 IC.		
38	Q6 & Q7 ARE REMOVED.SN74LVC2G06DCK(U86) IS ADDED IN THE SATA LED INDICATOR SECTION. Y6 CRYSTAL MA-506 27,0000M-CO: (FUND):ROHS IS REPLACED WITH NEW PART ABM8-27,000MHZ-B2-T.		

REV NO.	NATURE OF CHANGE	APPROVED BY	DATE	 Mistral Solutions (P) Ltd. #60 Adarsh regent,100 Feet Ring Road, Domtur Extension Bangalore 560 071, Ph : +91-80-30812600, Fax :+91-80-2535 6444 Down by: MISTRAL DESIGN TEAM Approved by: KRISHNA PRASADA Date: Monday, May 21, 2010 Date: Monday, August 08, 2016 Design file path: C:\SV\NT1_DM38X_6007_HARDWARE\SCHEMATICS\DM385\MS_TL_DM385VM_REV_B_SCH.DSN	Title	SCH_CHANGES
					Size	Document Number
				C	MS_TL_DM385VM_REV_B_SCH	B
					Date: Tuesday, January 24, 2012	Sheet 38 of 39

Figure A-38. DDR3_TP



Assembly Drawings

The assembly prints for the DM388 device are the same as the assembly prints for the DM385 device.
[Figure B-1](#) and [Figure B-2](#) show the assembly prints.

Figure B-1. Assembly Drawing (Top Side)

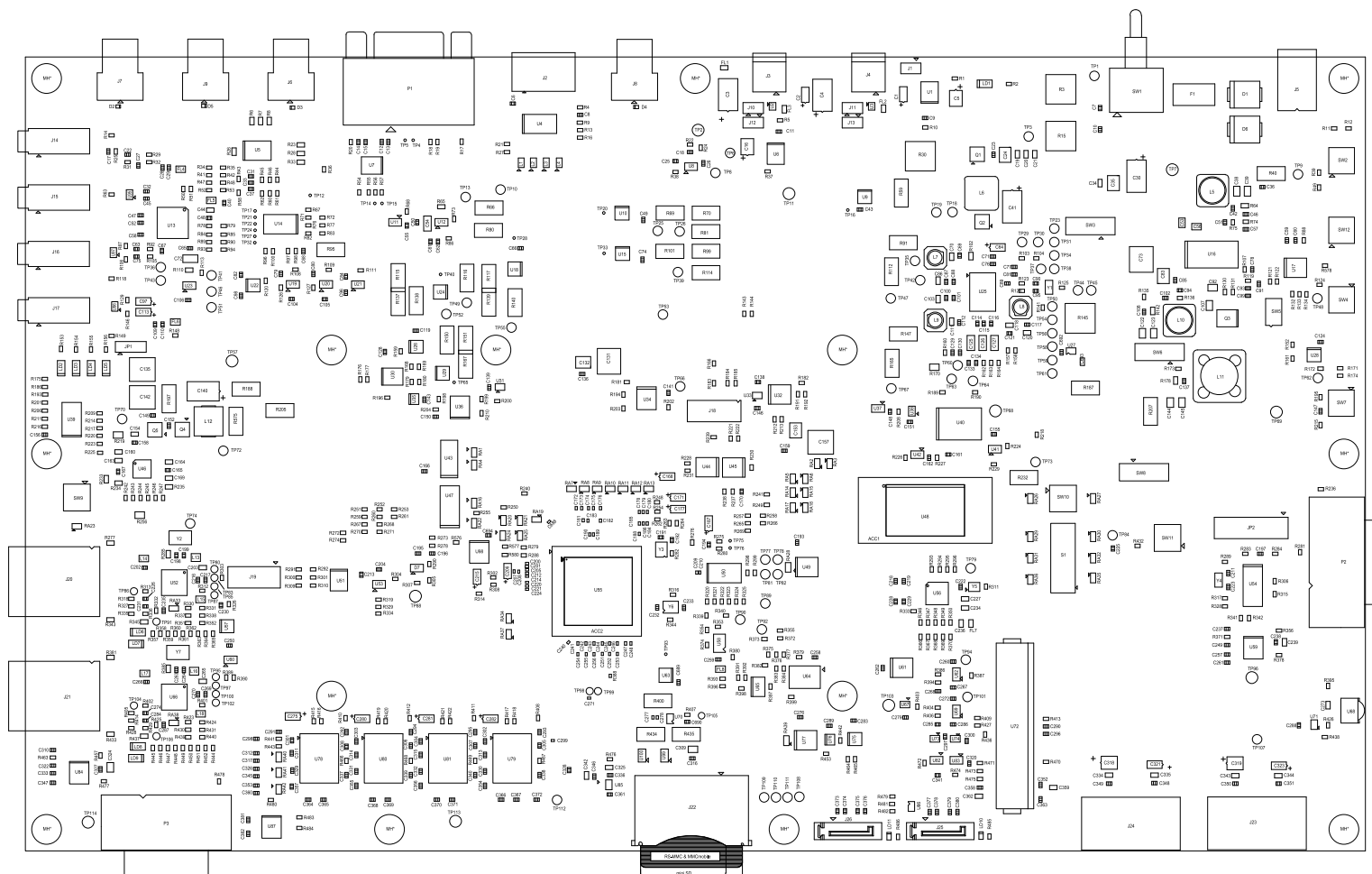
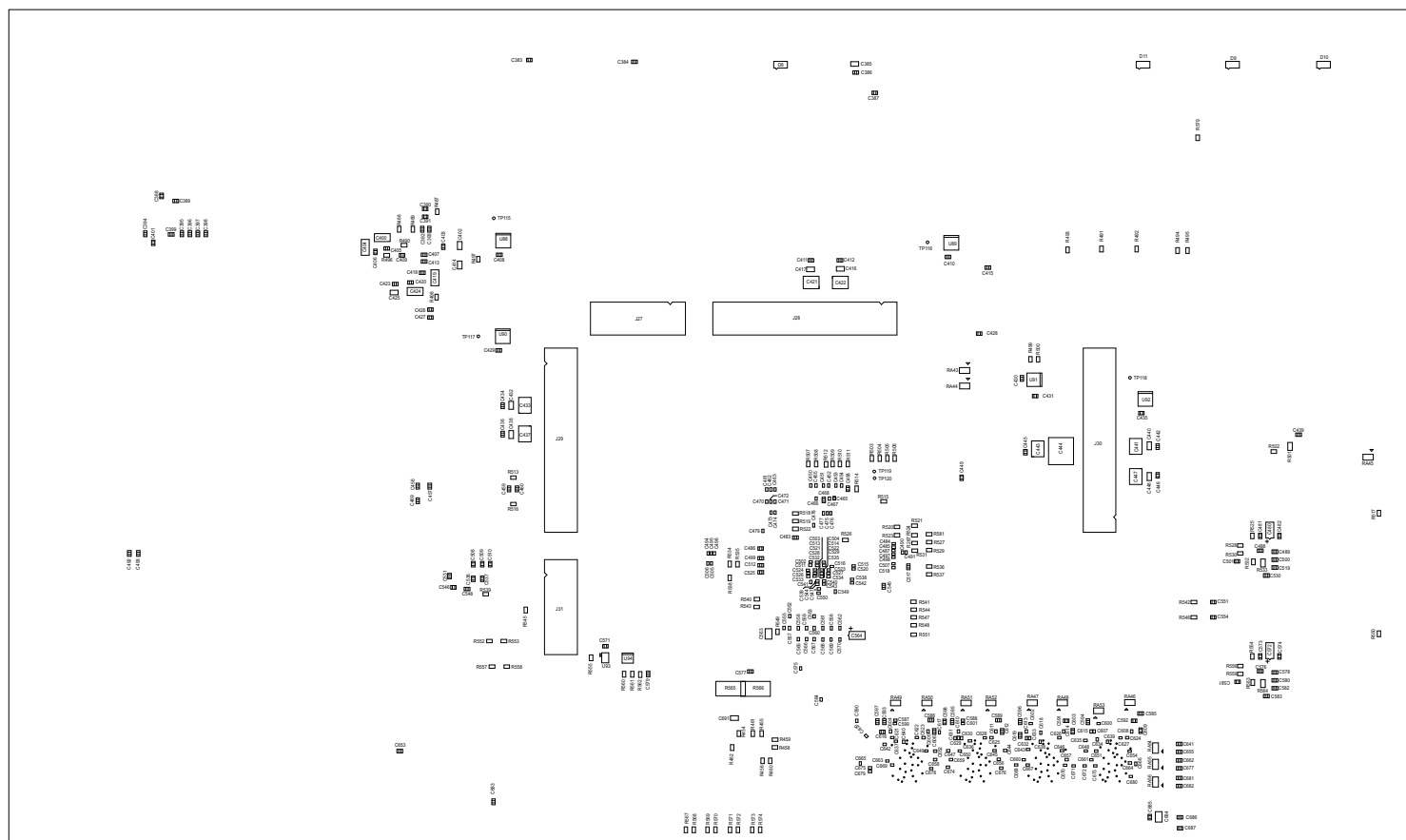


Figure B-2. Assembly Drawing (Bottom Side)



STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/sds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/sds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html>

3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 EVM Use Restrictions and Warnings:

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 Safety-Related Warnings and Restrictions:

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. Disclaimers:

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMNITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.
10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025