Texas Instruments

Part 2: Next-generation server power designs with integrated GaN technology

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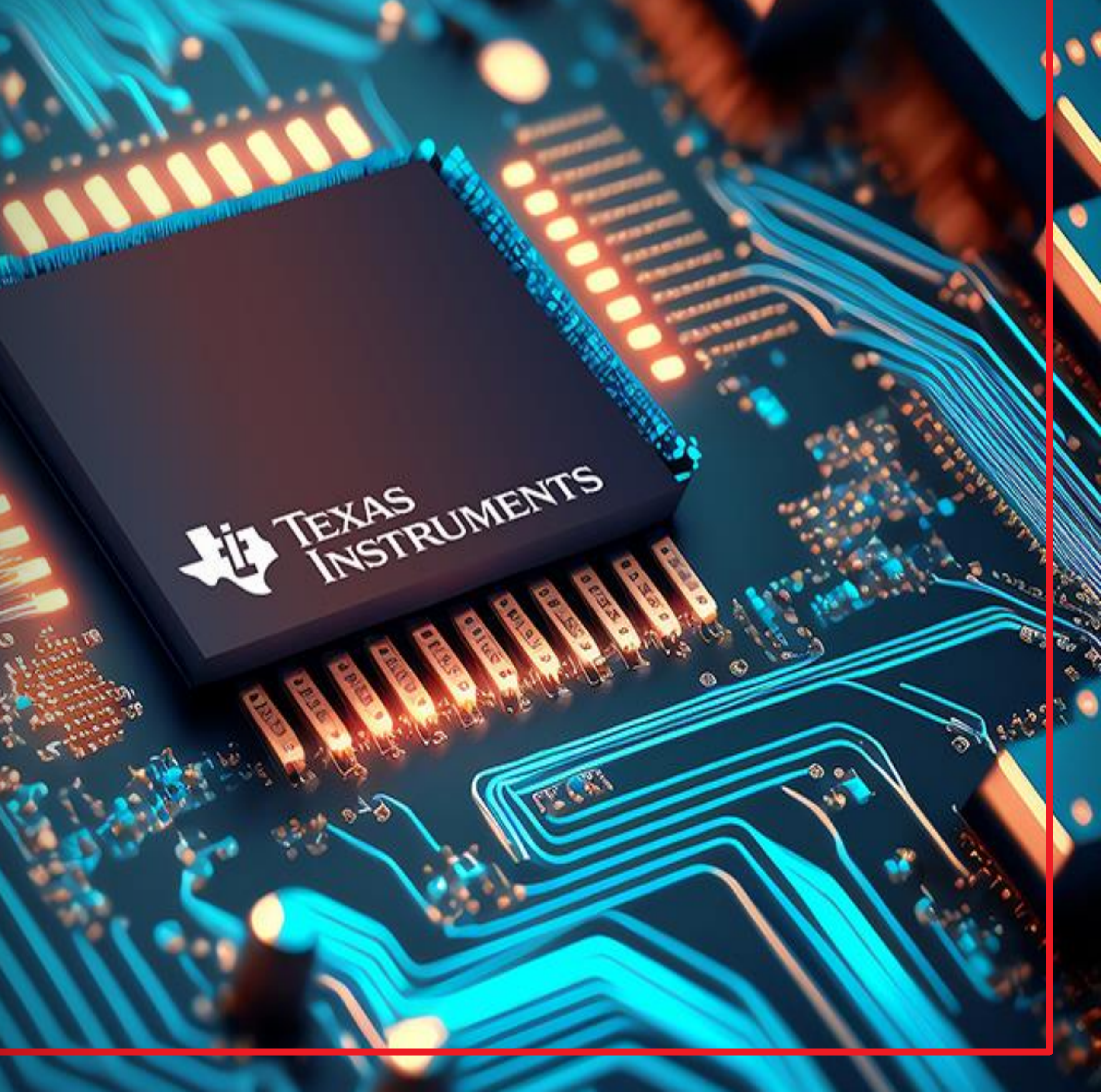
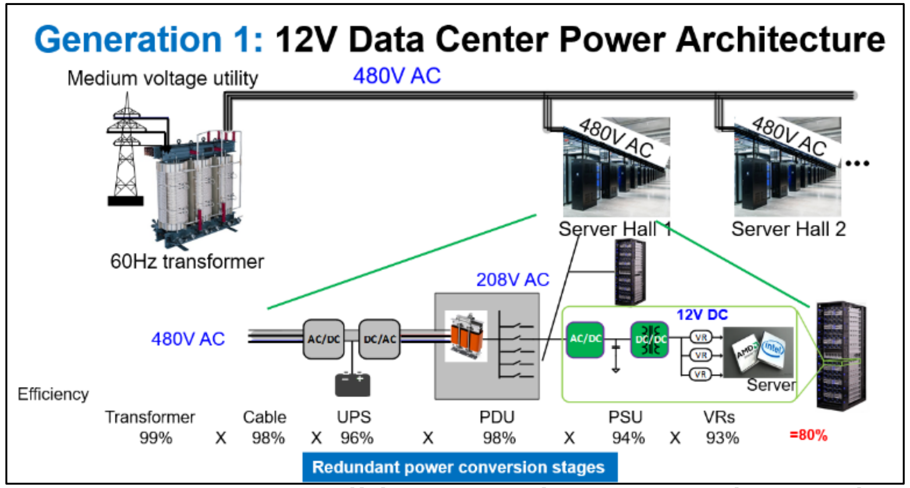


Agenda

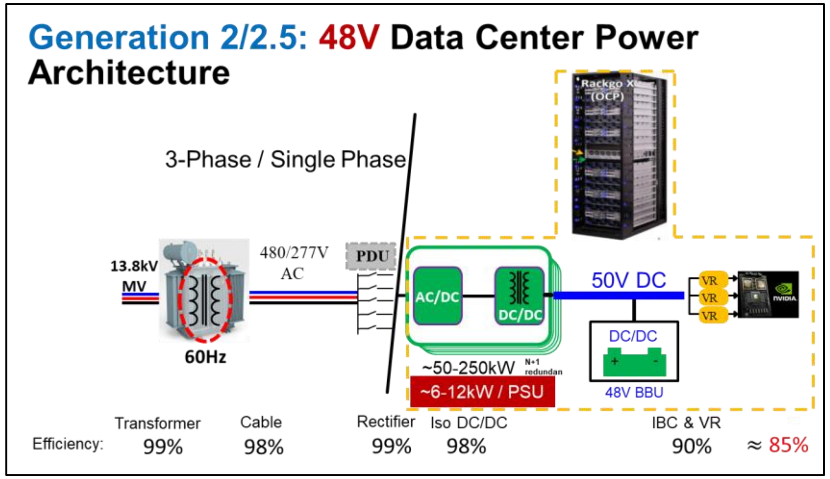
- Server power system evolution
- TI presence in server power
- Server power supply unit deep dive
  - PFC stage
  - ISO DC/DC stage
- Server power controllers
  - Server main power stage controller
  - Server aux supply controller
- Q&A

Please feel free to share your questions on "chat." We will also have 10 minutes of live Q&A towards the end of the presentation

Server PSU market trends and challenges

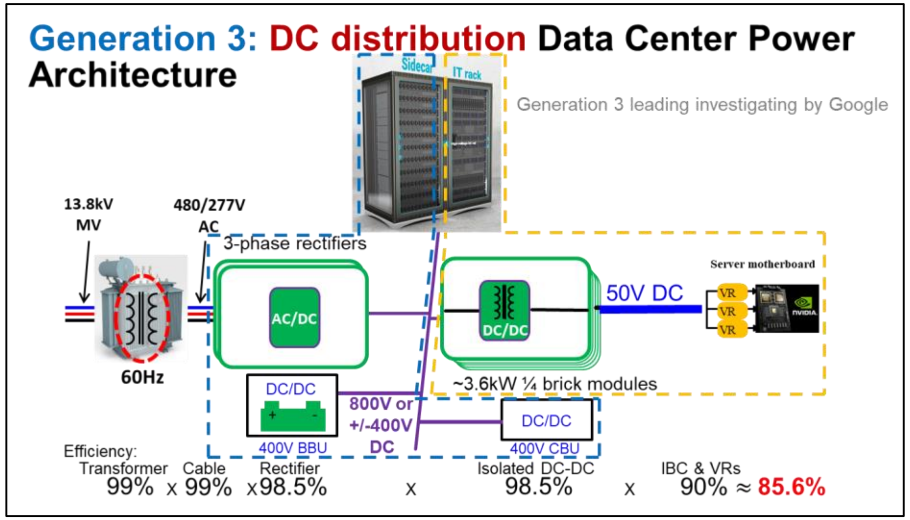


1990s – Now: Traditional rack servers (CRPS)

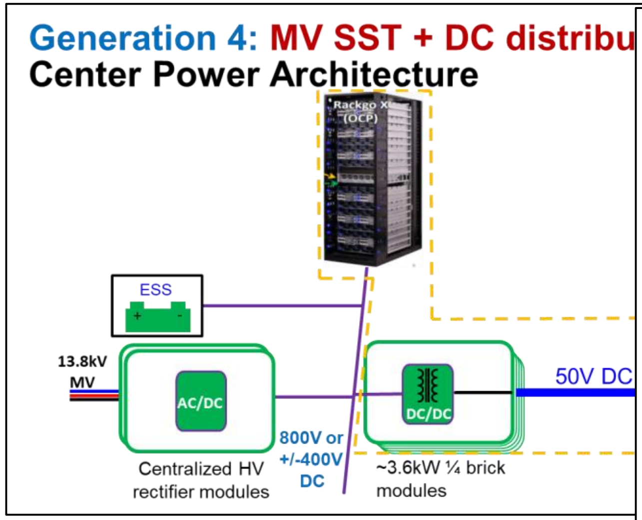


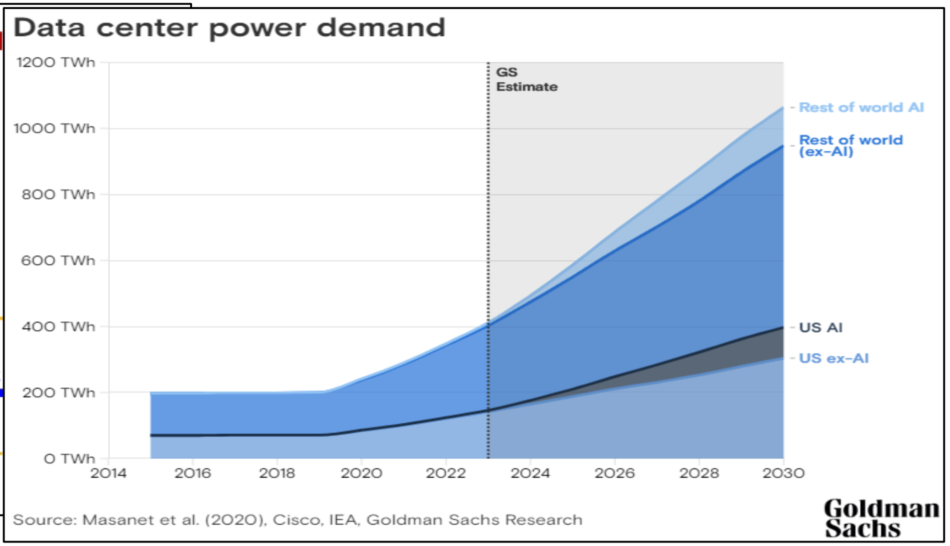
2016 – 2027: Cloud/AI computing (Open rack)

- Efficiency
- Power consumption
- Size
- Power density

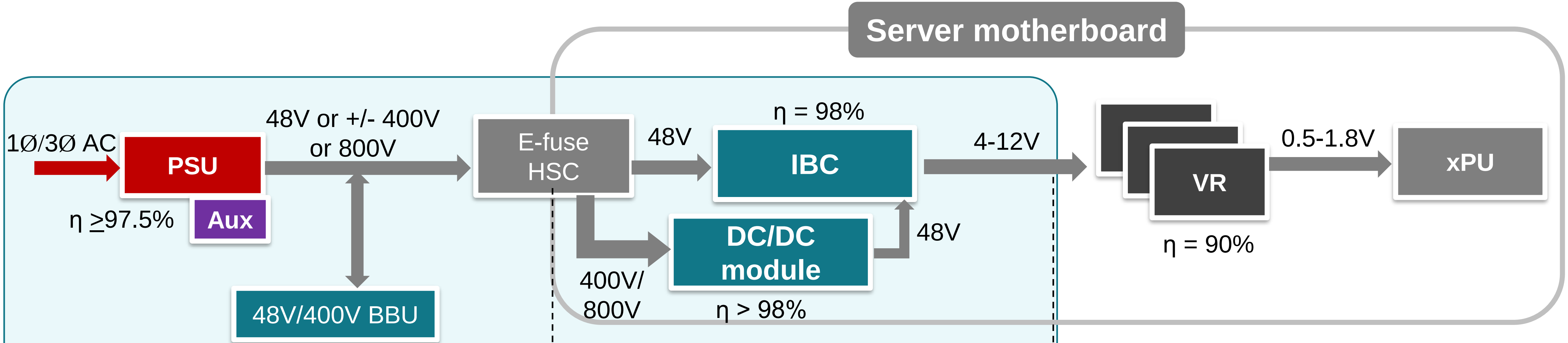


2027 onwards





TI solutions from grid to gate – Gen 2 & 3 architectures



PSU(AC/DC + DC/DC) + BBU: (DC/DC) + Aux power

- 650V GaN integrated power blocks
- 100/170V GaN integrated SRs/ HBs
- Digital controllers: UCD3138 and C2K
- Aux integrated power stage: UCG2882x
- Packages with thermal enhancements
- Advanced protection / monitoring features; OCP, OTP, ZVD, current sense

IBC: 48V to 4-12V DC/DC Module: 400/800V to 48V

- 650V GaN integrated power blocks
- 100/170V GaN integrated SRs/ HBs
- 40V monolithic SRs
- Digital controllers: UCD and C2K

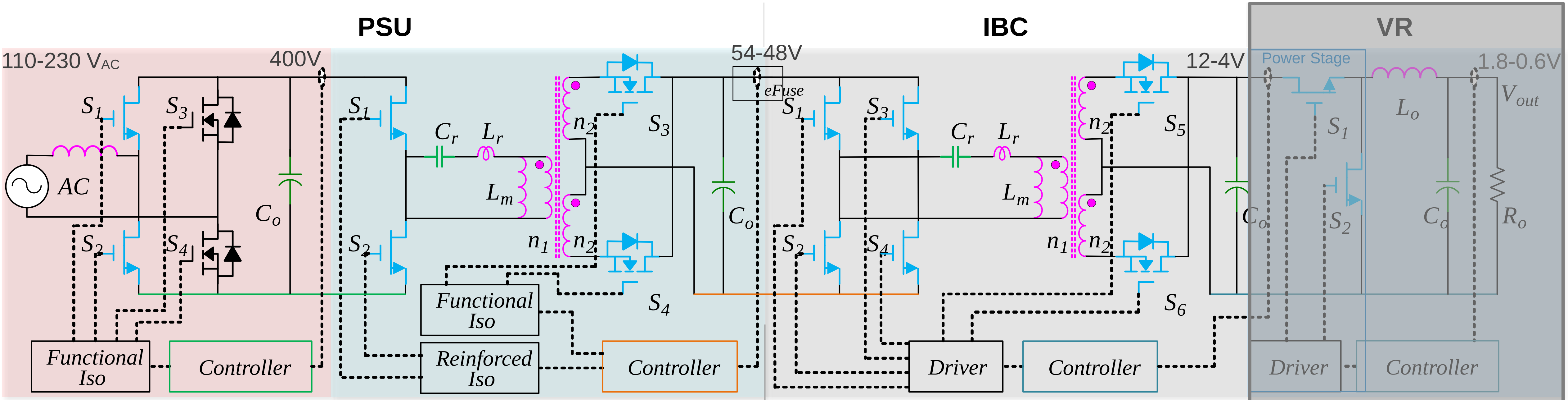
Multiphase VR

- Monolithic high current,
- High frequency power stage
- Integrated power module

TI-GaN

Server power delivery

GaN in server power (Gen 2 architecture)



- **Totem pole bridgeless PFC as rectifier**
- **650V GaN without Qrr**

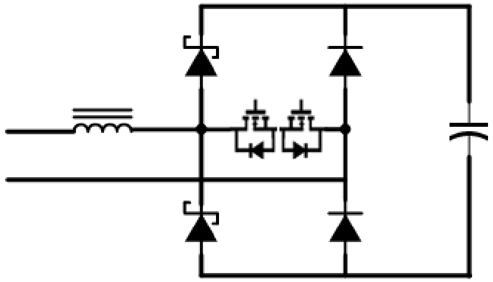
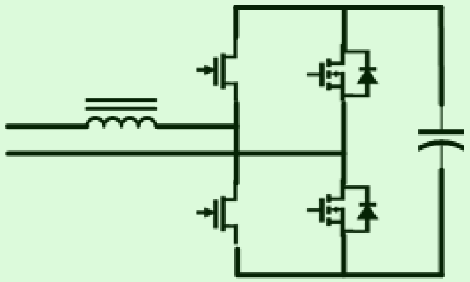
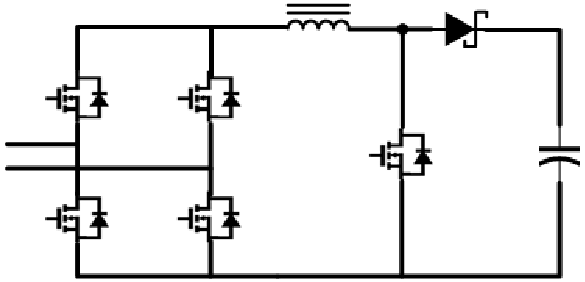
- **LLC resonant converter for isolated DC-DC stage**
- **Integrated GaN for deadtime optimization**
- **MV GaN as SR**

- **100V GaN power blocks**
- **40V monolithic SRs**

- Monolithic power stages
- Integrated capacitors
- Inductor integrated power stages

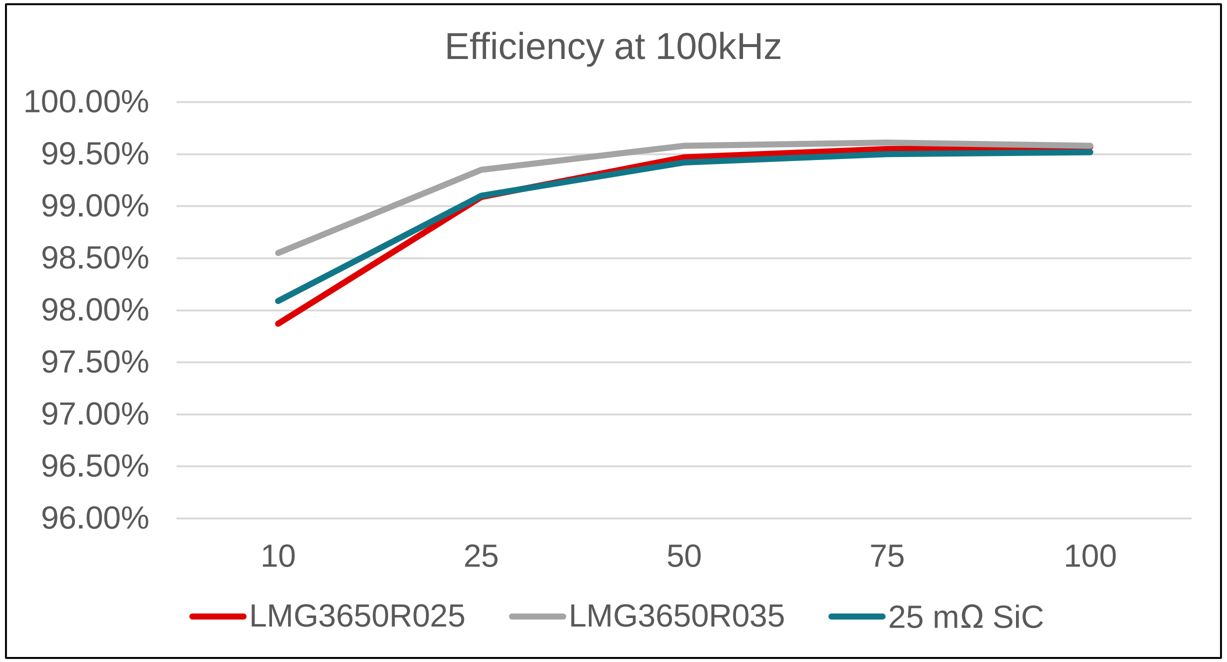
PFC

Which is the most efficient PFC architecture?

	AC switch PFC	Totem-pole PFC	Active bridge PFC
Block diagram			
Details	2 silicon diodes 2 MOSFETs 2 silicon diodes or SiC diodes 1 choke coil	2 **GaN FETs** or SiC MOSFETs 2 MOSFETs 1 choke coil	5 MOSFETs 1 SiC diode 1 choke coil
Cost	Medium	Low	High
Efficiency	On-time: 2 MOSFETs Off-time: 1 SiC diode + 1 silicon diode	On-time: 1 MOSFET + 1 FET Off-time: 1 MOSFET + 1 FET	On-time: 3 MOSFETs Off-time: 2 MOSFETs + 1 diode
	~98.7%	**~99.0%**	**~98.5%**

[Why GaN Enables High Efficiency in Totem-Pole PFC-Based Power Designs (powersystemsdesign.com)]

LMG3650R0XX vs 25mΩ SiC (100kHz)



Conclusion: LMG3650R035 has a better loss performance at mid load and full load due to lower switching loss combined with better performance on Qrr loss.

Test conditions:

- 2ph Totempole CCM PFC
- 4.5kW, 240Vac, 400Vdc
- 100kHz, 2ph. design
- Tamb = 55degC

	LMG3650R025	LMG3650R035	25mΩ SiC
Rdson, typ at 25C [mohm]	24	35	25
Coss(tr) [pF]	458	299	322

LMG3650R025

Load (%)	Device Conduction Power Loss (W)	Device Coss Power Loss (W)	Overlap Power Loss (W)	Deadtime Loss (W)	Switching Loss (W)	Driver Loss (W)	Total Loss per Device (W)	Efficiency (%)
10	0.016	2.300	0.029	0.013	2.329	0.086	2.443	97.87%
25	0.103	2.300	0.072	0.032	2.372	0.086	2.592	99.09%
50	0.422	2.300	0.143	0.065	2.443	0.086	3.016	99.47%
75	1.092	2.300	0.215	0.100	2.515	0.086	3.793	99.55%
100	2.072	2.300	0.286	0.136	2.586	0.086	4.880	99.57%

LMG3650R035

Load (%)	Device Conduction Power Loss (W)	Device Coss Power Loss (W)	Overlap Power Loss (W)	Deadtime Loss (W)	Switching Loss (W)	Driver Loss (W)	Total Loss per Device (W)	Efficiency (%)
10	0.022	1.500	0.029	0.013	1.529	0.086	1.650	98.55%
25	0.142	1.500	0.072	0.032	1.572	0.086	1.832	99.35%
50	0.591	1.500	0.143	0.066	1.643	0.086	2.386	99.58%
75	1.412	1.500	0.215	0.103	1.715	0.086	3.315	99.61%
100	2.736	1.500	0.286	0.141	1.786	0.086	4.749	99.58%

25mΩ SiC

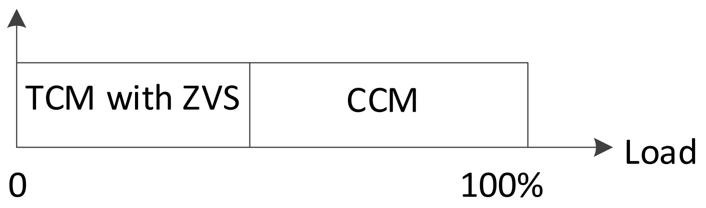
Load (%)	Device Conduction Power Loss (W)	Device Coss Power Loss (W)	Overlap Power Loss (W)	Deadtime Loss (W)	Switching Loss (W)	Driver Loss (W)	Qrr Loss(W)	Total Loss per Device (W)	Efficiency(%)
10	0.013	1.800	0.057	0.022	1.857	0.172	0.121	2.185	98.09%
25	0.082	1.800	0.143	0.055	1.943	0.172	0.302	2.554	99.10%
50	0.335	1.800	0.286	0.111	2.086	0.172	0.605	3.308	99.42%
75	0.771	1.800	0.430	0.168	2.230	0.172	0.907	4.247	99.50%
100	1.409	1.800	0.573	0.227	2.373	0.172	1.210	5.390	99.52%

*Due to slow switching compared to GaN, SiC overlap loss is 2x GaN loss
** Due to higher driving strength for SiC FET, SiC driver loss is 2x GaN loss

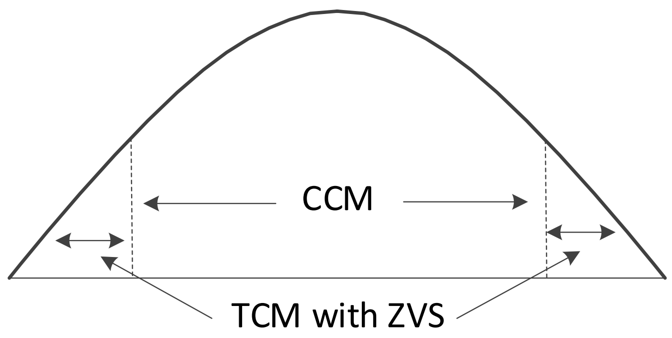
PFC mode of operation: CCM vs. TCM

	CCM operation	TCM operation
Pros	• Low inductor current ripple • Simple control	• Zero voltage switching (ZVS)
Cons	• Hard switching – high switching loss	• High inductor current ripple • Require multi-phase interleaved to reduce current ripple for high power applications: ❖ low power density ❖ high cost • Complex control

Why multi-mode PFC: CCM/TCM multi-mode operation



Multi-mode at different load



Multi-mode in AC half cycle

Combine the advantages of CCM and TCM:

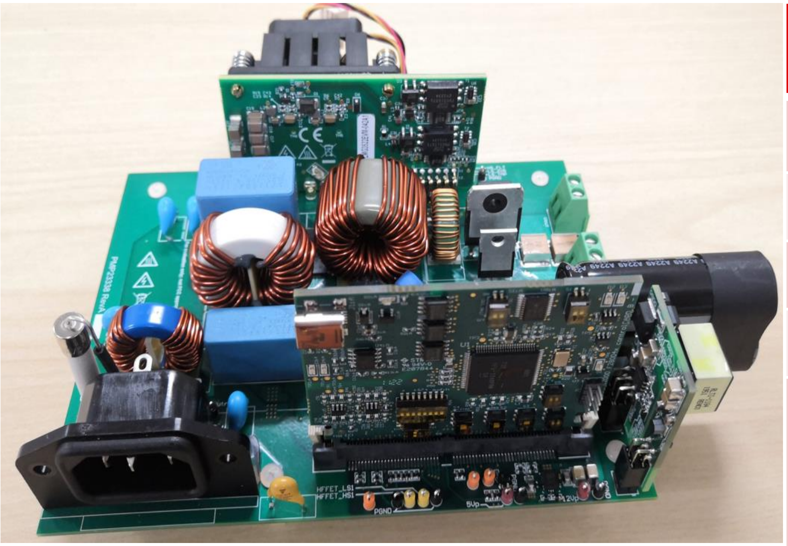
- Higher efficiency than CCM
  - ZVS when in TCM
- Higher power density and lower cost than interleaved TCM
  - Single phase
- Easier control than TCM
  - Same controller works for both CCM and TCM

PMP23537 CCM/TCM multi-mode controlled TTPL bridgeless PFC design

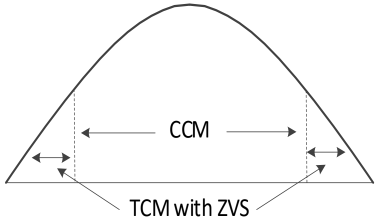
In Development

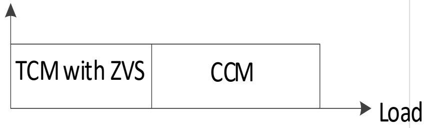
Features

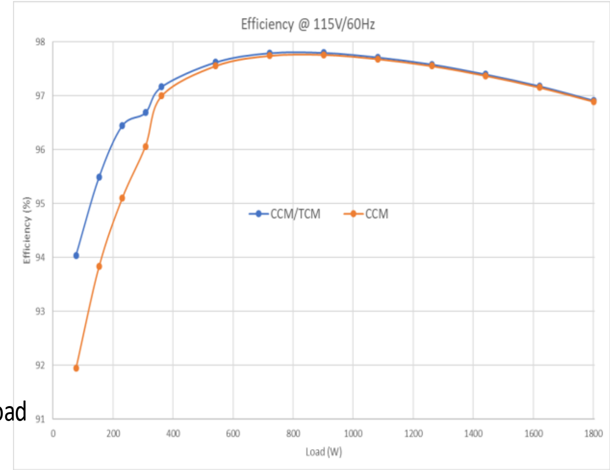
- CCM/TCM-ZVS multi-mode control in each AC half cycle. Light load efficiency is improved up to 2%
- TI GaN with integrated zero current sensing
- Single current sensor for both PFC control and e-metering with >99.5% accuracy
- Includes baby boost to extend holdup time and reduce bulk cap
- Re-rush current control when AC comes back from dropout

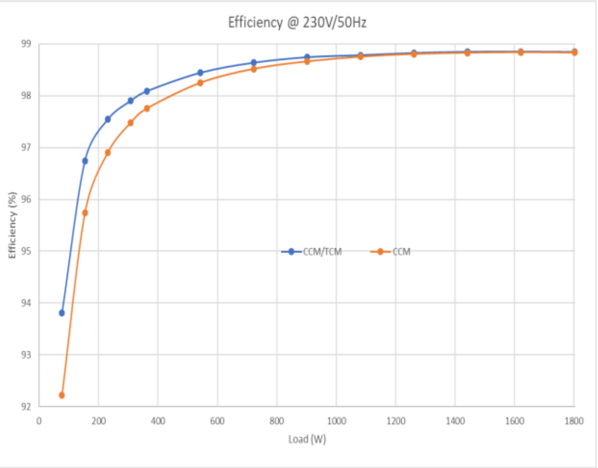


Parameter	Specification
Input voltage	85-265VAC
Output voltage	385VDC
Output power	3.6KW
Topology	Totem-pole PFC
IC	LMG3427R30, AMC1306, TMS320F28003x, TMCS1133, UCC27712, TPSM863252, UCC21220

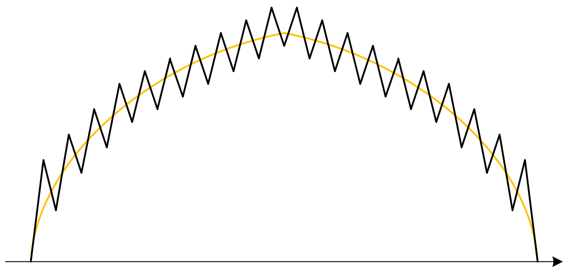






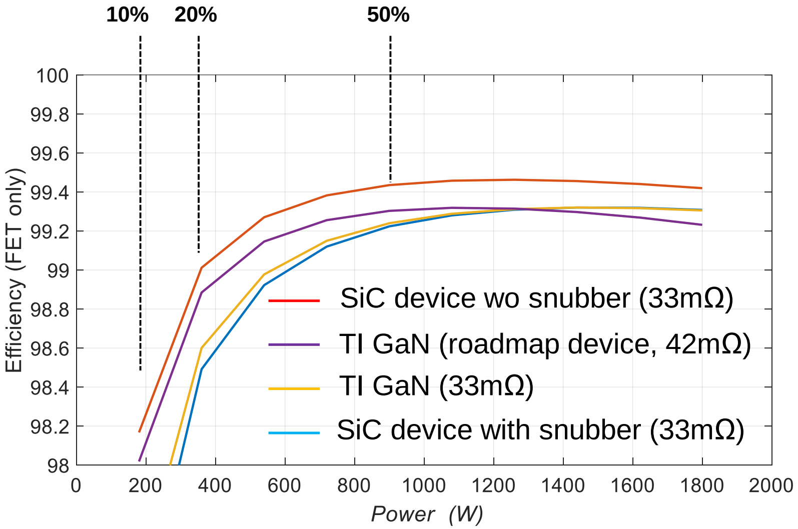


Efficiency comparison summary

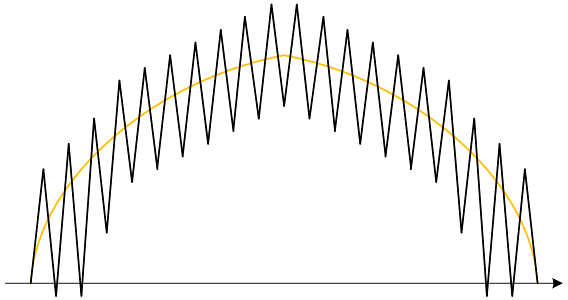


CCM: Continuous conduction mode

1-phase

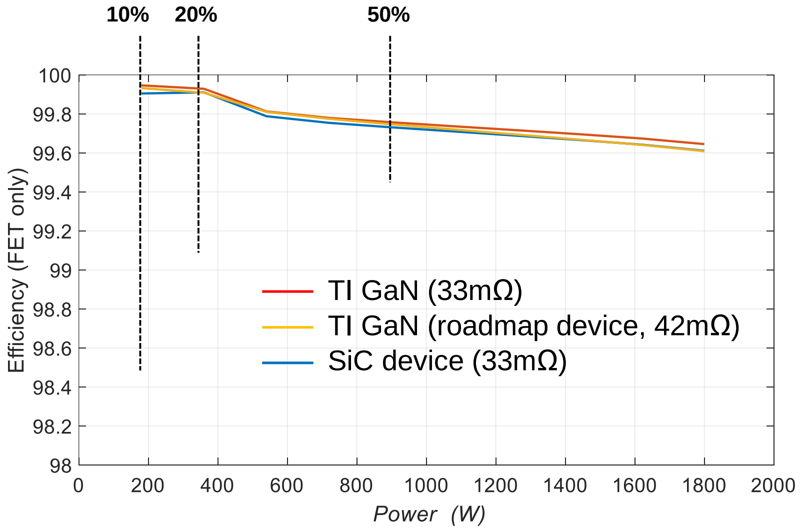


Parameter	Comp. SiC	TI GaN	TI GaN
Ron at 25C	33mΩ	33mΩ	42mΩ
Half-load η	99.2% - 99.4%	99.2%	99.3%

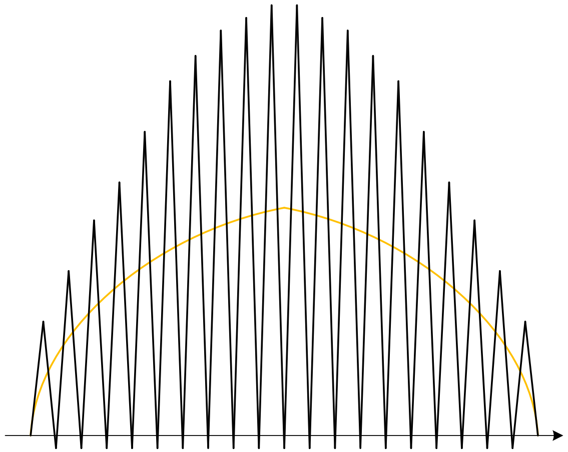


Multi-mode: CCM + TcM

L = 150µH, 1-phase

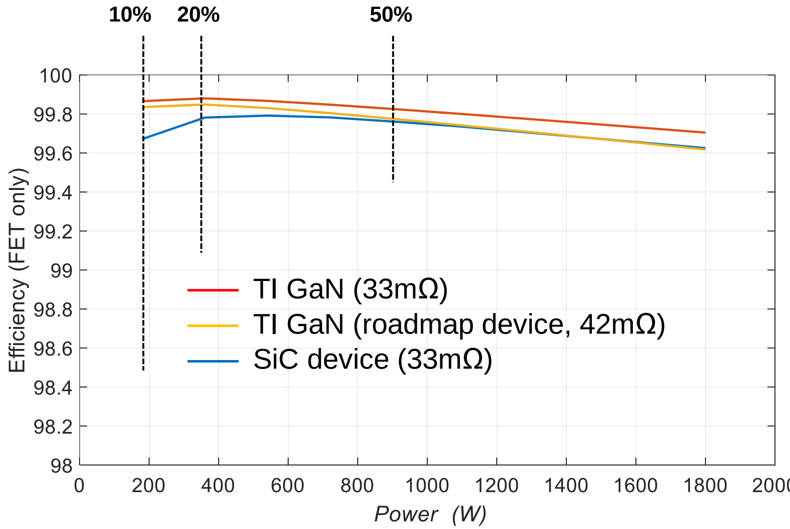


Parameter	Comp. SiC	TI GaN	TI GaN
Ron at 25C	33mΩ	33mΩ	42mΩ
Half-load η	99.73%	99.76%	99.75%



TcM: Triangular current mode

L = 25µH, 1-phase



Parameter	Comp. SiC	TI GaN	TI GaN
Ron at 25C	33mΩ	33mΩ	42mΩ
Half-load η	99.76%	99.82%	99.78%

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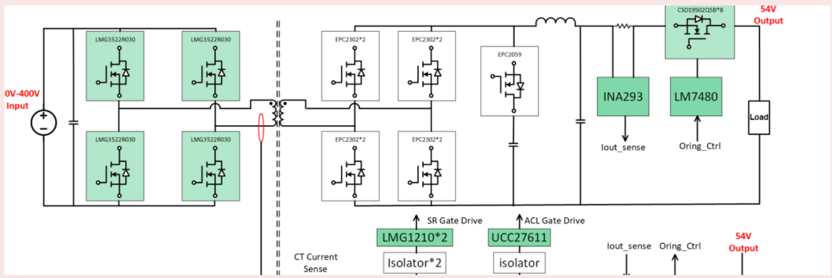
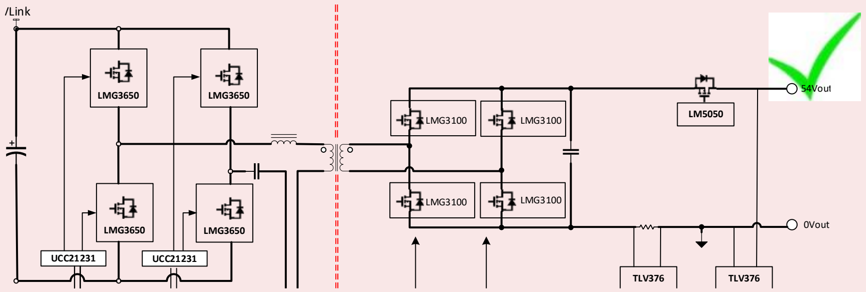
ISO DC/DC

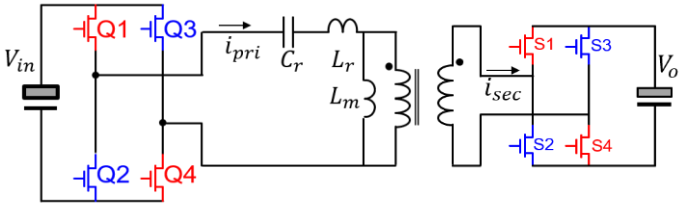
Which is the most efficient ISO DC/DC architecture?

	PSFB	FB-LLC with FB-secondary
Block diagram		
Cost	Medium	Low
Efficiency	**up to 98%**	**~98.5%**
High frequency operation	**Not suited beyond 200Khz**	**Can go 500Khz+**
Control & sync.	**Simpler**	**Slightly complicated as it works in a tight load and frequency range**
EMI	**Slightly complicated EMI management**	**Better performance**

LLC stage 2.3KW(FB- primary, FB- secondary) – Design & device parameters

Inputs:

Primary Topology:	Full-Bridge	
Secondary Topology:	Full-Bridge	
Number of output Rectifiers:	2	
Number of Parallel SRs / Rectifier:	2	
Input Votlage, Vin:	400	V
Output Votlage, Vo:	48	V
Output Power, Po:	2300	W → 1ph.
Switching Frequency, fs:	100	kHz
Magnetizing Inductance, Lm:	500	uH
Deadtime, td:	100	ns



Primary side device: HV Si-MOSFET

Vds (V) =	650	
Rdson (mOhm) =	27	@ 25 oC
Rdson (mOhm) =	52.6	@ 125 oC
Qg (nQ) =	108	
Vgs (V) =	10	
Eoff* (uJ) =	1.8	*Turn-off Energy - Eoss @10A turn-off
Coss (pF)=	1604	@ Vin

Secondary side device: MV Si-MOSFET

Vds (V)=	80	
Rdson (mOhm)=	1.9	@ 25 oC
Rdson (mOhm)=	3.04	@ 125 oC
Qg (nQ)=	31	
Vgs (V)=	10	
Coss (pF)=	1200	@ Vin
Body Diode Forward Voltage (V)=	0.82	

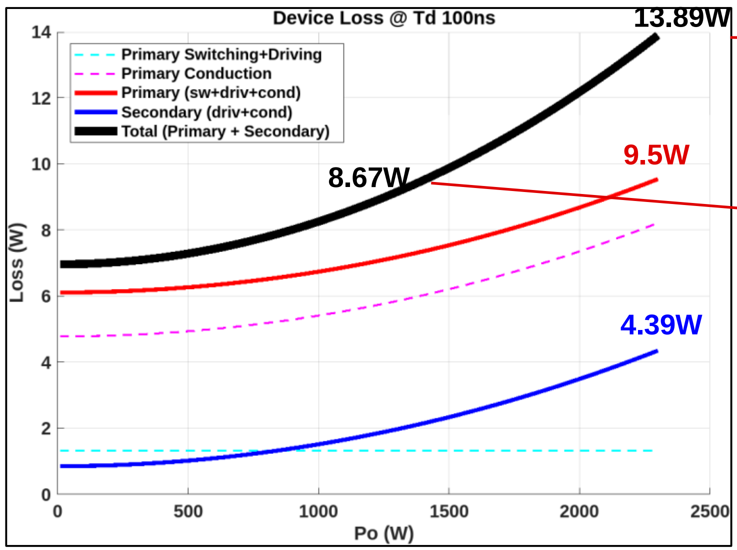
Primary side device: LMG3650R025

Vds (V) =	650	
Rdson (mOhm) =	24	@ 25 oC
Rdson (mOhm) =	43.2	@ 125 oC
Qg (nQ) =	119	
Vgs (V) =	12	
Eoff* (uJ) =	0.3	*Turn-off Energy - Eoss @10A turn-off
Coss (pF)=	458	@ Vin

Secondary side device: LMG3100R017

Vds (V)=	100	
Rdson (mOhm)=	1.7	@ 25 oC
Rdson (mOhm)=	2.41	@ 125 oC
Qg (nQ)=	20	
Vgs (V)=	5	
Coss (pF)=	1547	@ Vin
Body Diode Forward Voltage (V)=	1.5	

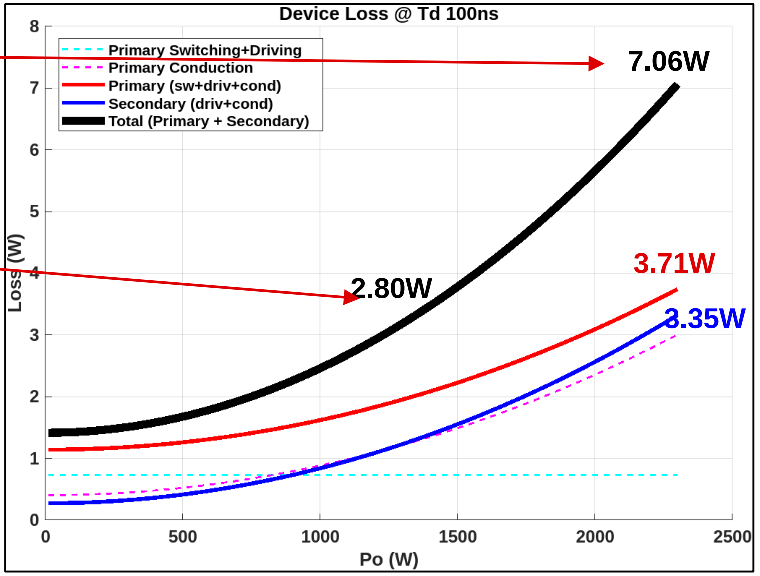
650V Si-MOSFET + 80V Si-MOSFET vs. LMG3650R025 + LMG3100R017

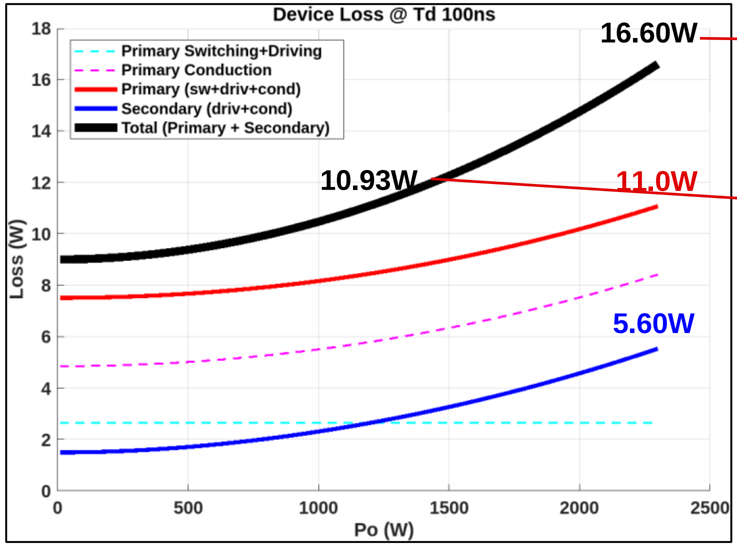


49.2% lower

67.7% lower

100KHz

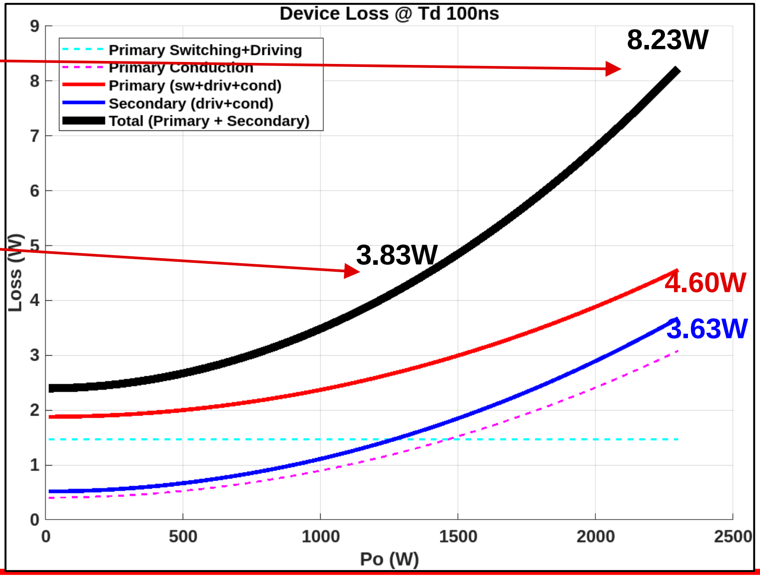




50.4% lower

64.95% lower

200KHz

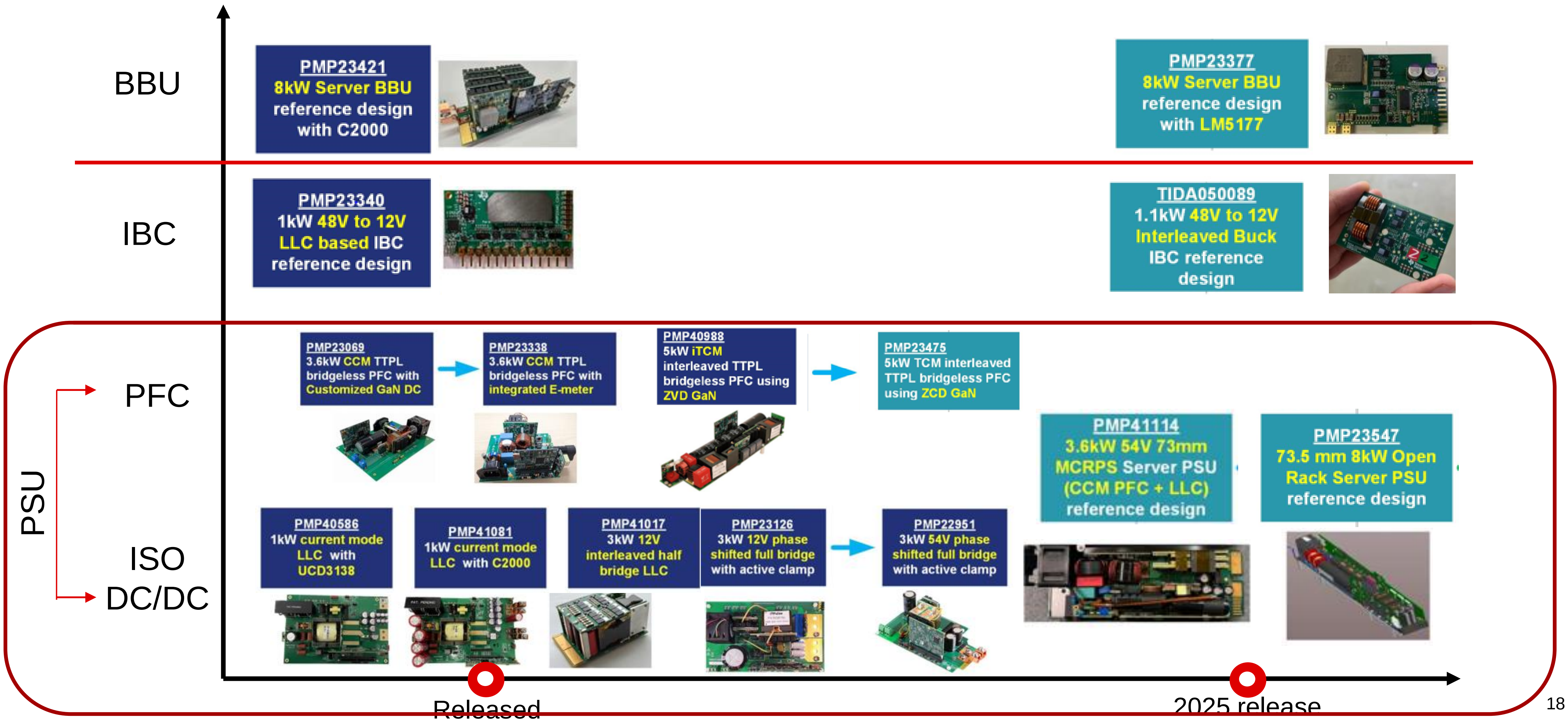


Server PSU, BBU and IBC reference designs

Status

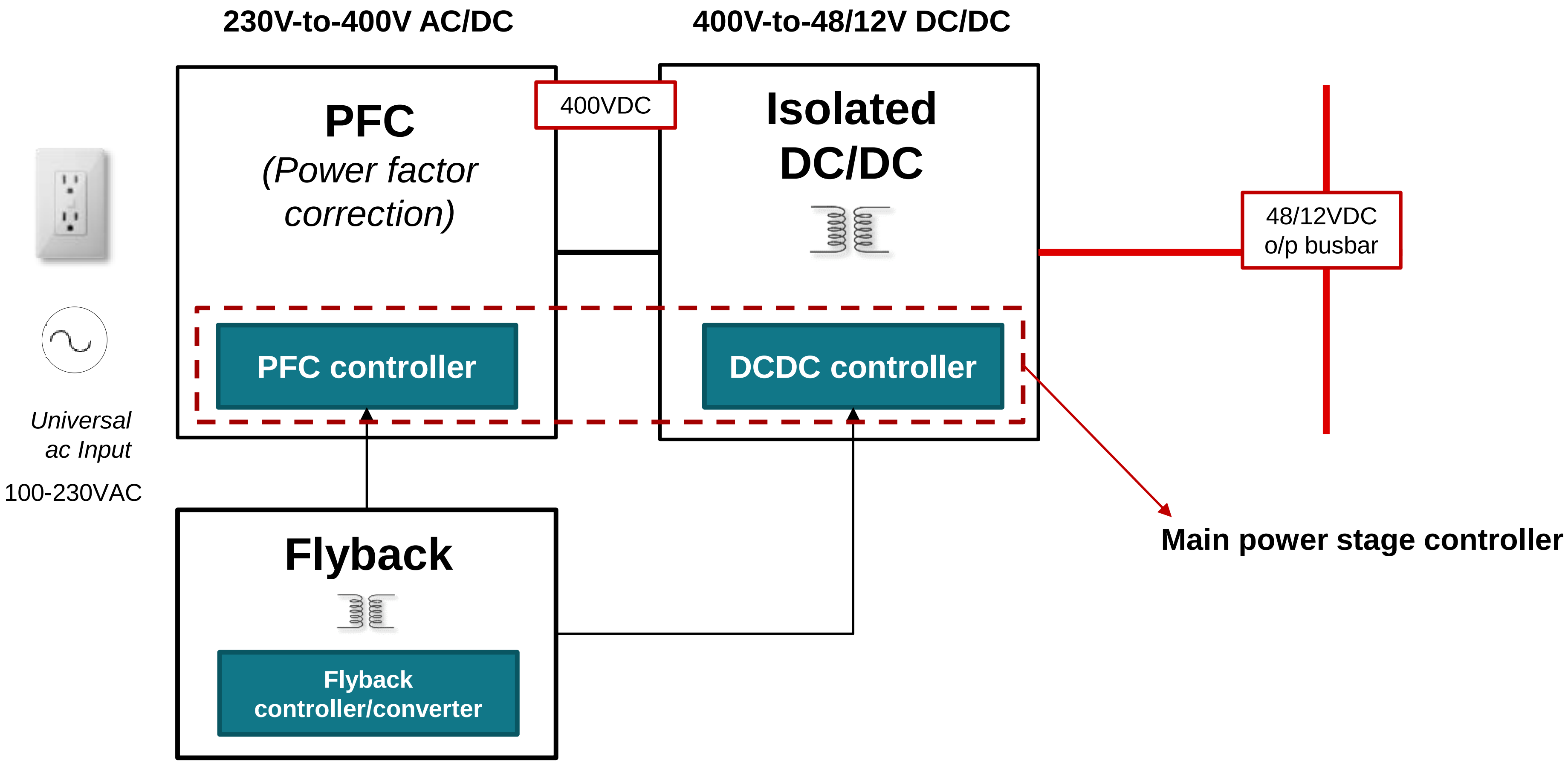
≤2024 release

2025 designs



Controllers in the server PSU

Typical server power supply control uses individual controllers at each stage



Increasing power density driving digital control in main power stage

Power supply

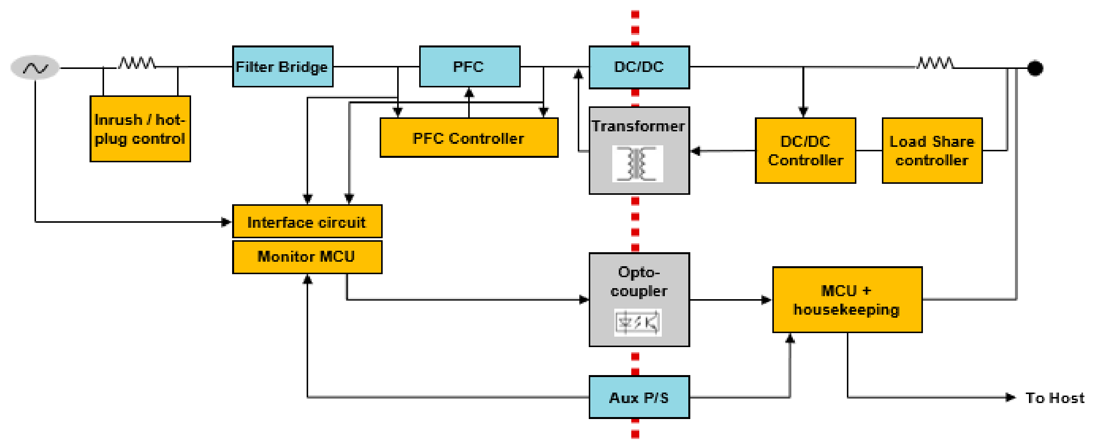
Basic power supply control

- Output regulation vs. line/load variations
- Fault protection

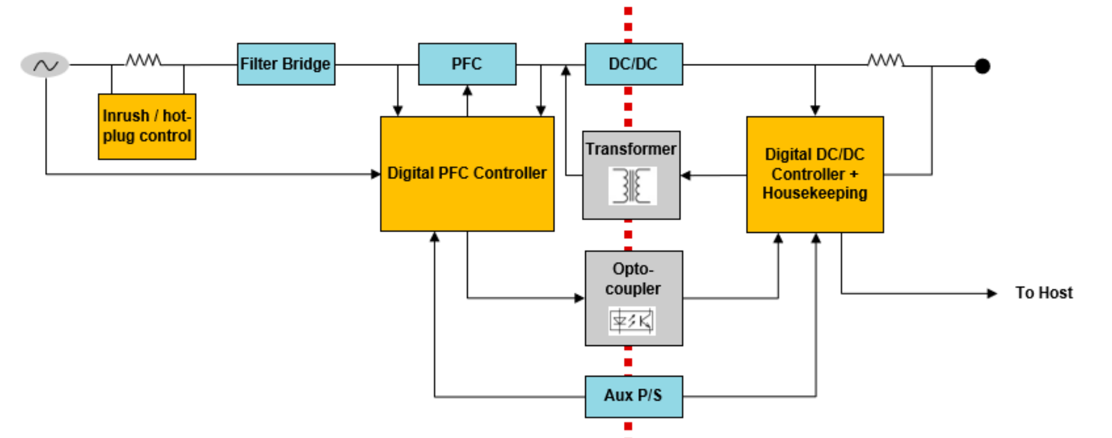
Housekeeping and system communication

- Thermal management
- Fan speed control
- Comms. With host MCU
- Enabling special operating modes (ex: light load, stand-by)
- Telemetry (P_{in}, V_{in}, I_{in}, temp)

A typical **power supply includes basic power control and system housekeeping**



Analog controlled PSU



Digital controlled PSU

Traditionally, analog controllers took care of the **basic power supply control and another MCU would take care of the housekeeping**: More components and manufacturing cost

Power supplies with digital controllers house **both functions into the same IC** and enables multi-threaded applications: One design/device, multiple PSUs

Key controller architectures in server main power stage

ANALOG

DEDICATED HARDWARE FEEDBACK

DIGITAL

DEDICATED HARDWARE & OPTIONAL PROCESSOR FEEDBACK

PROCESSOR DRIVEN FEEDBACK

Analog controllers

UCC28951
Texas Instruments

Fixed function

- Fixed function
- Simple implementation, fast time-to-market
- High PSU bandwidth
- Could use MCU for housekeeping
- Supports 1-2 topologies per controller

Hardware implemented digital power controllers

UCD3138A
Texas Instruments

Programmable, featuring an integrated MCU

- Flexible
- Minimal FW development, medium time-to-market
- No processor computation for PSU bandwidth
- Limited complex controls and housekeeping support
- Supports multiple topologies per controller

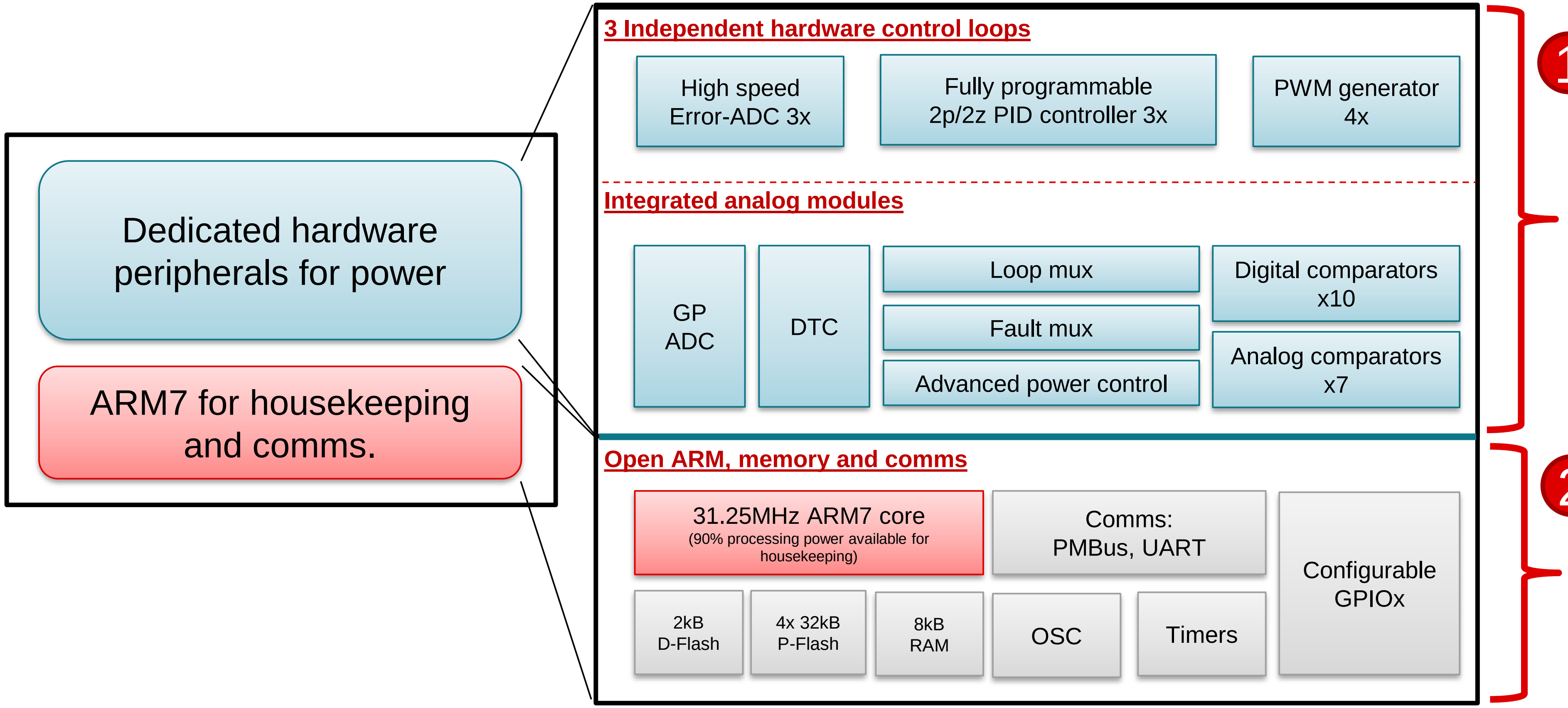
Fully software executed

C2000 MCUs
Texas Instruments

DSP/MCU based

- Very flexible
- Involved FW development, more time-to-market
- Processor computation determines PSU bandwidth
- Supports complex controls and housekeeping support
- Supports multiple topologies per controller

UCD3138A – Digital controller for server power



1 Programmable H/W-based architecture

- Executes time-critical high frequency SMPS function like V/I feedback loop with no dependence on processor
- Features H/W peripherals that support most common power supply topologies/functions

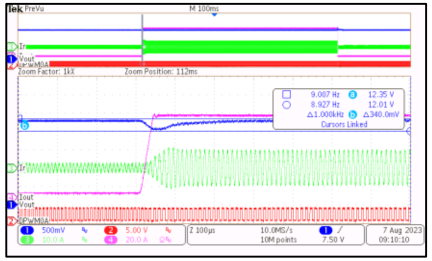
2 Programmable MCU

- GP-MCU used to configure and initialize state machine and run housekeeping, comms., and telemetry
- Can also be used for low-speed power supply control (such as PFC voltage loop, current sharing)

*Example block diagram shows UCD3138128A

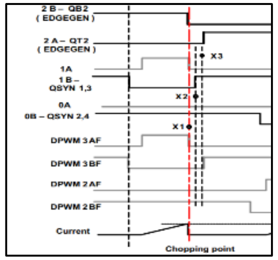
UCD3138A features specific to server power

Ultra-fast transient response



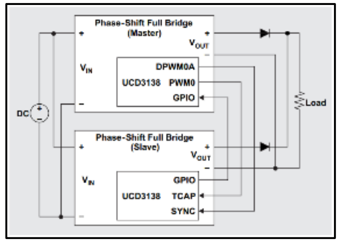
Hardware-etched peripherals → low output capacitance, smaller magnetics

Power converter fault handling



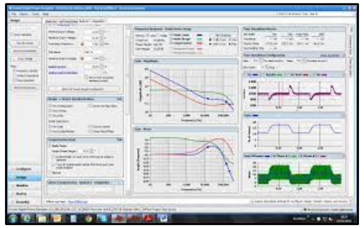
Analog/digital faults → flexibility to handle CBC or latched faults

Current sharing and synchronization



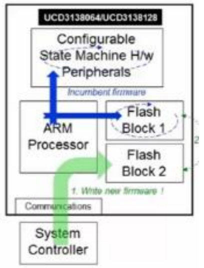
Synchronization & load sharing → modularity & superior EMI perf.

Fusion GUI for easy development



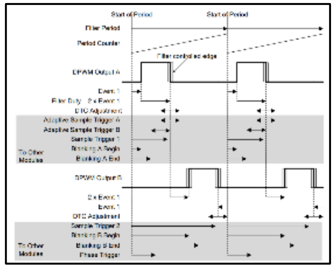
Blackbox development with GUI → faster time-to-market and superior debug capability

On-the-fly firmware upgrade



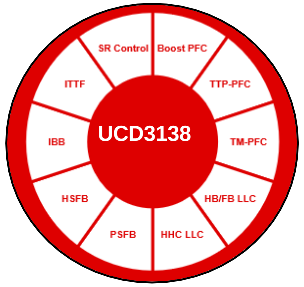
Dual memory bank architecture → zero downtime firmware update

Advanced high Res. PWMs



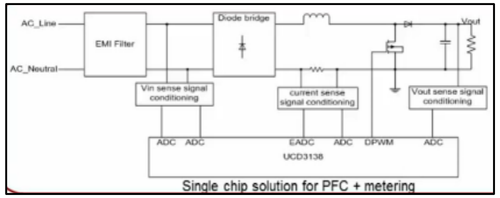
250ps resolution PWM outputs → lower output ripple

Multi-topology support



Flexible digital power controller → easy wide EE & economies of scale

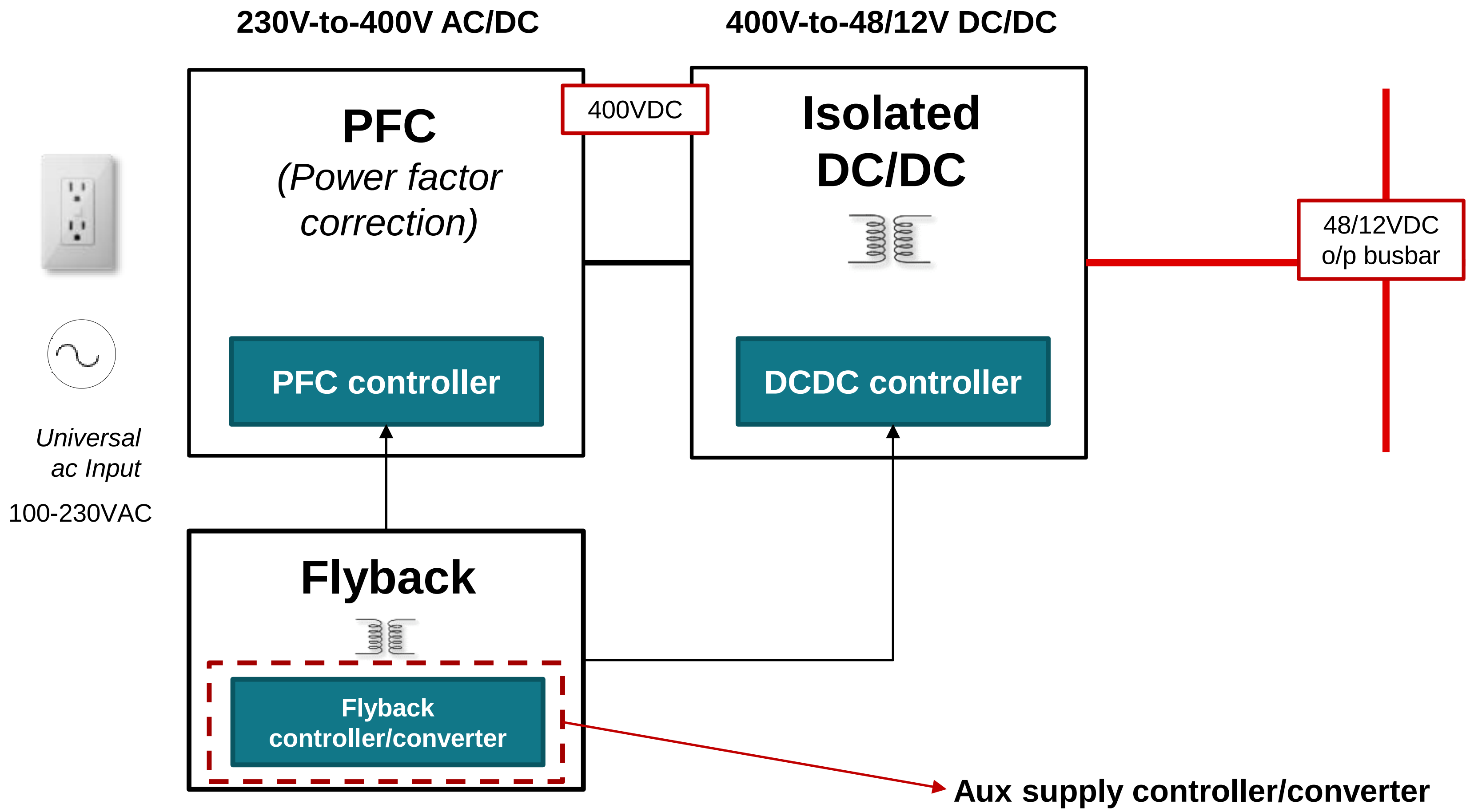
Advanced housekeeping functions



GP-ADC + Arm-MCU + Comms. → superior system integration

PID: Proportional Integrator Differentiator – a type of control method

Typical server power supply control uses individual controllers at each stage



Key aux supply concerns in server power

Increasing power density

Form factor

Increasing power density is driving smaller size & ease of design, providing space to improve thermals

Light load efficiency

Increasing efficiency requirements are the norm and aux supplies are expected to have good efficiency when in standby

Integration

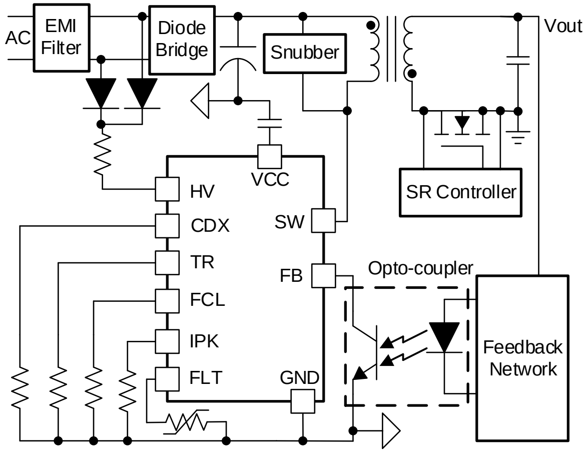
The form factor and efficiency needs are pushing the envelope for more integration – the control, the transistor and more

Future need

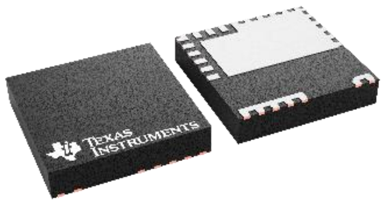
Support 3ph AC input 180V-305Vac – power transistor needs to be rated above 800V ~1.2-1.7kV

UCG28826 | TI's first GaN integrated flyback

UCG28826: Industry's first self-biasing flyback converter



- **Integrated 650-V GaN** with built-in current sense
- **Enables lowest system cost** with cutting-edge feature integration
- **Improved** efficiency, EMI, and design flexibility



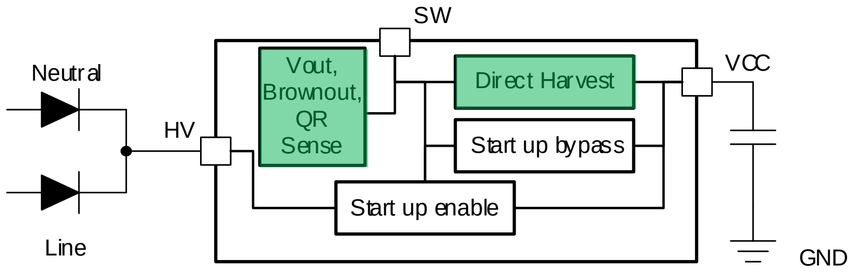
Industry-leading features for flyback converters

- Self-bias and sensing for **auxless converter design**
- Dynamic CCM/QR/DCM control law for **optimized variable-load efficiency**
- Switching slew rate control for **EMI mitigation**
- **Comprehensive protections** including OTP, OVP, OCP, OPP, Brownout, etc.
- **Leading design flexibility** including frequency clamping, fault response, etc.

Innovative self-bias & auxless-sensing scheme

Completely eliminate auxiliary winding and VCC pre-regulator

- Naturally harvest bias energy from power stage
- Direct switch-node sensing



- ✓ Higher integration
- ✓ Higher efficiency
- ✓ Smaller size
- ✓ Reduced cost
- ✓ Simplified design

Texas Instruments

UCG28826EVM-093: 65-W integrated GaN flyback converter

Available NOW

Key specifications

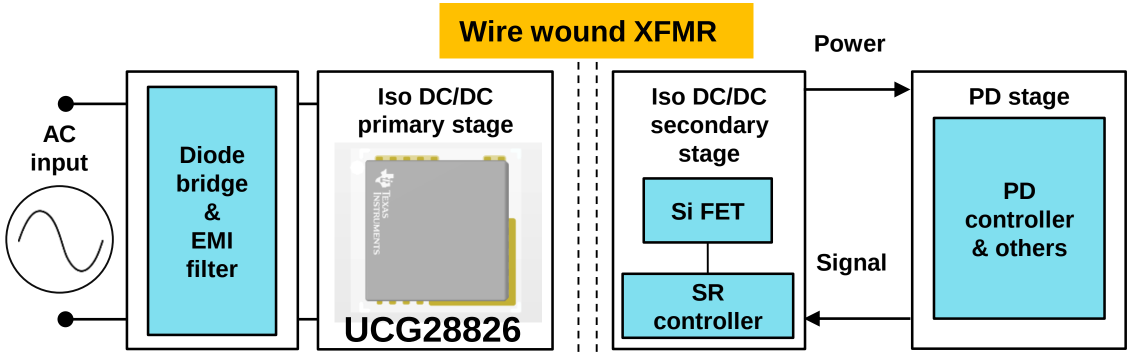
- Input voltage: 90 to 264VAC
- Max output power: 65W
- Output voltage range: 5-20Vdc
- PD output: 5V/3A, 9V/3A, 15V/3A, 20V/3.25A
- EMC compliance CISPR32B / EN55032B
- Average efficiency and standby power to meet DoE level VI and CoC Tier 2 limits
- Peak efficiency **> 94%**
- Power density: **2.84W/cm^3** without case
- Profile: **Cubicle**
- Form factor w/o case: **3.93cm x 3.45cm x 1.7cm= 23cm^3**
- Form factor w/case: **4.33cm x 3.95cm x 2.1cm = 36cm^3**

Applications

- High density PSU
- Cell phone chargers
- Notebook adapters

Benefits

- Auxless design enables lower component count, higher density
- Supports USB-PD charging protocol
- Quasi-resonant operation with adjustable valley switching function to maximize efficiency at any line and load condition
- SSR topology implementation with an opto-coupler for accurate step voltage control



For User's Guide and more: http://www.ti.com/tool/UCG28826EVM-093

Production | Samples

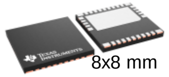
PFC/ISO device selection guide

High Voltage Device Portfolio

PFC/ISO primary device selection

<1.5KW

LMG341xR070
70mΩ / 600V

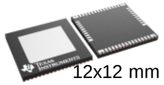

8x8 mm

LMG365x, TOLL
70mΩ/650V

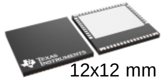

11.6x9.8 mm

1.5-2.5KW

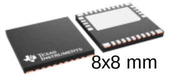
LMG352xR050
50mΩ / 650V


12x12 mm

LMG3422R050
50mΩ / 600V


12x12 mm

LMG341xR050
50mΩ / 600V


8x8 mm

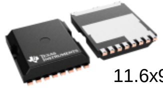
LMG352xR030
30mΩ / 650V

LMG3422R030
30mΩ / 600V

LMG365x, TOLL
35mΩ/650V

>2.5KW

LMG365x, TOLL
25mΩ/650V


11.6x9.8 mm

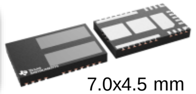
Medium Voltage Device Portfolio

ISO secondary device selection

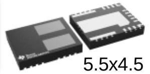
48V

Integrated Half - Bridge

LMG2100R026
HB 2.6mΩ / 100V


7.0x4.5 mm

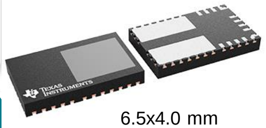
LMG2100R044
HB 4.4mΩ / 100V


5.5x4.5 mm

Integrated Single-FET

LMG3100R017
1.7mΩ / 100V

LMG3100R044
4.4mΩ / 100V


6.5x4.0 mm

Controller selection

Main power stage

UCD3138A (40/64/80p)
3HS loops, 8 DPWMs, 450ns latency, ARM7TDMi, 31.25MHz, upto 128k dual bank flash,
2k D-flash, 8k RAM, upto 43 GPIOs, 15 ADCs

TMS320F28003x
32bit DSP core @ 120MHz
384KB (192KW) of flash (ECC-protected)
69KB (34.5KW) of RAM (ECC-protected)
16 ePWM channels w/ 8 channels having high-res capability (150-ps resolution)

Aux supply

UCG28826x
65W (45/120W), SSR, HVSU, GaN-integrated

UCC28742
SSR, high eff., 1% o/p regulation

UCC28740
SSR, CVCC, HVSU, 100kHz max.

UCC28730
PSR, CVCC, wake up monitor

All samples and associated reference designs / EVMs available on ti.com; click on a device name to be redirected.