Application Report
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Migrating From the TMS320C203, TMS320LC203 or TMS320F206 to the TMS320LC206/TMS320C206

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Abstract

This document discusses the process needed to migrate applications from the Texas Instruments (TI™) TMS320C203, TMS320LC203 or TMS320F206 to the TMS320LC206/TMS320C206 digital signal processor (DSP).

Design Problem

How do I migrate from the TMS320C203, TMS320LC203 or TMS320F206 to the TMS320LC206/TMS320C206?

Solution

Understand the differences among the ‘20x DSP devices before designing the migration plan. The following sections of this document cover most of the differences within the ‘20x DSP devices, ‘C/’LC203, ‘F206, ‘C206/’LC206. (Refer to the individual IC data sheets for details.)

- ❒ Device configuration pins
- ❒ Power supply pins
- ❒ Reset circuit
- ❒ Memory interface
- ❒ Peripherals

Device Configuration Pins

Three device configuration pins are different between the ‘203/’F206 and the ‘C/’LC206. Table 1 provides the pin differences.

Table 1. Device-Specific Pin-outs

Pin	'C203	'LC203	'F206	'LC206	'C206
1	*TEST*	*TEST*	*TEST*	*EXT8*	*EXT8*
2	$\overline{BOOT}$	$\overline{BOOT}$	$MP / \overline{MC}$	$MP / \overline{MC}$	$MP / \overline{MC}$
10	*PLL5V*	*PLL5V*	*PLL5V*	$\overline{PLLRS}$	$\overline{PLLRS}$

Pin 1: This is the TEST pin in the '203 and 'F206 devices. It is connected to V_{ss} for normal operation. On the 'C/'LC206, input status of the pin (EXT8) is used by the on-chip bootloader to determine the type of bootloading. If this pin is tied low, the 'C203 style bootloader (using 8-bit external EPROM) is used. If it is tied high, the enhanced 'C206 bootloader is used. This pin is sampled at reset and its level is stored in bit 3 (LEVEXT8) of the PMST register. To remain compatible with the '203, this pin should be tied low. Note that the on-chip bootloader is available in standard 'C/'LC206 parts only. For custom 'C/'LC206 devices, the usage of this pin (and hence the bit) is dependant on customer application.

Pin 2: On the '203 device, this is the BOOT pin. When held low during reset, this pin enables transfer of code from external global data memory for bootloading. On the 'F206 and 'C/'LC206 devices, the functionality of this pin has been changed to microprocessor or microcontroller select (MP/MC). When held low, this pin enables access of on-chip program memory. On the 'F206, this pin, when held low, accesses the on-chip Flash in program space. On the 'C/'LC206, this pin, when held low, accesses the on-chip ROM in program space. If this pin is held high, the processor executes from off-chip memory. At reset, the processor accesses the internal program memory or external program memory depending on the condition of this pin.

Pin 10: This pin is tied high or low for the '203 device depending on whether the device is operating on 5 V or 3.3 V. This pin is always tied high in the 'F206 device. On the 'C/'LC206, this pin resets the on-chip PLL circuit. Three different reset configurations are possible for 'C/'LC206 devices.

Power Supply Pins

The 'C203 and 'F206 devices operate with a single supply voltage of 5 V. The 'LC203 and 'LC206 devices operate with a single supply voltage of 3.3 V. The 'C206 device requires dual supply, 3.3 V for the core and 5 V for the I/O.

Table 2 outlines the power supply details for all devices in the '20x family (V_{dd5} = 5 V, V_{dd3} = 3.3 V).

Table 2. Power Pin Assignment Across Devices

Pin	'C203	'LC203	'F206	'LC206	'C206
4	V_{dd5}	v_{dd3}	V_{dd5}	v_{dd3}	v_{dd3}
7	V_{dd5}	v_{dd3}	V_{dd5}	v_{dd3}	V_{dd5}
11	V_{dd5}	v_{dd3}	V_{dd5}	v_{dd3}	v_{dd3}
16	V_{dd5}	v_{dd3}	V_{dd5}	v_{dd3}	V_{dd5}
35	V_{dd5}	v_{dd3}	V_{dd5}	v_{dd3}	V_{dd5}
50	V_{dd5}	v_{dd3}	V_{dd5}	v_{dd3}	V_{dd5}
63	V_{dd5}	v_{dd3}	V_{dd5}	v_{dd3}	V_{dd5}

Pin	'C203	'LC203	'F206	'LC206	'C206
75	V_{dd5}	v_{dd3}	V_{dd5}	v_{dd3}	v_{dd3}
91	V_{dd5}	v_{dd3}	V_{dd5}	v_{dd3}	V_{dd5}

TMS320C206/LC206 Reset and PLL Lock Conditions

The 'C/'LC206 devices have special reset conditions compared to '203 and 'F206 devices, as the PLL needs to be reset in addition to the core. The PLL lock-up time is also higher in the case of 'C/'LC206 devices (5000 clock cycles) compared to '203 and 'F206 devices (2500 cycles). Table 3 (applicable to case A) explains the reset conditions for 'C/LC206 devices. Typical reset setups are explained in the following three cases.

Table 3. '206 Reset Configuration

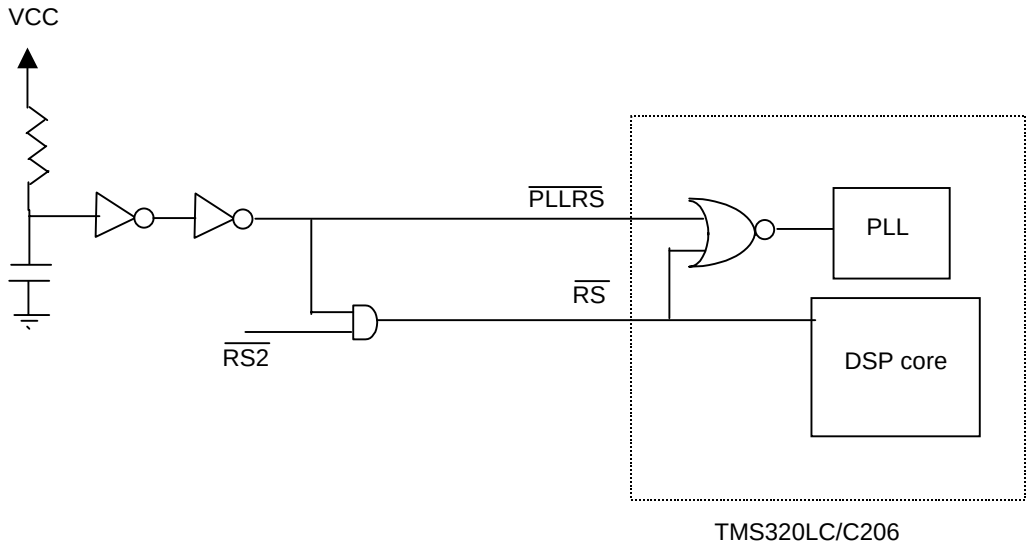
CONDITION	$\overline{\text{PLLRS}}$	$\overline{\text{RS2}}$	$\overline{\text{RS}}$	PLL[2]	DSP Core
Power on reset (POR)	0	X [3]	0	Reset	Reset
After POR	Always 1	1	1	No	No
After POR	Always 1	0	0	No	Reset

Notes: 1) The PLL can be reset only along with the core.
2) PLL-reset means PLL resets and initiates locking sequence.
3) X = Don't care

Case A

The following circuit will initiate PLL and DSP core reset at power-up. After power-up, reset pulses on $\overline{RS2}$ (e.g., watchdog timer) will reset the DSP core only. The PLL will not be reset, as $\overline{PLLRS}$ remains inactive (high) while $\overline{RS2}$ is active low. This scheme will keep CLKOUT1 locked for all resets except for power-on reset.

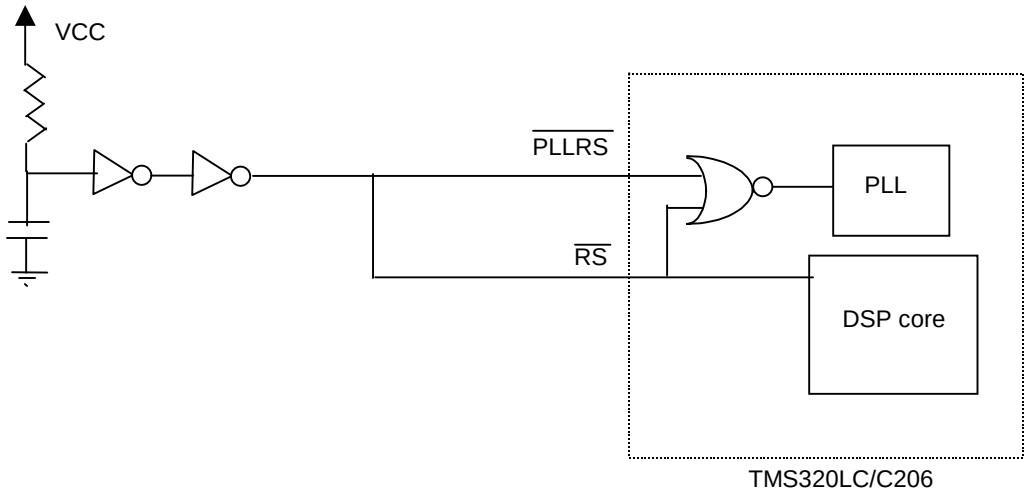
Figure 1. Case A



Case B

The following circuit will initiate PLL-reset and DSP-core-reset for every reset. Following every reset, the PLL will initiate PLL locking sequence, as $\overline{PLLRS}$ is low during reset.

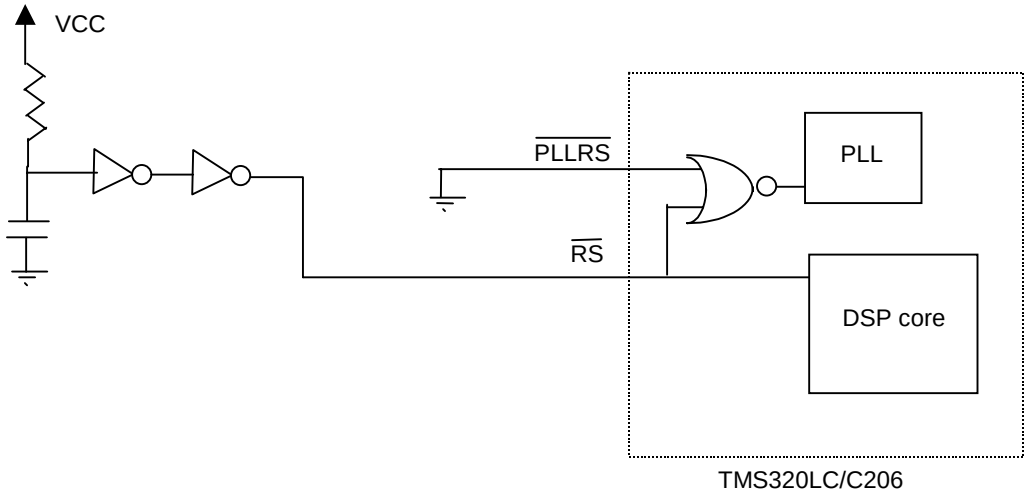
Figure 2. Case B



Case C

The circuit shown below is equivalent to case B. PLL and DSP core will be reset for each reset. PLL will initiate locking sequence for every reset, as $\overline{PLLRS}$ is low during reset.

Figure 3. Case C



Memory Interface

The ‘read-enable’ (or ‘output-enable)’ signal (pin 45 – RD) is programmable in the ‘F206/’C206/’LC206 devices. The functionality of this pin is defined by the FRDN bit (bit 15) of the PMST register. Pin 45 outputs the ‘read-enable’ signal (RD) from the core when FRDN = 0. This is the condition at reset. When FRDN = 1, Pin 45 outputs the inverted R/W signal from the core. This selection is useful to design zero-wait-state external memory interfaces at 40-MHz operation. ‘203 devices do not have this feature.

Since different fabrication processes are employed for devices in the ‘20x family, there may be minor variations in timings. Texas Instruments recommends that the customer refer to the relevant datasheets for timing variations. See the References section at the end of this document for the literature numbers of the data sheets for the DSPs discussed in this document.

Peripheral Enhancements

The ‘Synchronous Serial Port’ (SSP) is available as a standard peripheral in all the devices of the ‘20x family. The ‘Enhanced Synchronous Serial Port’ (ESSP) is available only in ‘F206/’C206/’LC206 devices. The ESSP offers several enhancements over the SSP and also has several new features. ESSP features are upward compatible to the standard SSP. Table 4 describes the additional registers used to enable ESSP features and also the PMST register described in the previous section.

Table 4. Additional Registers In F206/C206/LC206 Devices

Name	Description	I/O Address
SSPST	ESSP Status register	FFF2h
SSPMC	ESSP Multi-channel register	FFF3h
SSPCT	ESSP Count register	FFFBh
PMST	Processor mode status register	FFE4h

References

TMS320C203, TMS320C209, TMS320LC203 Digital Signal Processors, Literature number SPRS025B

TMS320F206 Digital Signal Processor, Literature number SPRS050A

TMS320C206, TMS320LC206 Digital Signal Processors, Literature number SPRS065B)

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