TMS320 DSP
DESIGNER'S NOTEBOOK

TMS320C5x Interrupts

APPLICATION BRIEF: SPRA217

Jeff Beinar and Mansoor Chishtie
Digital Signal Processing Products
Semiconductor Group

Texas Instruments
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CONTACT INFORMATION

US TMS320 HOTLINE	(281) 274-2320
US TMS320 FAX	(281) 274-2324
US TMS320 BBS	(281) 274-2323
US TMS320 email	dsph@ti.com

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TMS320C5x Interrupts

Abstract

This document discusses how the RETE instruction works when another interrupt is pending.

Design Problem

How does the RETE instruction work when another interrupt is pending?

Solution

Let's assume that we are in an Interrupt Service Routine and that an external interrupt occurs which is low for three cycles thereby setting the appropriate bit in the IFR on the next cycle. However, since we are in the ISR, INTM = 1, globally disabling the next interrupt from being recognized. The last instruction in the ISR is a RETE.

If there is a pending interrupt in IFR when RETE is executed then 'C5x will immediately jump to the pending ISR without going back to the interrupted code.

Table 1. RETE Instruction Cycle When an Interrupt is Pending

		← interrupt occurs while in Interrupt Service Routine									
Cycle	0	1	2	3	4	5	6	7	8	9	10
Fetch	ISR1	ISR2	ISR3	RETE	D	D	D	I6	I7		
Decode	--	ISR1	ISR2	ISR3	RETE	D	D	D	INTR		
Read	--	--	ISR1	ISR2	ISR3	RETE	D	D	D	INTR	
Execute	--	--	--	ISR1	ISR2	ISR3	RETE	D	D	D	INTR
INTM	1	1	1	1	1	1	1	0	0	0	

- RETE changes INTM at the end of execute phase.
- INTM becomes active in cycle 7, that will make interrupt jammed on next cycle in the decode phase.
- I6 and I7 in Figure 1 will be fetched again when the 'C5x returns from the interrupt.
- D refers to "Dummy Cycle."