Miniature Packages for Portable Applications - Silicon DustE? in Portable Systems

Literature Number: SNOA844

Technology Edge

This paper was presented at the International IC-China Conference & Exhibition 2001
March 26-27, Shanghai; March 29-30; Beijing, April 2-3, Shenzhen

Miniature Packages for Portable Applications - Silicon Dustä in Portable Systems

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Often driven by the conflicting design goals of *Better, Faster and Smaller* , design engineers face tough challenges in creating new products. Consumers want longer battery life, smaller products (although including additional features), that are less expensive than previous generations. For the end-product manufacturers these characteristics become low power (longer battery life), lightweight, compact solutions (integrated or small footprint) easy to manufacture in the current environment. These requirements then are translated from the end product to the components. Leadless leadframe packages, LLP, and micro SMD offer a solution to these issues in portable applications.

Lower system supply voltage requirements enabled the shift from bipolar to BiCMOS and CMOS for analog designers. The shrinking dimensions of BiCMOS and CMOS process technologies shifted the balance between a pad-limited design and a core-limited design. The geometry rules on pad design have not changed as dramatically as the design rules for gate and interconnect geometries. Depending on the process used, a smaller footprint does not always offer the most cost-effective solution. If the die must grow to fit the pads around the parameter, using JEDEC standard pad pitch, that is not an effective use of silicon. Small packages are not necessarily one size fits all . National Semiconductor has developed and offers a variety of packages such as the leadless leadframe package, LLP, and chip scale micro SMD that optimize the equation of footprint and cost while keeping in mind the designer s goal of performance, ease-of-use and cost of manufacturing. Figure 1 shows an example of the footprint area of the MSOP-8, LLP-16, and the micro SMD-8. All devices shown are surface mount devices that can be assembled on printed circuit boards using conventional manufacturing techniques in common usage.

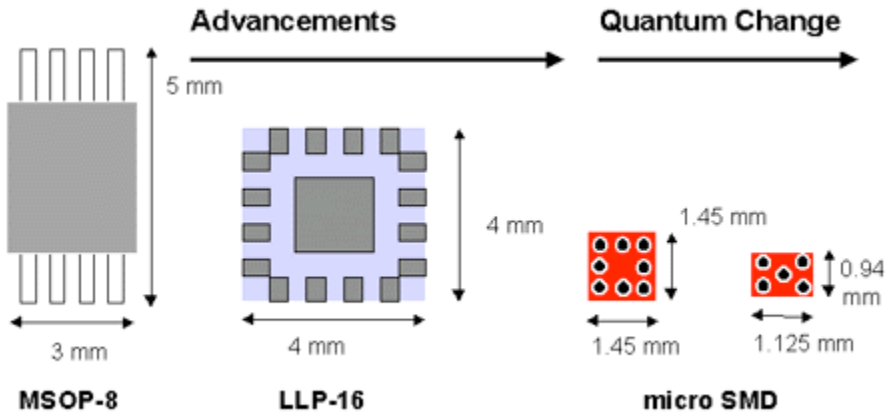

Figure 1. Quantum Change in Footprint Size

System designers care about reduced footprint and thinner profile, not just reduced package size. The goal is for the entire product to have a smaller size than previous generations. By considering the need to shrink the entire package, a smaller volume of used area, the demand for thinner packages have multiplied. Figure 2 highlights the shrinking profile of surface mount packaging technologies. As supply voltages decrease and package volumes evaporate, more systems have become portable applications.

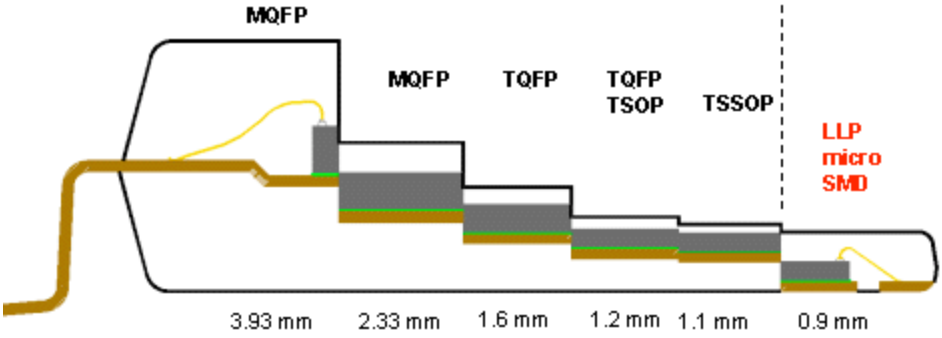

Figure 2. Surface Mount Package Profile Comparison

The two dominant trends in packaging technology have been increasing the pin count and reducing the package size. For the past three decades the most visible change in packaging has been the increasing pin count required by the integration of functions. Examples include Quad Flat Packs (QFP) and Ball Grid Arrays (BGA) with pin counts in the 100s. Reducing the package size, or miniaturization, has been an unexpected development of the move to lower system voltages (<5.0V) and the constraints in footprint driven by the dominance of consumer portable products. The best-known example of this is the SOT package. SOTs (Surface Mount Technology), initially developed for discrete components, found a strong partner with the new generation of analog and linear ICs. Three to eight pins comprise over 85% of analog functions. 90% of analog functions have 28 pins or less. Miniaturization of packaging has created a new design methodology (which enables optimizing all aspects of the system design) of breaking up functions that previously were slated for integration. At National Semiconductor we call this dis-integration . The next leap in miniaturizing packaging came when the package assembly process was examined and the traditional wirebond and leadframe methodology were discarded. This led to the break-though in surface mount packaging, micro SMD. Bumps, directly placed on the surface of the die, provide the interconnect between the die and the PC board. Surface mount packaging went from incremental improvements to quantum change. Device footprints were dramatically reduced.

Describing the LLP

The leadless leadframe package, LLP, is a leadframe based chip scale package. While maintaining a pad pitch of 0.5mm, a greater pin count to die area can be supported with LLP. Using LLP, the number of pins can be increased without increasing the die area. Similar to the micro SMD, the LLP has a reduced thermal resistance, reduced package height and mass and reduced board space.

For pincounts less than forty-four pins all contacts are located around the periphery of the package. For devices of fourteen pins and less, the pinout configuration used in the LLP is dual-in-line. With a standard pad pitch of 0.5mm, the package size increases in 0.5mm increments. For functions with greater than fourteen pins a quad configuration is used. To improve solder joint reliability, a pad pitch of 1.0mm is used for these larger devices. The exposed die attach pad can be soldered to the board to provide superior thermal performance, enhanced solder joint reliability and improved package self-alignment during reflow. All pins are eutectic solder for simpler printed circuit board placement. These pins, or contacts, are flush with the bottom of the LLP so coplanarity is never an issue.

Describing the micro SMD

Micro SMD is a chip scale package. An eutectic solder bump, which is masked unto the die at the wafer level, is the interconnect between the die and the PCB. Like the LLP the bumps of the micro SMD are located around the periphery die with a pad pitch that conforms to JEDEC MO-211 of 0.5mm. The manufacturing process steps include standard wafer fabrication, a second passivation layer, deposition of eutectic solder bumps on I/O pads, application of a proprietary protective backcoating, standard wafer testing, laser marking, singulation, and shipping in tape and reel. The package is applied at the wafer-level before individual chips are separated. IC functionally is tested only once. A list of available parts from NSC can be found at www.national.com/appinfo

/microsmd/

Micro SMD extends the flip chip packaging technology to standard surface mount technology, and does not require underfill. Using standard surface mount assembly technology the micro SMD has the smallest footprint per I/O. With the smallest footprint currently available, the 4-bump micro SMD has a total surface area of roughly $0.8mm^2$.

Thermal Performance and Heat Dissipation

Small size does not imply reduced or relaxed performance parameters. The miniature size of the micro SMD often provokes the question about thermal performance. The micro SMD-8 has a q_{JA} of 220° C/W. This performance is on par with the SOT23-5, which has a q_{JA} of 265° C/W, and is clearly superior to the thermal performance of the SC70-5, which has a q_{JA} = 478° C/W. This lower q_{JA} enables superior electrical performance in devices thermally limited by the amount of power they drive such as Low Dropout Regulators (LDOs) and Audio Amplifiers. Figure 3 shows the theta ja (q_{ja})of a variety of packages.

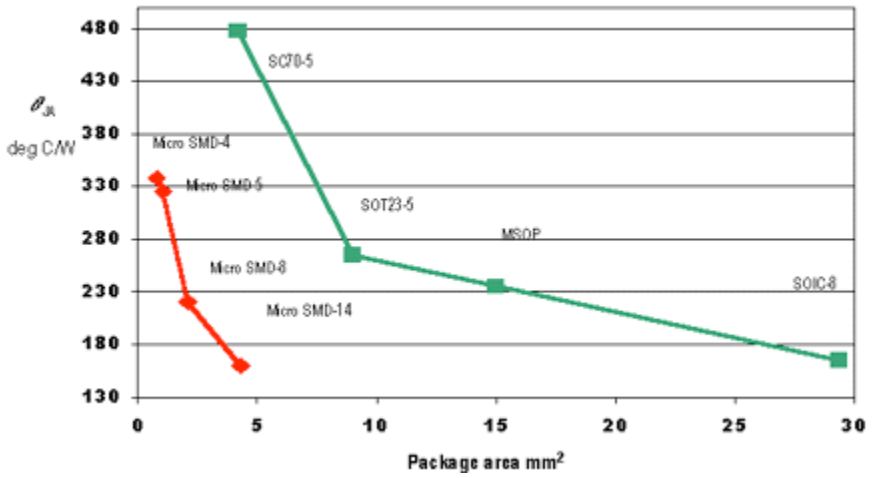

Figure 3. q_{JA} of Various Packages by Footprint Sizes. Heat dissipation of the micro SMD is on par with the SOT23, the dominant package in portable communications.

Soldering the exposed die attach pad (DAP) lowers the q_{JA} of the LLP even further to 33° C/W. This is on par with the TO-92, which has a q_{JA} of 45° C/W. With a q_{JA} so low the LLP can be used with higher supply voltages with no no degradation in system performance. Figure 4 shows the q_{JA} of the LLP-16 compared to the TSSOP-16. To get the optimal thermal performance a copper LLP thermal land matching the dimensions of the DAP should be located directly under it. In high power applications with devices of <14 pins a dog bone shape enhances thermal performance. Thermal vias conduct heat from the surface of the PCB to the ground plane. Vias are typically placed in a grid pattern. The vias should be plugged to avoid solder wicking during assembly. If copper plating cannot plug the vias, the thermal vias can be tented with the solder mask on the PCB top layer. A void in the solder paste will have a negative affect on heat dissipation. The effect is minimal and does not affect reliability of solder joint integrity unless the void is greater than 25% of the corresponding volume.

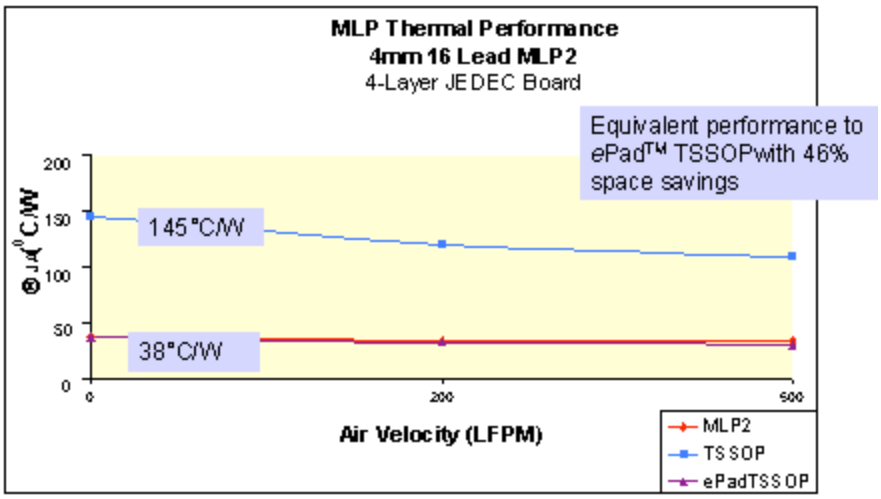

Figure 4. θ_{JA} LLP vs TSSOP

There are three ways to dissipate heat conduction, convection and radiation. With heatsinks, large leadframes and heavy gauge wirebond, example TO-92, most heat is transferred off of the die through conduction. In tiny packages such as the SC70-5 most heat transfer is through natural convection off of the die as the leadframe and wirebond is too thin to handle much heat transfer through conduction. Most portable applications are closed environments without fans, liquid cooled air, etc. The active side of the micro SMD is bonded down to the PC board and the heat is transferred conductively from the die through the bumps to the PC board. Conduction is much more efficient than convection in transferring heat.

Similarities between the LLP and micro SMD
Like the micro SMD the LLP has a moisture sensitivity level of 1. An MSL of 1 makes both of these packages hermetic. That means they do not absorb any moisture and therefore do not need bake, dry pack or nitrogen storage. This greatly simplifies handling and board manufacturing.

Both the LLP and the micro SMD are shipped in standard polycarbonate conductive carrier tape with pressure sensitive adhesive cover tape. Both 7" and 13" reels are available.

Standard pick and place equipment with an accuracy of ± 0.05mm can place micro SMD and LLP. Device recognition is achieved through package silhouette or locating individual bumps on the interconnect pattern. Bump location is more accurate method but can be a more expensive solution and slower. Either method works since both micro SMD and LLP benefits from self-alignment during reflow.

Without any special considerations LLP and micro SMD can be assembled using standard IR / IR convection surface mount technique reflow processes. If using no-clean fluxes nitrogen purge is recommended.

Summary
Micro SMD and LLP are true chip scale packages that provide the smallest possible footprint without putting the device on its side. Offering excellent package robustness, high assembly yield, and superior electrical performance we believe that the future trend in surface mount packaging for analog components is addressed by micro SMD and LLP.

As process geometries and system supply voltages continue to decrease, more devices will change over to miniature packages. Integration will not vacuum all of the silicon in a system into one chip. Similar functions will continue to be integrated but where it makes sense dis-integration, in miniature packages that do not require special handling, will increase the flexibility of the end-system. Driven by the explosive growth in portable consumer applications the opportunities afforded by offering smaller devices expand daily. Micro SMD is an ideal

package for low pincount analog functions such as operational amplifiers, regulators, references, converters, and temperature sensors. LLP answers the need for improved thermal performance and bridges the gap in pin count to die area. Between LLP and micro SMD the most cost-effective package miniaturization solution for portable and hand-held products is available

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