Application Note

DP83867 Troubleshooting Guide

ABSTRACT

The DP83867 is a robust, low power, fully featured Physical Layer transceiver. This application note was created to help troubleshoot the DP83867 and to show what to look at in the event that the PHY is not working as intended.

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1 DP83867 Application Overview

The DP83867 is a robust, low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support the 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols.

Figure 1-1 is a high-level system block diagram of a typical DP83867 application.

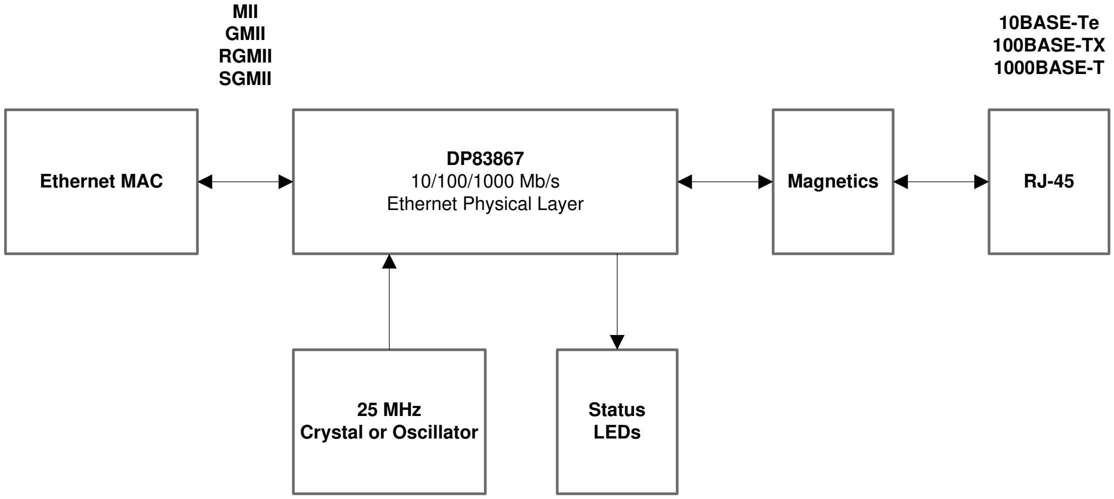

Figure 1-1. DP83867 Block Diagram

The DP83867 can connect to an Ethernet MAC and to a media. The connection to the media is via a transformer and a connector.

Table 1-1. DP83867 Configurations

DP83867 Version	MAC interface	Pin number/ package
DP83867IR/CR/IS/CS/E	RGMII	48 pins / QFN package
DP83867IS/CS/E	SGMII	48 pins/ QFN package
DP83867IRPAPR	MII/GMII/RGMII	64 pins / QFP package

2 Troubleshooting the Application

The following sections approach the debug from a high level, attempting to start with application characteristics that have a broad impact and then zeroing in on more focused aspects of the design.

2.1 Schematic and Layout Checklist

The DP83867 Schematic Checklist and DP8386X Layout Checklist compile the best practices for designing with DP83867 into an easy-to-use document. The recommendation is to go through these documents for a detailed description what connections and components are needed for the PHY to work.

The following sections can present expected behaviors if the PHY is powered and initialized correctly. Any deviations from expected behaviors can point to errors due to incorrect peripheral circuity.

2.2 Device Health Checks

This section dives into device health checks which makes sure the device is powered and initialized correctly. This section can be skipped if DP83867 is:

- Linking up (LED indication or register status) when connected to link partner or showing FLP signals when Ethernet cable is disconnected
- Responding to register access (if applicable)

2.2.1 Voltage Checks

DP83867 needs to have sufficient power as well as

- One 10nF, and one 10uF decoupling per rail
- One 100nF, and one 1uF decoupling per pin

The DP83867 supports the two configurations for power supplies shown in Figure 2-1 and Figure 2-2.

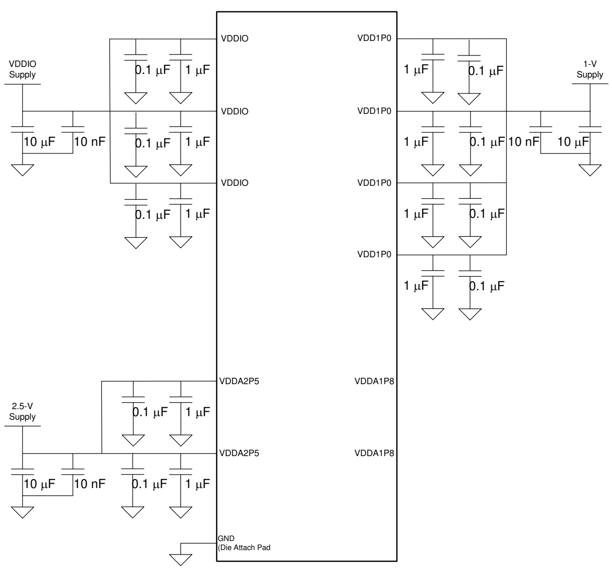

Figure 2-1. Two Supply Configuration

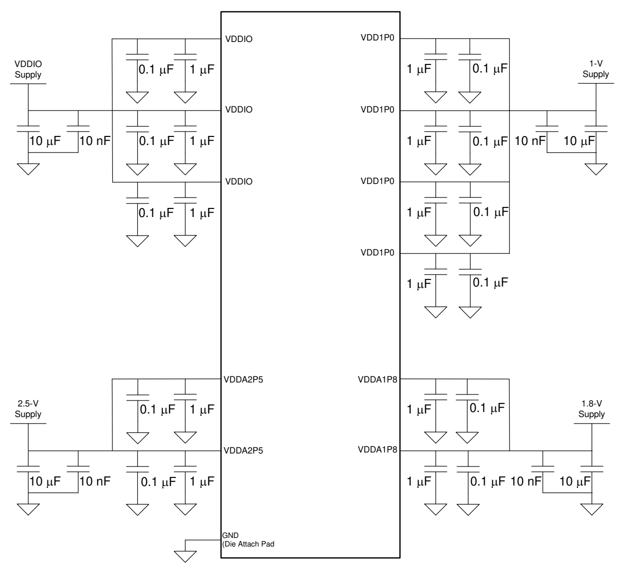

Figure 2-2. Three Supply Configuration

When operating in three-supply configuration, VDDA1P8 must be stable within 25ms of VDDA2P5 ramping up. Make sure to supply VDDIO1P8 after VDDA2V5.

- When powering down the DP83867, VDDA1P8 needs to be brought down before VDDA2P5.

Power up the device and verify the sequence of these supplies with an oscilloscope. Perform DC measurements of the supplies as close to the pin as possible. Confirm that each measurement is within the limits defined below.

Table 2-1. Recommended Operating Conditions

	Min(V)	Typ(V)	Max(V)
VDDIO (1.8V)	1.71	1.8	1.89
VDDIO (2.5V)	2.375	2.5	2.625
VDDIO (3.3V)	3.15	3.3	3.45
VDD1P1 (PAP)	1.045	1.1	1.155
VDD1P0 (RGZ)	0.95	1	1.155
VDDA1P8	1.71	1.8	1.89
VDDA2P5	2.375	2.5	2.625

2.2.2 Probe the RESET_N Signal

The reset input is active low. This pin has a weak internal pull-up resistor to provide a default state if left unconnected or not driven externally.

Confirm that the controller is not driving the RESET_N signal low. Otherwise, the device will be held in reset and does not respond.

2.2.3 Probe RBIAS

The RBIAS pin is used to set the internal reference current within the DP83869. RBIAS should be a 11kΩ resistor with a 1% tolerance. The preference is to have a single component over multiple in series as the tolerance range can increase.

If properly powered, a 1V signal will appear when probing the RBIAS pin.

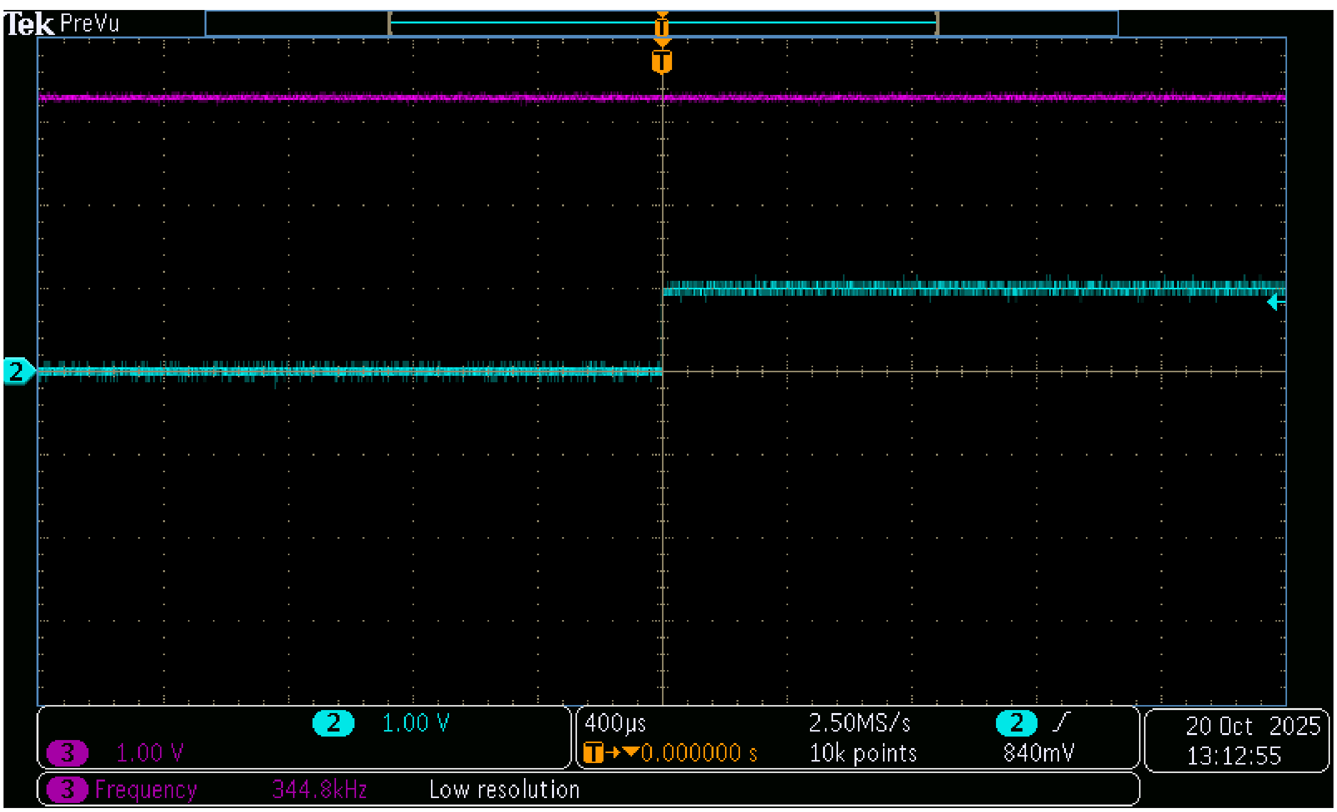

Figure 2-3. RBIAS Voltage (Blue) and VDDIO (Purple)

2.2.4 Probe the XI Clock

The following guidelines are the main specifications to reference for compatible input clocks

Table 2-2. 25MHz Crystal Specifications

Parameter	Min	Typ	Max	Unit
Frequency		25		MHz
Frequency Tolerance	-50		50	ppm

Probing on the crystal nodes can change the capacitive loading and therefore change the operational frequency. If using a crystal as the clock source, probe the CLK_OUT signal. The default signal on CLK_OUT is a buffered version of the XI reference and provides a representative measurement.

Table 2-3. 25MHz Oscillator Specifications

Parameter	Min	Typ	Max	Unit
Frequency		25		MHz
Frequency Tolerance	-50		50	ppm
Rise or Fall Time			5	ns
Symmetry	40		60	%
Jitter RMS			11	ps

For a 1.8V clock source, XI can be tied directly to the clock source. For a 3.3V or 2.5V clock source, a capacitive divider should be used between the clock source and the XI pin to meet the XI pin specification recommended operating conditions.

Note

For more information on designing with a crystal network, please refer to the Selection and specification of crystals for Texas Instruments Ethernet physical layer transceivers, application note.

2.2.5 Probe the Strap Pins During Initialization

The DP83867 has strap pins for configuring the device in a predetermined mode. The voltage at these strap pins determines which mode the DP83867 can operate in.

On initialization, the external strap network along with the internal resistor creates a voltage divider that the PHY samples. No other component on the line should affect the DC bias set by this network.

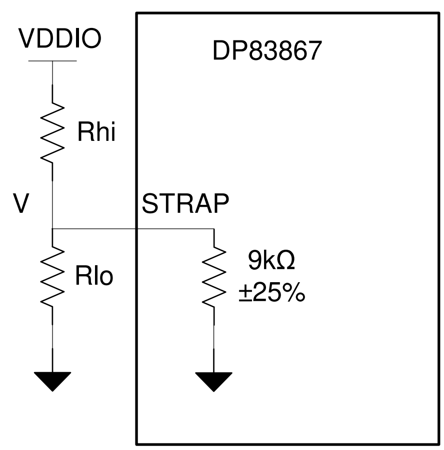

Figure 2-4. DP83867 Strap Circuit

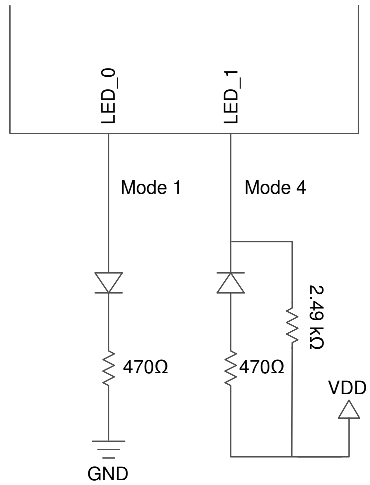

Figure 2-5. DP83867 LED Strap Circuit

In some cases, other devices on the board (for example, the MAC) will drive the strap pins unexpectedly. The strap values can be read from register 0x006E (STRAP_STS1) and 0x006F (STRAP_STS2). If there is power cycle dependency to an issue, the strapping may be marginal and can be observed cycle to cycle against this register to determine if the PHY is strapped in an unintended state.

Measurements can be made during power up and after power up when the RESET_N signal is asserted.

Note

Registers 0x6E and 0x6F are extended registers and cannot be accessed directly. Please reference Section 4.1

2.2.6 Probe the Serial Management Interface (MDC, MDIO)

The Serial Management Interface (SMI) can be useful in providing status fields during a debug. Make sure the MDIO line has a pull up resistor to VDDIO as this pin is an open-drain to the PHY. When idle, the voltage needs to be VDDIO. Make sure the SMI access uses the following sequence:

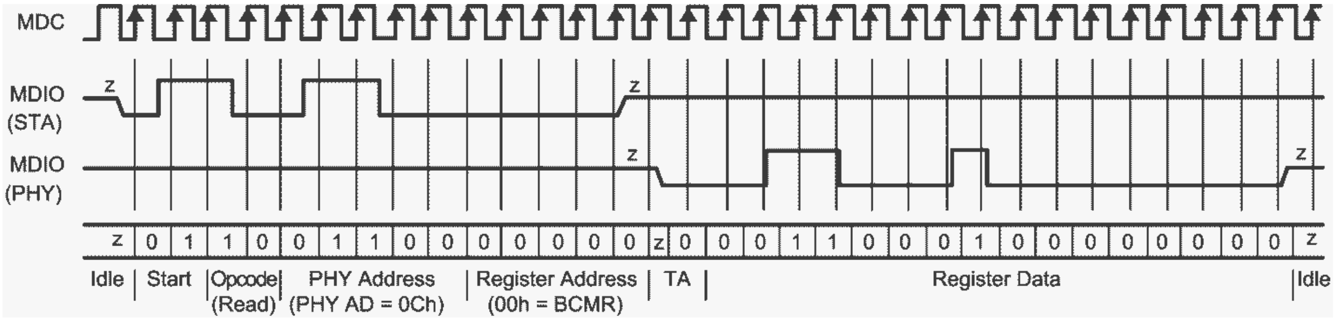

Figure 2-6. SMI Read Operation

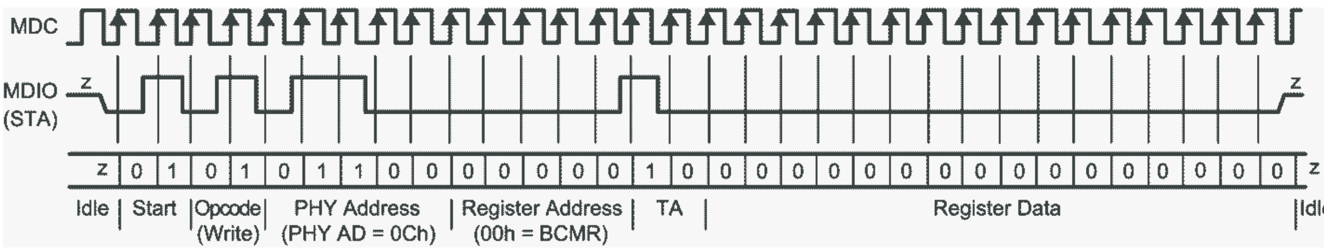

Figure 2-7. SMI Write Operation

Confirm the processor and PHY have the same SMI I/O voltage. It can be helpful to use a Logic Analyzer to debug MDIO communication.

2.2.6.1 Read and Check Register Values

Read the registers and verify the default values shown in the data sheet. Note that the initial values of some registers can vary based on strap options. An example of expected register values for PHY operation and link in 100/1000Mbps with auto-negotiation are shown in Table 2-5

The expected register values for PHY operation and link in 1000 Mbps with auto-negotiation enabled are shown in Table 2-4.

Table 2-4. DP83867 Register Value References

Register Address	Register Value		Comments
	100Mbps	1000Mbps	
0x0000	1140	1140	Auto-negotiation enabled
0x0001	796D	796D	Link established
0x0004	01E1	01E1	DUT 10/100Mbps advertisement
0x0009	0000	0300	1000Mbps advertisement
0x0011	6C02	BF02	PHY Status

Example: After powering and linking the PHY in 1000Mbps, Reg 0x11 contains the value BF02. This confirms:

- 1000Mbps Mode
- Full-Duplex
- Auto-Negotiation is complete
- Link Established

Example: After powering and linking the PHY in 10 Mbps, register 0x1 contains the value 0x7969. In this case, bit[2] is low, while the expected value is high. Bit[2] of register 0x1 corresponds to link status, so it is known that the PHY is not linked.

If register access is not readily available, a USB-2-MDIO GUI is available from TI and can be used with an MSP430F5529™ Launchpad, purchasable through the TI eStore. The GUI supports reading and writing registers, running script files, and can be used with the DP83869HM and the other devices in TI's Ethernet portfolio. The USB-2-MDIO User's Guide and GUI are available for download.

2.3 MDI Health Checks

This section dives into device health checks which makes sure that the device's MDI section is operating properly. This section can be skipped if DP83867 is linked up and reporting no errors on Reg 0x15 when sending traffic through the device.

2.3.1 Magnetics

The following guidelines are the main specifications to reference for compatible magnetics:

Table 2-5. Magnetic Isolation Requirements

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turns Ratio	±2% Tolerance	1:1	-
Open Circuit Inductance	-	320 to 350	μH
Insertion Loss	1-100MHz	-1	dB
Return Loss	1-30MHz	-16	dB
	30-60MHz	-12	dB
	60-100MHz	-10	dB
Differential to Common Mode Rejection Ratio	1-50MHz	-30	dB
	50-150MHz	-20	dB
Crosstalk	30MHz	-35	dB
	60MHz	-30	dB
Isolation	HPOT	1500	Vrms

If these exact requirements cannot be met, the following allowances can be made:

- Turns ratio: 3% is tolerable
- Insertion loss: -1dB or closer to 0dB
- Return loss: Meets or exceeds values in table above

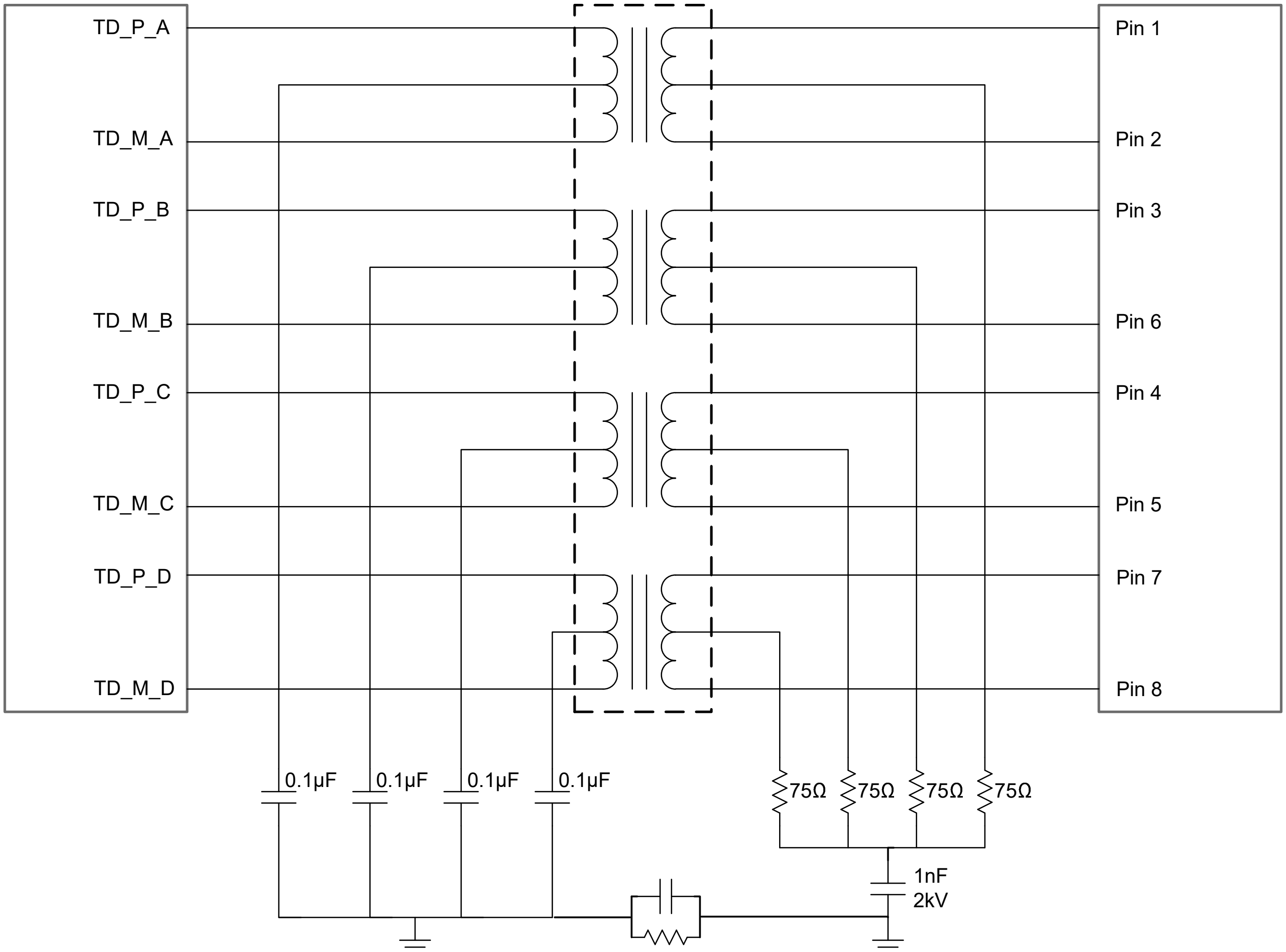

Figure 2-8. PHY to RJ45 and Magnetics

- Each PHY-side center tap must be isolated from one another and connected to ground by a decoupling capacitor.

2.3.2 Probe the MDI Signals

When Auto-negotiation enable, A link pulse should be visible on the channel A transmit and receive differential pairs (TD_P_A and TD_M_A).

A short Ethernet cable with 100 Ohm terminations can be used for measuring the MDI signals. A terminated cable is shown in Figure 2-9. A connection diagram for making measurements with the terminated cable is shown in Figure 2-10.

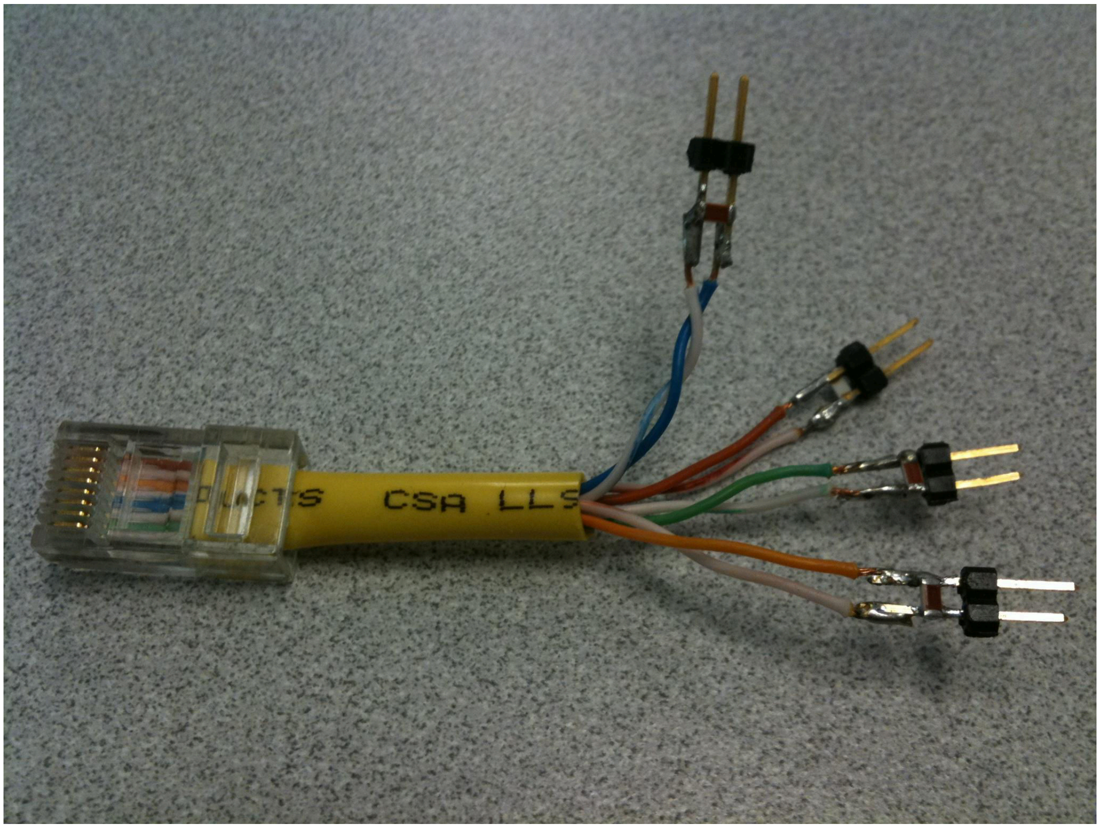

Figure 2-9. 100 Ohm Terminated Cable for MDI Signal Measurement

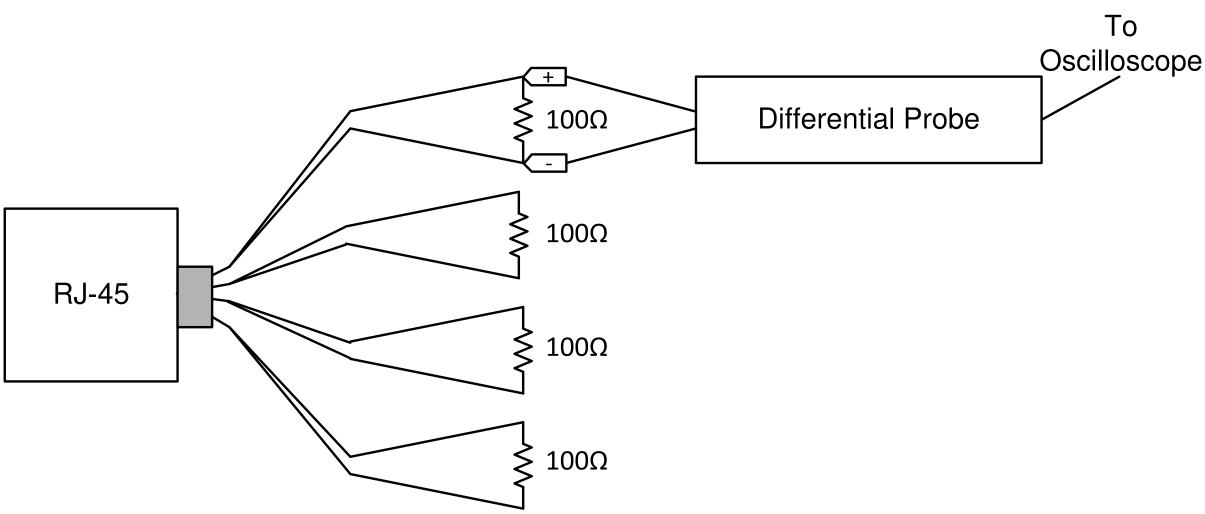

Figure 2-10. Connection Diagram for 100M Terminated Cable

Auto-Negotation link pulses are nominally 100ns wide. Pulses are spaced by 62µs or 125µs and are transmitted in bursts. The bursts are nominally 2ms in duration and occur every 16ms. An example link pulse is shown below in Figure 2-11.

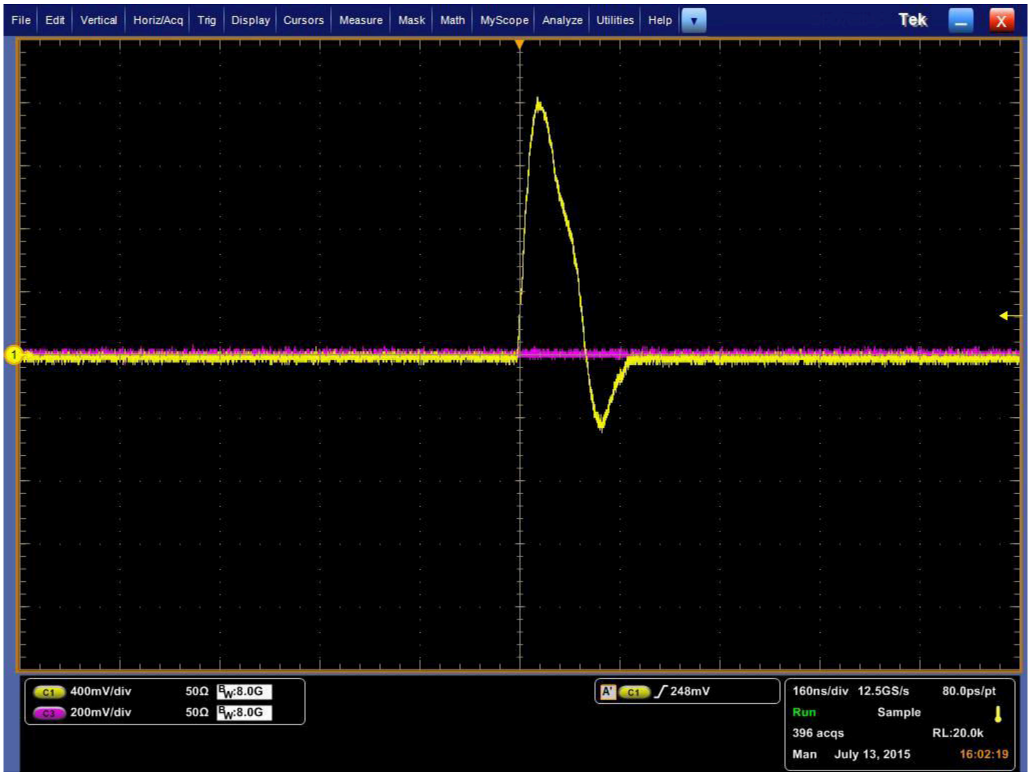

Figure 2-11. DP83867 Link Pulse

Observing this pulse confirms the PHY is on and attempting to link.

2.3.3 Check the Link Quality

After establishing a valid link, confirming the key status register values and visually verifying that the link LED is lit, the next data transfer debug step is to check the MDI Interface. There are several possible sources of link problems:

1. Link partner transmit problem
2. Cable length and quality
3. 25MHz reference clock quality
4. MDI signal quality

With the PHY powered and connected to a link partner, the following registers can be used to determine the Mean Square Error (MSE). For 100Mbps communication please refer to channel A only. The MSE registers are not valid for 10Mbps communication. With the MSE value, use Table 2-7 to determine the link quality.

Table 2-6. Link Quality MSE Registers for 1000Mbps

Channel	Register Address
A	0x225
B	0x265
C	0x2A5
D	0x2E5

For a given channel, read the register value to determine the MSE (Mean Square Error), convert to decimal, and refer to the following table to determine link quality:

Table 2-7. MSE Link Quality Conversion

Link Quality	MSE Range
Excellent	0x020A > MSE
Good	0x33B > MSE > 0x020A
Poor	MSE > 0x33B

2.3.3.1 Improving Short Cable Link Margin

If DP83867 encounters link quality issues with short cables 1m or less in length, consider the section below.

The PHY's digital signal processing (DSP) block may converge to suboptimal filter values at shorter cable lengths which can result in poor Signal to Noise Ratio (SNR). The register configuration below can improve the SNR by adjusting timing bandwidths to help the DSP converge correctly:

```
begin
// Hard Reset
001F 8000
// Threshold for consecutive amount of Idle symbols for Viterbi Idle detector to assert Idle Mode
set to 5
0053 2054
// CAGC DC Compensation Disable
00EF 3840
// Master Training Timers - increasing time in different training states
0102 7477
// Master Training Timers - increasing time in different training states
0103 7777
// Master Training Timers - increasing time in different training states
0104 4577
// Timing Loop Bandwidth
010C 7777
// Timing Loop Bandwidth
01C2 7FDE
// Slave Timers - increasing time in different training states
0115 5555
// Slave Timers - increasing time in different training states
0118 0771
// Timing Loop Bandwidth
011D 6DB2
// Timing Loop Bandwidth
011E 3FFB
// Timing Loop Bandwidth
01C3 FFC6
// Timing Loop Bandwidth
01C4 0FC2
// Timing Loop Bandwidth
01C5 0FF0
// FFE Fix
012C 0E81
// Soft Reset
001F 4000
end
```

2.3.3.2 Improving Inter-channel Link Margin

The DP83867 uses an AGC gain convergence circuit (automatic gain control of MDI receiver) to provide faster linkup. There is a tradeoff between the linkup time and gain mismatch between pairs. In applications where packet errors are observed, gain matching can be improved by increasing the gain convergence time with the following register writes:

```
begin
// Hard reset
001F 8000
// Increase time for AGC
0102 7477
// No AGC Re-train
00E4 0080
// Soft reset
001F 4000
end
```

2.3.4 PMA Compliance

IEEE PMA compliance measurements can be made to verify the signaling characteristics. For details on these measurements and how to properly configure the PHY, please refer to the How to Configure DP8386x for Ethernet Compliance Testing, application note.

If compliance testing fails after following the above application note, check the following:

- Remove ESD diodes on MDI lines for compliance tests
- Ensure the RBIAS value falls within the 1% range
- Ensure the magnetics follow data sheet specifications.
- Do not short center taps on the magnetics, check capacitors on the center taps
- Make sure there are no clock or data signals routed near the MDI lines
- Check length matching and impedance matching for MDI lines

If these checks do not help, adjusting registers 0x00A0, 0x00A1, 0x00A2, and 0x00A3 can help with compliance testing.

2.4 MII Health Checks

This section dives into device health checks which makes sure the MAC interface is operating properly.

2.4.1 MII Check

The Media Independent Interface (MII) is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC. MII operation is available on PAP variants of DP83867 only.

The MII signals are summarized below:

Table 2-8. MII Signals

Function	Pins
Data Signals	TX_D[3:0]
	RX_D[3:0]
Transmit and Receive Signals	TX_EN
	RX_DV
Error Signal	RX_ER

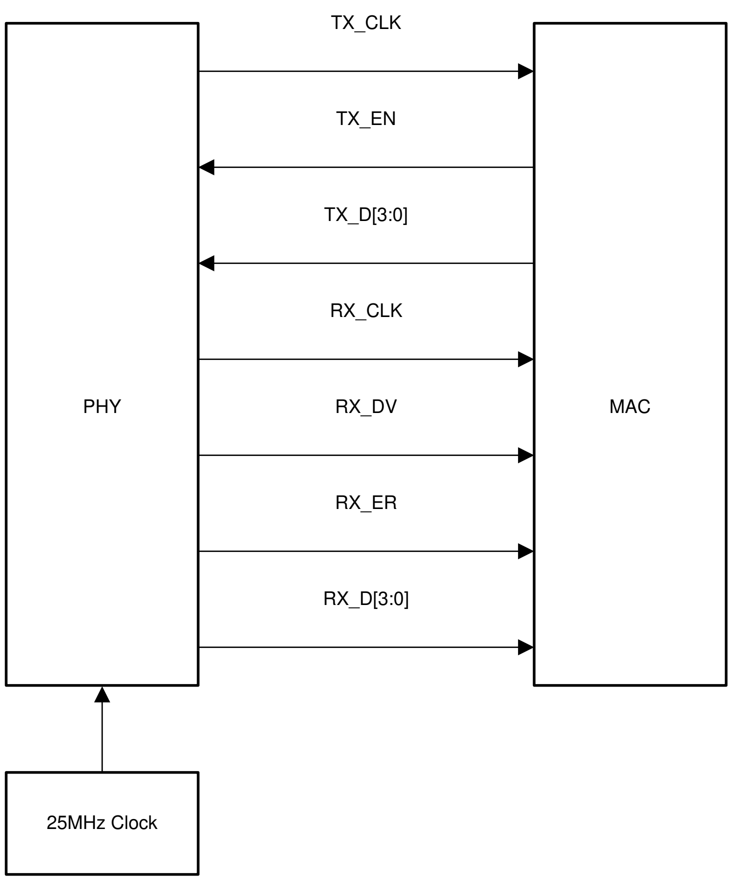

Figure 2-12. MII Signaling

Data on TX_D[3:0] is latched at the PHY with reference to TX_CLK. Data on RX_D[3:0] is provided with reference to RX_CLK. If a MAC TX or RX bus is suspected to be problematic, probe the lines at the receiver side of the trace to make sure that the receiver's setup and hold times are met.

Table 2-9. 100M MII Timings

Spec	Min	Typ	Max	Units
TX_CLK High/Low Time	16	20	24	ns
TX_D[3:0], TX_EN Setup to TX_CLK	10			ns
TX_D[3:0], TX_EN Hold from TX_CLK	0			ns
RX_CLK High/Low time	16	20	24	ns
RX_D[3:0], RX_ER, RX_DV delay from RX_CLK rising	10		30	ns

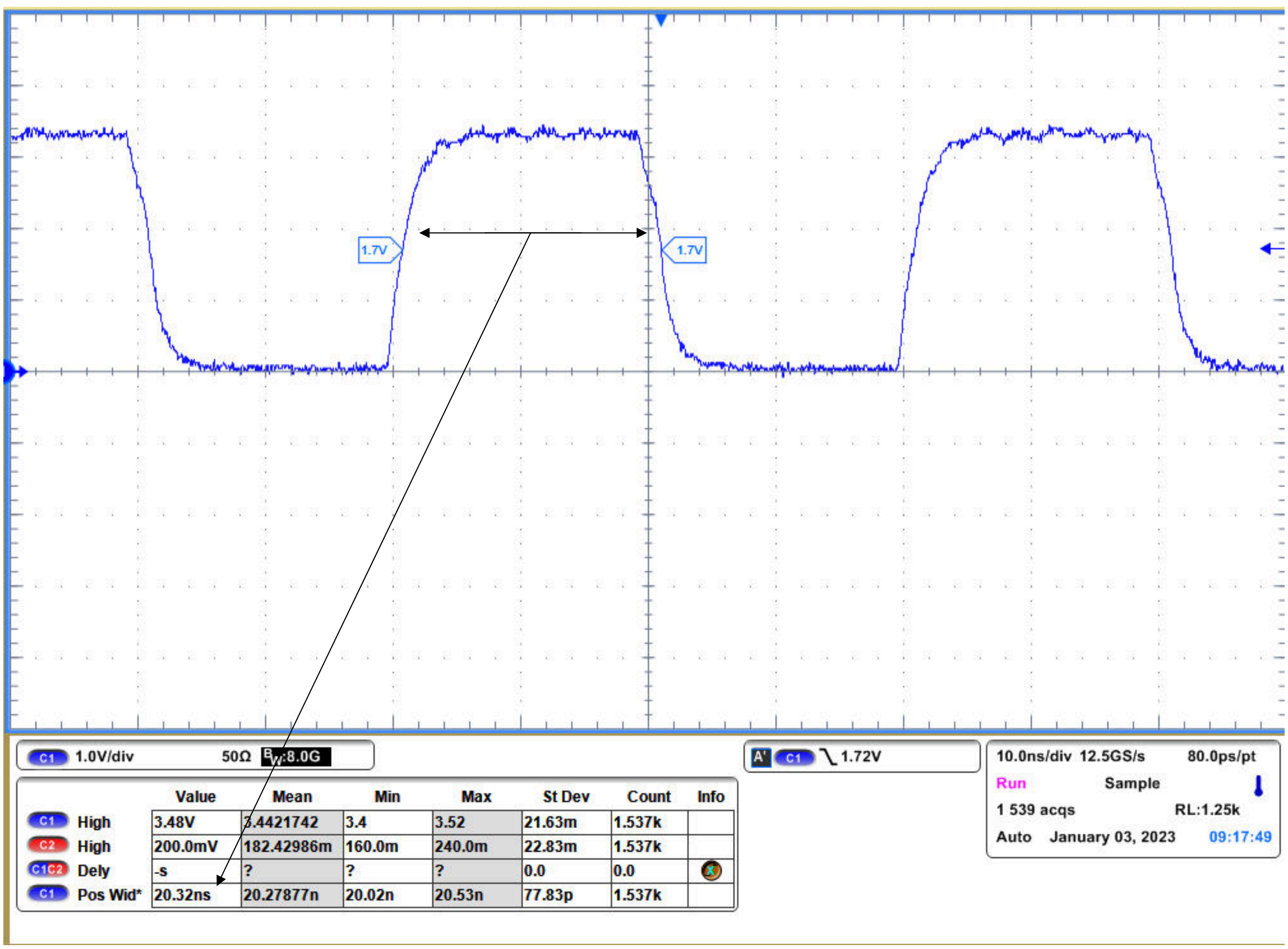

Figure 2-13. 100M RX_CLK High Time

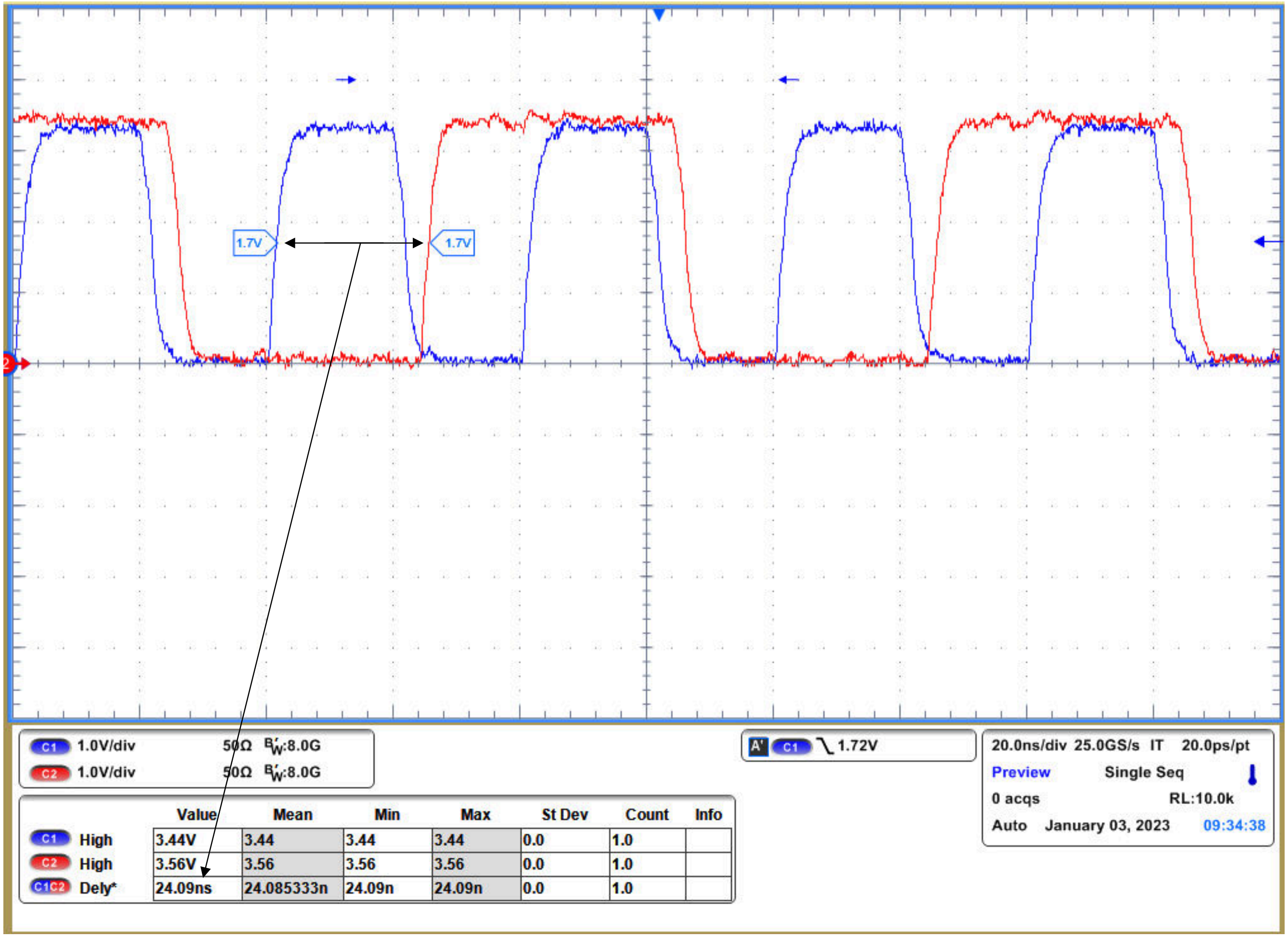

Figure 2-14. 100M RX_D1 Delay From RX_CLK

2.4.2 GMII Check

The Gigabit Media Independent Interface (GMII) is a synchronous 8-bit wide data interface that connects the PHY to the MAC. GMII operation is available on PAP variants of DP83867 only.

The GMII signals are summarized below:

Table 2-10. GMII Signals

Function	Pins
Data Signals	TX_D[7:0]
	RX_D[7:0]
Transmit and Receive Signals	TX_EN
	RX_DV
Error Signals	TX_ER
	RX_ER
Carrier and Collision	CRS
	COL

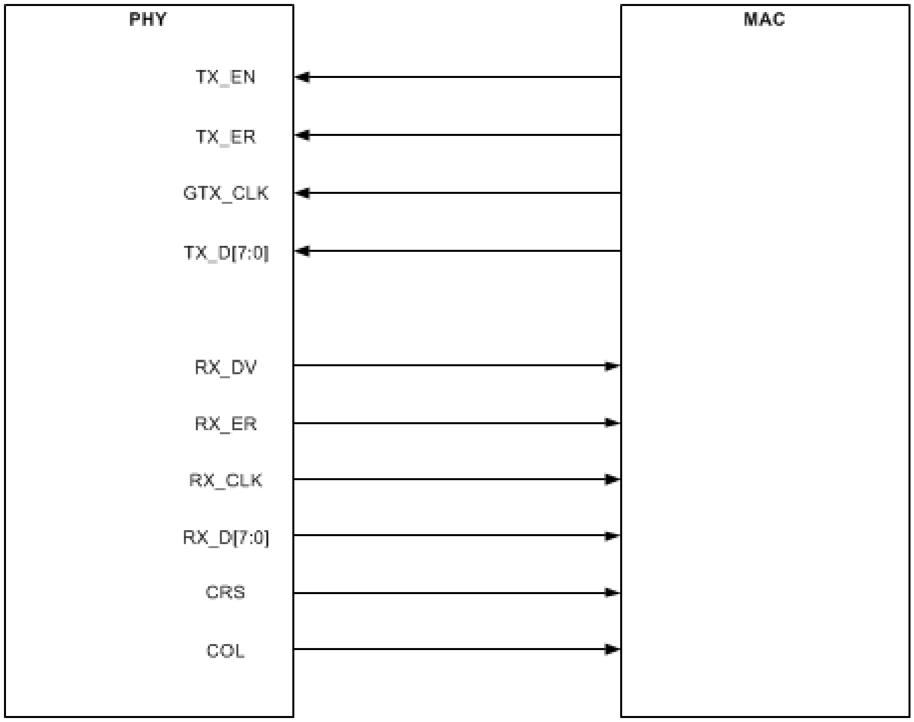

Figure 2-15. GMII Signaling

Data on TX_D[7:0] is latched at the PHY with reference to GTX_CLK. Data on RX_D[7:0] is provided with reference to RX_CLK. If a MAC TX or RX bus is suspected to be problematic, probe the lines at the receiver side of the trace to make sure that the receiver's setup and hold times are met.

Table 2-11. GMII Timings

Spec	Min	Max	Unit
GTX_CLK Rise/Fall Time		1	ns
TX_D, TX_EN, TX_ER Setup to GTX_CLK	2		ns
TX_D, TX_EN, TX_ER Hold from GTX_CLK	0.5		ns
RX_CLK Rise/Fall Time		1	ns
RX_D, RX_DV, RX_ER delay from RX_CLK rising	0.5	5.5	ns

2.4.3 RGMII Check

The Reduced Gigabit Media Independent Interface (RGMII) is a 4-bit wide data interface that supports up to 1000Mbps communication between a PHY and MAC.

The RGMII signals are summarized below:

Table 2-12. RGMII Signals

Function	Pins
Data Signals	TX_D[3:0]
	RX_D[3:0]

Table 2-12. RGMII Signals (continued)

Function	Pins
Transmit and Receive Signals	TX_CTRL
	RX_CTRL

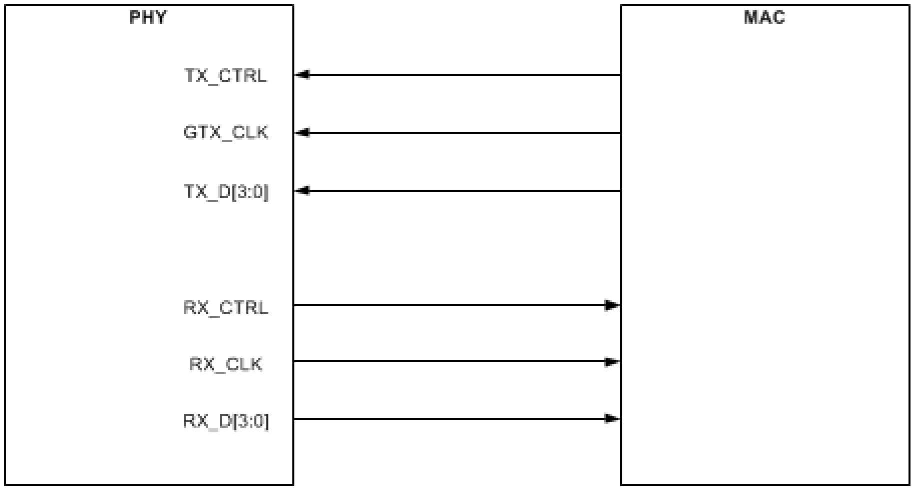

Figure 2-16. RGMII Signaling

Reference the waveforms in this section to verify the expected MAC data and clock signals for RGMII in shift and align modes. To capture data and clock signals, measure close to the receiver end. Note the following requirements for selecting the correct delay mode:

Table 2-13. Selecting the Correct RGMII Delay Mode

If MAC's Configuration is	Required PHY Configuration
RGMII Align Mode on TX side	RGMII Shift Mode on TX side
RGMII Align Mode on RX side	RGMII Shift Mode on RX side
RGMII Shift Mode on TX side	RGMII Align Mode on TX side
RGMII Shift Mode on RX side	RGMII Align Mode on RX side

Note

In Shift mode, the clock skew can be adjusted using the RGMII Delay Control Register (RGMIIDCTL), address 0x0086.

RX_D[3:0] and RX_CLK in Shift and Align Mode

For the PHY set in RX align mode in 10/100Mbps, probe the clock and data signals on the MAC end and compare to the reference waveforms shown below:

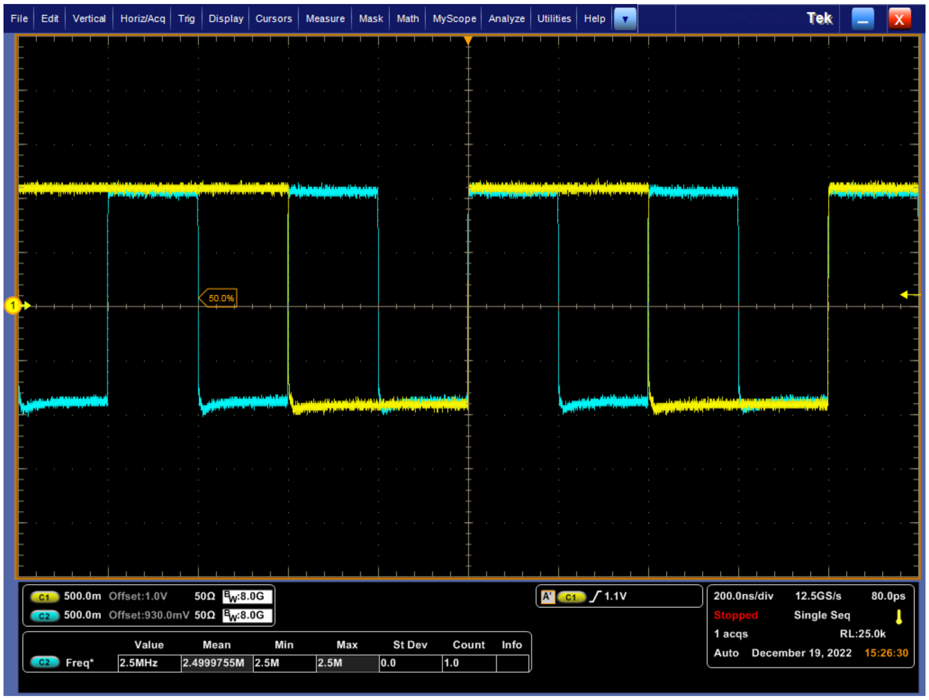

Figure 2-17. 10 Mbps Data Aligned with RX_CLK

Verify the frequency of the clock (C2) as 2.5MHz, and the data (C1) being sampled at the rising edge of the clock.

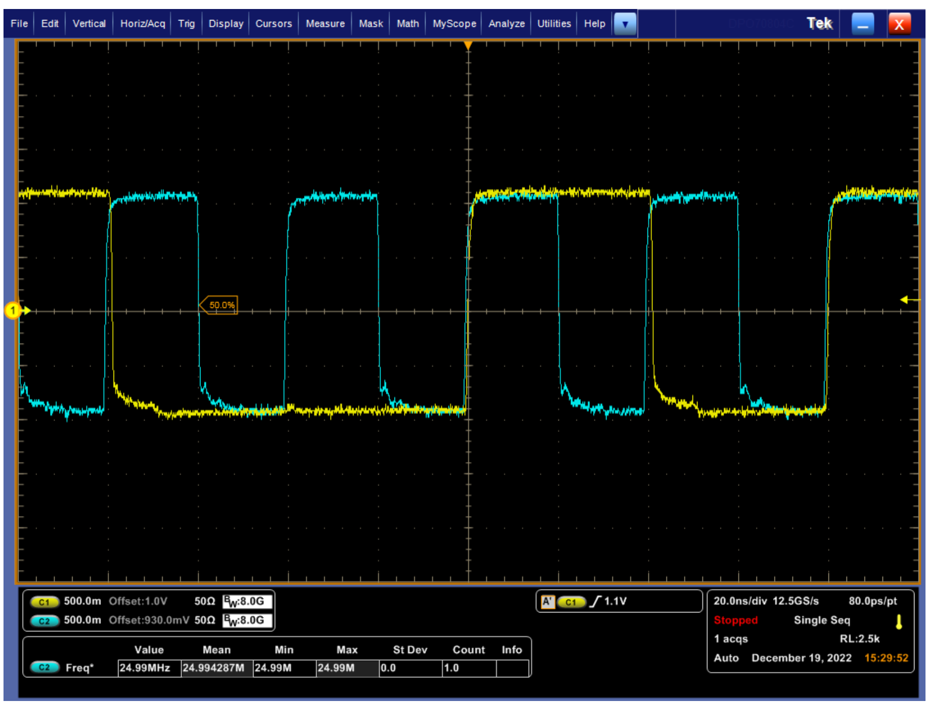

Figure 2-18. 100 Mbps Data Aligned with RX_CLK

Verify the frequency of the clock (C2) as 25MHz, and the data (C1) being sampled at the rising edge of the clock.

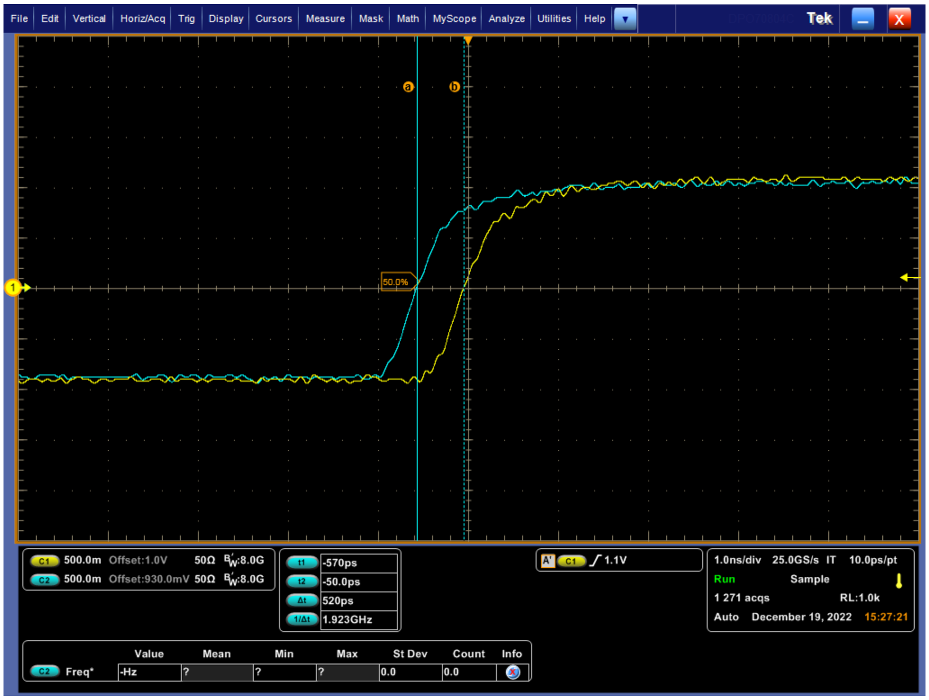

Figure 2-19. 10Mbps Data and Clock Delay in Align Mode

Verify the delay between clock and data is <500ps in align mode.

For the PHY set in RX shift mode (0x32) in 10/100Mbps, probe the clock and data signals on the MAC end and compare to the following reference waveforms.

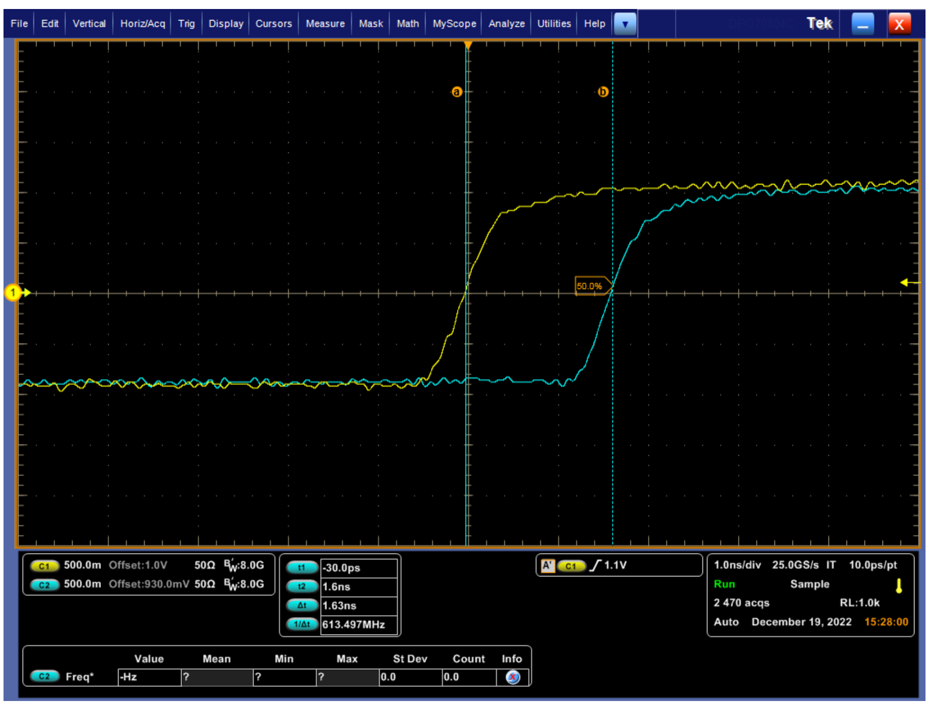

Figure 2-20. 10 Mbps Data and RX_CLK in Shift Mode (4ns Programmed Delay)

Verify the delay between clock and data is >1ns in shift mode. The programmed delay is relative to the clock's initial position in aligned mode. Measuring the difference in the clock's position before and after setting shift mode yields a value closer to the programmed delay.

TX_D[3:0] and TX_CLK in Shift and Align Mode

For the PHY set in TX shift or align mode, probe the data and clock signals on the PHY end and verify the timing requirements below are met:

Table 2-14. RGMII Timings

PARAMETER		MIN	NOM	MAX	UNIT
T_{skewT}	Data to Clock output Skew (at Transmitter)	–500	0	500	ps
T_{skewR}	Data to Clock input Skew (at Receiver)	1	1.8	2.6	ns
T_{setupT}	Data to Clock output Setup (at Transmitter – internal delay)	1.2	2		ns
T_{holdT}	Clock to Data output Hold (at Transmitter – internal delay)	1.2	2		ns
T_{setupR}	Data to Clock input Setup (at Receiver – internal delay)	1	2		ns
T_{holdR}	Clock to Data input Hold (at Receiver – internal delay)	1	2		ns
T_{cyc}	Clock Cycle Duration	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit	45	50	55%	
Duty_T	Duty Cycle for 10/100T	40	50	60%	
T_R	Rise Time (20% to 80%)			0.75	ns
T_F	Fall Time (20% to 80%)			0.75	ns

2.4.4 SGMII Check

The Serial Gigabit Media Independent Interface (SGMII) provides a means of conveying network data and port speed between a 100M/1000M PHY and a MAC with less signal pins than required for GMII or RGMII. The SGMII interface uses 1.25Gbps LVDS differential signaling which has the added benefit of reducing EMI emissions relative to GMII or RGMII. SGMII is available on DP83867E/IS/CS variants only

Table 2-15. SGMII Output Spec

SGMII Output		Min	Max	Unit
Output Differential Voltage	SO_P and SO_N, AC Coupled	0.3	0.8	V Peak diff

All SGMII connections must be AC-coupled through a 0.1uF capacitor

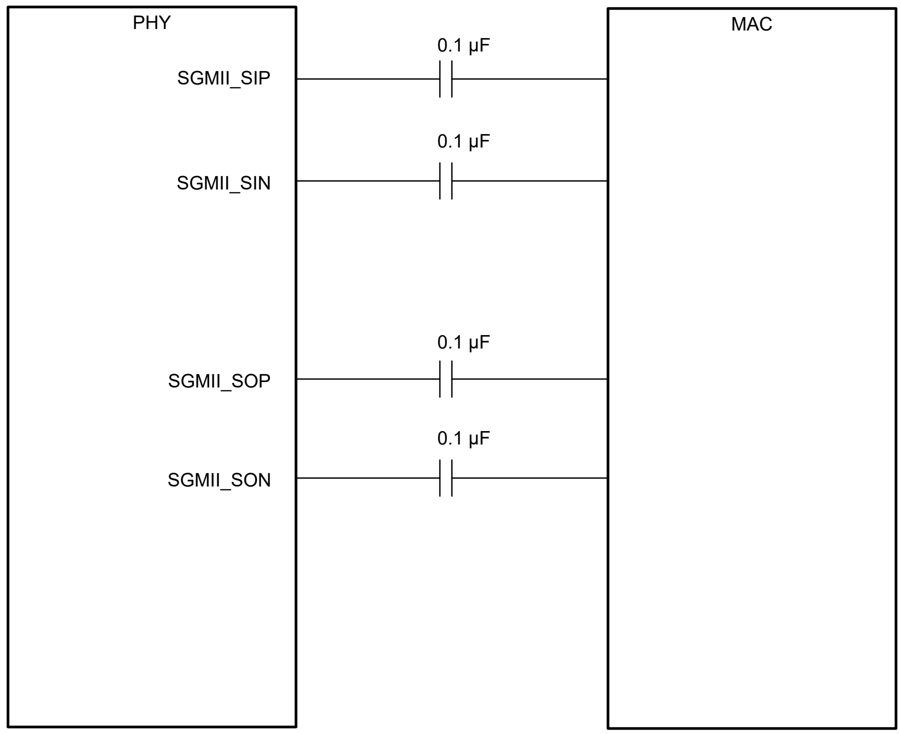

Figure 2-21. SGMII Signaling

If SGMII is not operating properly, consider the following:

1. Check Register 0x0037[0] for the SGMII autonegotiation completion status
2. Check Register 0x0037[1] to see whether an SGMII control page has been received
3. Verify the SGMII signals have the correct peak to peak voltage
4. Reset the SGMII auto-negotiation in register 0x0014[7]

2.5 Loopback and PRBS

2.5.1 Loopback Modes

There are several options for loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the MII and MDI data paths. DP8386 7 can be configured to one of the near-end (MII) loopback modes or to the reverse (MDI) loopback mode.

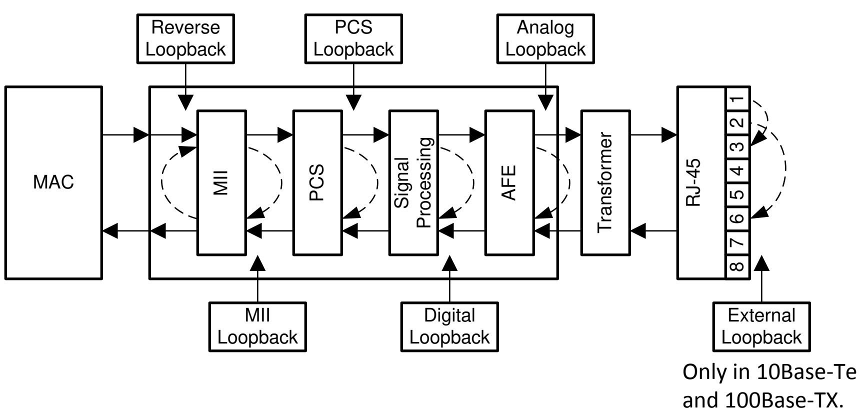

Figure 2-22. Loopbacks

The availability of Loopback depends on the operational mode of the PHY. The Link Status in these loopback modes is also effected by the operational mode. The table below lists out the exceptions where loopbacks are not available.

Table 2-16. Loopback Availability Exception

OP MODE	LOOPBACK	EXCEPTION
RGMII/GMII (PAP)	PCS	10M
	External	1000M
SGMII (E/IS/CS)	MII	10M
	Digital	10M
	Analog	10M

MII loopback can be used to verify the MAC interface, while reverse loopback is used with a link partner to verify the data path along the MDI.

- MII loopback is enabled by setting register 0x0000[14]
- Reverse loopback is enabled by setting register 0x0016[5]

2.5.2 Transmitting and Receiving Packets with the MAC

If generating and checking packets with the MAC is possible, and the PHY has a working link partner with reverse loopback capability, verify the full data path as follows:

1. Connect the PHY to the MAC and a working link partner.
2. Enable reverse loopback on the link partner.
3. Transmit test packets from the MAC to the PHY.
4. Verify the MAC receives the same test packets.

If the MAC receives the same test packets transmitted without issue, the full data path through MAC → PHY → MDI is valid. If this test does not pass, perform MII loopback to isolate the issue along the data path:

1. Power and connect the PHY to the MAC.
2. Enable MII loopback on the PHY.
3. Transmit test packets from the MAC to the PHY.
4. Verify the MAC receives the same test packets.

If the MAC receives the same test packets, the data path through MAC → PHY is valid, and the issue has been isolated to the MDI data path. If this test does not pass, the issueis likely on the MAC interface. To verify the MAC interface, refer to MII Health Checks. To verify the PHY internal data path, perform the above procedure using analog loopback mode.

2.5.3 Transmitting and Receiving Packets with BIST

DP83867 incorporates an internal PRBS Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. BIST can be performed using various loopback modes to isolate any issues to specific parts of the data path. The BIST generates packetized data with variable content and IPG.

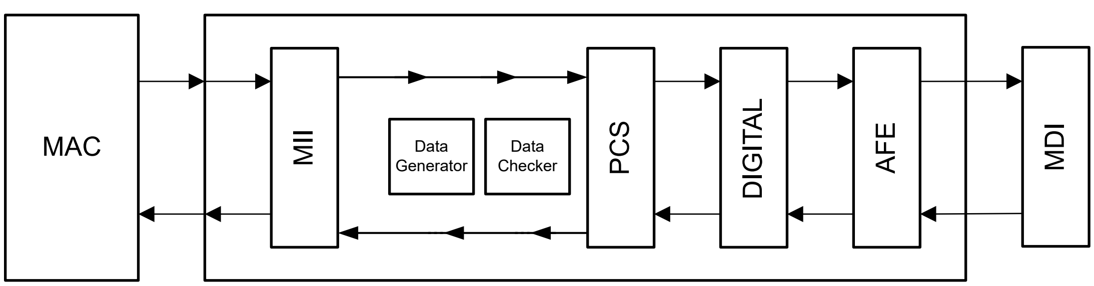

Figure 2-23. BIST Block Diagram

If generating and checking packets with the MAC is not possible, use PRBS packet generation and checking functionalities to verify the data path. Perform reverse loopback with PRBS and a working link partner as follows:

1. Connect the PHY to a link partner.
2. Enable PRBS packet generation on the PHY (write Reg 0x0016 = 0xF000).
3. Enable reverse loopback on the link partner (If link partner is DP83867, write Reg 0x0016 = 0020).
4. Wait at least one second, then check PRBS lock status on the PHY by reading register 0x17[11].

If register 0x17[11] is high, the data path through PHY → MDI is valid. If this test does not pass, the issue could be on the PHY's internal data path or the MDI. To verify the internal data path, perform PRBS with analog loopback using the following script. This script can be modified as needed using notes (1), (2), and (3) to test the appropriate speed and loopback:

```
// This is how you make a comment. All scripts must start with 'begin'
begin
// hard reset
001F 8000
// disable auto-neg, force 10Mbps (1)
0000 0100
// enable analog loopback (2)
0016 0008
// force mdi mode for 10/100 Mbps (not relevant for 1000Mbps)
0010 5008
// loopback configuration register required
00FE E720
// enable packet gen, keep analog loopback (3)
0016 5008

// (1)
// for 100Mbps, write 0000 to 2100
// for 1000Mbps, write 0000 to 0140
// (2)
// for digital loopback, write 0016 to 0004
// for PCS loopback, write 0016 to 0003
// (3)
// for packet generation with digital loopback, write 0016 to 5004
// for packet generation with PCS loopback, write 0016 to 5003
end
```

If the internal data path is valid the issue is isolated to the MDI or the link partner.

3 Application Specific Debugs

3.1 Link up in 100Mbps Full Duplex Force Mode

If DP83867 is configure in force 100Mbps full duplex force mode through register 0x0000 bit[12] and bit[6,13] and wasn't able to link up, please check the following process:

- Check the link partner PHY and see if auto-negotiation is enable on the link partner PHY.
- If the link partner PHY's auto-negotiation is on and able to advertise 100Mbps full duplex and half duplex, enable register 0x001E[11] for the link up
- If the link partner PHY's auto-negotiation is disable, make sure the link partner PHY is also program in force 100Mbps full duplex mode in register 0x0000.

3.2 Unstable Link Up Debug in 1Gbps communication

If repeating link up and link down occurs between DP83867 and another Link Partner, follow this section for debug:

1. Write register 0x001F to 4000 (software reset) and see if you are able to link up.
2. Check if DP83867 is able to link up with another TI gigabit PHY.
3. Check the Schematic and Layout Checklist section to make sure the board design follows the recommendations.
4. Read register 0x0013 bit[12] and register 0x0011 bit[12]. If both registers indicate page received in 1Gbps communication. Write register 0x01D5 = F508 to change DP83867PHY from low power mode to normal operational mode.

```
begin
// Check page recieved in 1Gbps communication
0012
0013
// changing from lower power mode to normal operational mode
01D5 F508
end
```

3.3 DP83867PHY and DP83867PHY Cannot Link Up in 1Gbps

If two DP83867PHYs are able to link up at 10Mbps and 100Mbps but not able to link up at 1Gbps, please refer to the following debug process:

Note

This errata only occur in old revision of the DP83867PHY (Register 0x0003 = A0F1)

- Try software reset by writing register 0x001F = 4000 on one of the DP83867PHY and see if that resolve the issue.
- Read register 0x0005[15] and If 0x0005 bit[15] = 0,
  - Auto-MDIX is most likely not complete. Both of the PHY is sending Auto-MDIX FLP_Brust in the same channel at the same time and result in deadlock situation.

  Solution:

  - Change Auto MDIX timer on one of the PHY can prevent the deadlock situation.
  - Change register 0x002C bit[32] = 0 on one of the DP83867PHY

  Auto MDIX Timer Configuration Register (AMDIX_TMR_CFG), Address 0x002C

BIT	NAME	TYPE	DEFAULT	DESCRIPTION
15:4	RESERVED	RW	0x141	RESERVED
3:0	RAMDIX_TMR	RW	0xF	Robust Auto MDIX Timer 0000: 32ms 0001: 64ms 0010: 96ms . . 1111: 480ms

  - write 0x001F to 4000 to software reset the PHY
- Read register 0x0005[15] and If 0x0005 bit[15] = 1
  - Auto-MDIX is complete and Auto-negotiation pseudo random number (PRN) is most likely be the issue. Pseudo random number (PRN) sending *random number* to determine which PHY is Master PHY (clocked from a local source) and which one is the slave PHY (clocked from the recovered clock on the received data stream) when both PHY are communicate in 1000Base-T. This can be check through register 0x000A bit[14].
  - However, the PRN is not exactly random and if both DP83867 start auto-negotiation at the same time, there is a possibility both DP83867 send out the exact same random seed (PRN) and result in dead lock.

  Solution:

  - Write 0x0009 bit[12:11] to 11 on one of the DP83867PHY and write 0x0009 bit[12 :11] to 10 on another DP83867PHY. This register can force one of the PHY to always be MASTER in 1000Base-T communication to prevent the Pseudo random number (PRN) process.
  - Write 0x001F to 4000 to software reset the PHY or write 0x0000[9] =1 to restart the auto-negotiation

3.4 EMC Debug

The following section mainly go over the general guideline on how to debug EMC issue on DP83867PHY.

- Check the test setup:

  EMC test:

  – No loop cable

  – Place the cable away from the emission source or Antenna (mainly on RE test)
  – Shielded cable is preferred
  – Make sure the test board and test equipment match (mainly on CE test)
    - Cable type needs to match the CDN test equipment
  – Turn off CLK_OUT when it is open or not used
  – EMI test:
    - Check the ground path of both test board and test equipment
    - Shielded cable is preferred
    - Make sure the cable type match with test equipment (mainly on CI test)
      – Cable type needs to match the CDN test equipment
- Check the schematic
  – Make sure there is a ground isolation

    Make sure there is a ground isolation path (R//C) between connector ground and earth ground

    Make sure the Transformer follow data sheet specification

    No shorted center taps on transformer

    Double check on the capacitors on the center taps of transformer

    Remove ESD diodes on MDI lines for compliance test

    Check Rbias value and make sure the value falls in the 1% range

    Follow the schematic check list recommendation in Section 2.1
- Check the layout
  – Make sure no clock signal and data signal near the MDI lines
  – Check length matching and impedance matching for MDI lines
  – No vias around the MDI lines
  – Follow the layout checklist in Section 2.1
- If customer is struggling on conducted immunity IEC61000 4-6 on DP83867 PHY, please program the following script:
  –

```
begin
008A 010F
00C0 0000
00B3 000C
0100 1027
001F 4000
end
```

These registers tune the filter inside the PHY to further optimize and filter out high frequency noise and improve the Signal to Noise ratio.

3.5 Packet Errors in Links with Low IPG

If packet errors are observed in ethernet links with inter-packet gaps (IPG) equal to or less than 12 idle symbols, it may be necessary to tune the Viterbi threshold within DP83867. This threshold can be tuned in the VTM_IDLE_CHECK_CNT_THR register (0x0053[3:0]) where the default value of 0x5 is intended for IPGs greater than or equal to 12 symbols.

If the application expects an IPG less than 12 symbols, the Viterbi threshold can be tuned lower to 0x4 or 0x3. If errors are observed with an IPG of exactly 12 symbols, this threshold can be tuned lower as a debug step to ensure the errors are not a result of IPG.

3.6 10Base-Te TP_IDL Failure

If DP83867 is failing 10Base-Te TP_IDL tests, check that the board layout follows the recommendations in the Schematic and Layout Checklist section of this application note. If the layout is determined to not be at fault or if the layout cannot be changed, consider tuning the TP_IDL swing on DP83867.

Register 0x0023[15:12] controls the swing of the DP83867 output signal used by 10Base-Te TP_IDL tests. Read the default register value and increase or decrease as needed.

3.7 Slow RGMII Rise/Fall Times

If DP83867 exhibits slow RGMII rise/fall times on the RGMII transmitters (RX_CLK, RX_D0, ...) please double check the following:

- Keep RGMII traces as short as possible. Long traces can increase trace capacitance and slow rise/fall times.
- Check the connected MAC input capacitance. If the MAC is loading the RGMII lines with high capacitance, it will slow rise/fall times.
- Check the probe capacitance. A low capacitance probe should be used for RGMII measurements

If these considerations are taken and RGMII rise/fall times are still slow, adjust the IO_IMPEDANCE_CTRL register located at address 0x0170. In general, a lower impedance value is expected to produce faster RGMII rise/fall times. One method to adjust this register is described below:

1. Read the IO_IMPEDANCE_CTRL register
2. Based on the read value, write the corresponding new value as shown in the table below:

Read Value (0x170[4:0])	New Value (0x170[4:0])
0x00, 0x01	0x08
0x02, 0x03	0x0A
0x04, 0x05, 0x06, 0x07	0x0C
0x08, 0x09	0x0E
0x0A, 0x0B	0x10
0x0C, 0x0D, 0x0E, 0x0F	0x12
0x10, 0x11, 0x12, 0x13	0x14
0x14, 0x15	0x16
0x16, 0x17, 0x18, 0x19	0x18
0x1A, 0x1B	0x1A
0x1C, 0x1D, 0x1E, 0x1F	0x1C

4 Tools and References

The following section contains additional tools and references relevant for debugs.

4.1 Extended Register Access

To read and write registers in extended register space, refer to the following procedure:

Write procedure for MMD "1F" registers:

write reg<000D> = 0x001F

write reg<000E> = <address>

write reg<000D> = 0x401F

write reg<000E> = <value>

Read procedure for MMD "1F" registers:

write reg<000D> = 0x001F

write reg<000E> = <address>

write reg<000D> = 0x401F

read reg<000E>

Note

- To read or write MMD "1" registers, replace 1F with 01.
- Above write and read procedure is normally used for registers with address greater than 0x001F. But the procedure can also be used for any address in general.

5 Conclusion

This application note provides a suggested flow for evaluating a new application and confirming the expected functionality. The step-by-step recommendations will help ease board bring up and initial evaluation of DP83867 designs.

6 References

1. Texas Instruments, *How to Pass IEEE Ethernet Compliance Tests*, application note.
2. Texas Instruments, *How to Configure DP838xx for Ethernet Compliance Testing*, application note.

7 Revision History

Changes from Revision B (December 2022) to Revision C (April 2024)	Page

Changes from Revision A (April 2016) to Revision B (December 2022)	Page

Changes from Revision * (October 2015) to Revision A (April 2016)	Page