

# DS92LV16

*Easy-to-Use LVDS Serdes for the Serdes Neophyte*



Literature Number: SNLA182

# Technology Edge

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## **Easy-to-Use LVDS Serdes for the Serdes Neophyte** BY: Dave Lewis, Analog Marketing Signal Manager

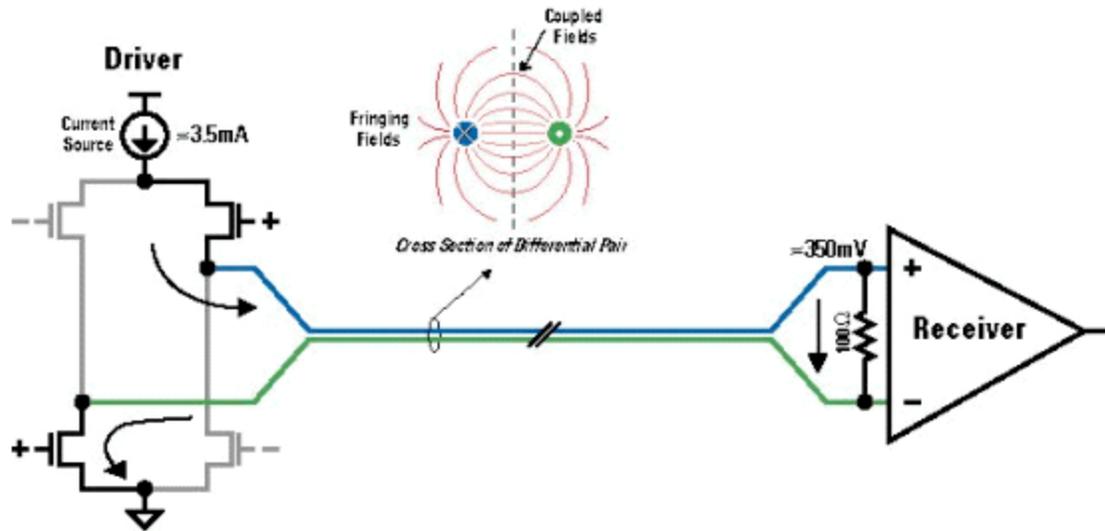
The world has come to expect information as graphics - no longer is simple text acceptable - and this has driven interconnect speeds ever higher. This trend has been biggest in telecom and datacom equipment, but now many other applications including industrial, medical, and consumer equipment must revolutionize their interconnect speeds from mere kilobits per second to megabits or gigabits per second. Whether this interconnect is cable or backplane, traditional parallel buses break down at those speeds due to signal integrity, EMI, and power consumption issues, and serialization becomes the only choice. For many designers, however, serializers have been a bit of a black art. National Semiconductor has introduced the DS92LV16 16:1/1:16 serializer/deserializer to meet the needs of both new and experienced serdes users.

To be easy-to-use, a serializer/deserializer (serdes), must have the following:

- Robust signalling
- Wide frequency range
- Allow local clock generation using inexpensive crystals
- Accept any input data: coded or uncoded
- Provide live insertion capability

### **Signalling**

Electrical signalling at gigabit speeds requires differential signalling. There are many differential signalling standards such as ECL/PECL, LVDS, CML, and others. ECL and PECL are difficult to implement in CMOS process technology and CML exists as many flavours. Low Voltage Differential Signaling (LVDS), on the other hand, is a widely recognized standard (TIA/EIA-644) and is available on most ASICs and FPGAs as well as on 100s of standard chips. LVDS also has the advantage of being a current loop technology, resulting in the tendency for radiated electric fields to cancel, reducing EMI. National's DS92LV16 uses the LVDS industry-proven technology for the serial link.



### Clocking

A serdes should operate over a wide clock range to satisfy the needs of a wide variety of applications. Once a design is completed with the serdes, the design can be reused, saving time and inventory costs. When talking of clocks, there are two to consider: transmit clock and receiver reference clock. The transmit clock is latches the data into the serializer and it is this clock which is embedded in into the serial stream. At the other end, the receiver recovers this embedded clock with the help of a local clock reference called REFCLK. Serdes devices specify the maximum allowable difference between the transmit clock and REFCLK frequencies. A typical value is +/-100 PPM which means that the two clocks' frequencies must be within 100 parts per million of each other. Many designs will generate the two clocks locally (one on each board), meaning that the two clock generators must be within this +/-100 PPM tolerance. A serdes with a wider permissible frequency disparity relaxes the requirements on the selection of clock sources, allowing less accurate and therefore less expensive clock generators to be used. The DS92LV16 serializes a 16-bit bus over a wide frequency range from 35-80 Mhz and has a clock frequency disparity specification of +/-5% or +/- 50,000 PPM.

### Data Coding

An easy-to-use serdes should be able to serialize any form of data. It should not require pre-coding of data. Most newer serdes devices accept any data, doing the coding internally, but some older parts require input data to be pre-coded using 8b/10b coding. The 8b/10b coding scheme is based on representing each byte (8 bits) as a 10-bit code. A look-up table determines which 10-bit code corresponds to each byte. Since there are four times more 10-bit codes than 8-bit codes, the codes can be assigned so that the number of ones and zeros in the serial stream is roughly balanced. This "DC balance" is an advantage when sending data across long cables or across fiber. The DS92LV16 does not use 8b/10b coding, but opts for a different scheme requiring less overhead and providing true hot plug capability. The DS92LV16 coding scheme, proven on a range of 10-bit serdes, sends the 16-bit word along with a start and stop bit for a total of 18 bits for every 16-bit word (compared to 20 bits for 8b/10b). Although not DC balanced, this scheme not only uses less overhead, but provides true live insertion capability.

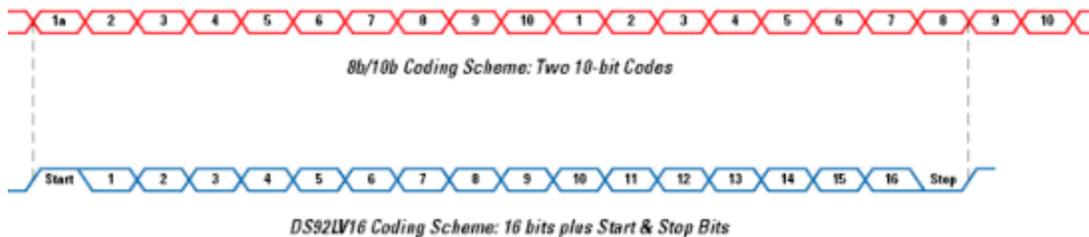
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### Live Insertion

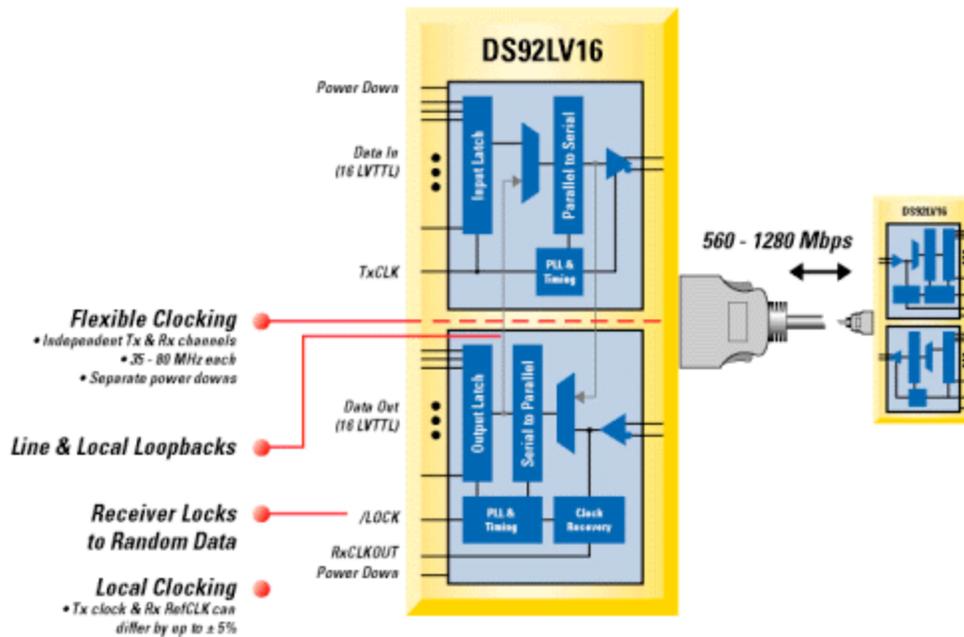
Live insertion (also called hot plug or hot insertion) means the device does not disrupt data on the active data lines during insertion. For differential technologies like LVDS, any device with power up high impedance (i.e. the device's outputs are held in the high impedance state until the device is powered up) will minimize the disturbance of data during live insertion, because the coupled noise is mostly common mode which is rejected by the receiver. (Differential signalling means two wires are used to convey information and the differential receivers look at the difference in the voltages of the two wires to determine logic high and logic low. A differential device being plugged into these two wires will tend to disturb both lines equally. This "common mode noise" is then rejected by the differential receiver.) National Semiconductor has conducted several live insertion backplane experiments which show that LVDS-equipped cards can be inserted into an active backplane without bit errors. Traditionally, live insertion was defined this way, but is that the whole story?

After a successful live insertion event, the serdes deserializer logic must then lock to the active data stream before it can present valid data at its outputs. 8b/10b coded devices generally must receive special 10-bit words called comma characters to train the deserializer where the byte or word boundaries in the serial stream are. Many datacom systems and some telecom systems send a lot of these characters during normal data transmission anyway, so the 8b/10b serdes needs only to wait until a string of these characters is sent. Non-datacom systems, however, must interrupt normal data flow to send these training characters after live insertion. If live insertion is defined as no interruption of data during a live insertion event, interruption of data flow by the system to send training signals directly after live insertion is equally bad.

The DS92LV16 has power up high impedance to avoid data corruption during live insertion, plus its coding scheme allows the chip's deserializer to then lock onto the random data stream automatically. The DS92LV16 accomplishes lock to random data by storing a useful length of the serial stream and looking for consistent start and stop bits. If consistency is not found, it will look at the next length of serial data until lock is achieved--

automatically and without system intervention. This feature allows hot plugging of cards without special higher level system control.

### Conclusion



National Semiconductor's DS92LV16 can be easily designed into a variety of applications from communications equipment, the traditional home of serdes devices, to new industrial, medical, and professional consumer equipment now needing high speed interconnect. The 35-80 MHz 16-bit serializer/deserializer delivers 560 Mbps to 1.28 Gbps at low noise, low power, and low cost.

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