AN-1320 Enhancing LMH0031 Jitter Performance With Easy-To-Use VCXOs

ABSTRACT

This application report discusses how to improve and enhance LMH0031 Jitter performance with VCXOs.

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1 Introduction

The LMH0031 SMPTE 292M / 259M Digital Video Deserializer is a monolithic integrated circuit that deserializes and decodes SMPTE 292M, 1.485 Gbps (or 1.4835 Gbps) serial component video data, to 20-bit parallel data with a synchronized parallel word-rate clock. It also deserializes and decodes SMPTE 259M, 270 Mbps, 360 Mbps and SMPTE 344M, 540 Mbps serial component video data, to 10-bit parallel data. Functions performed by the LMH0031 include: clock/data recovery from the serial data, serial-to-parallel data conversion, SMPTE standard data decoding, NRZI-to-NRZ conversion, parallel data clock generation, and automatic video format determination.

The LMH0031 has excellent immunity to input jitter on the SDI inputs, but the parallel data output clock (V_{CLK}) has jitter characteristics which make it unsuitable for a direct connection to a PLL-based serializer such as the LMH0030. The LMH0031 output clock is intended to be used as a parallel video data clock for logic blocks rather than as a reference clock. One way to reduce this jitter is to use a Voltage Controlled Crystal Oscillator (VCXO) with the LMH0031 and use the recovered, jittery clock to phase and frequency lock the VCXO generated clock to the recovered data. Facility for this has been included in the LMH0031.

In normal operation for the LMH0031, the recovered clock is brought out through the V_{CLK} output pin. The LMH0031's R_{BB} pin provides a current, controlled by R_{REF}, which can be used to bias the SDI input pins. In VCXO operation, the direction of the V_{CLK} pin is changed from output to input and it is supplied with the clock from a VCXO. This VCXO clock is then phase locked to the internal V_{CLK} via a phase-frequency detector on board the LMH0031. The R_{BB} function is changed from the bias supply output to the control voltage output of the phase-frequency detector. An external loop filter and a voltage amplifier are required to interface the control voltage output to the VCXO frequency control input. Table 1 shows the LMH0031 pin functionality differences between normal mode and VCXO mode.

VCXO operation is enabled by setting the EXTERNAL V_{CLK} bit of the LMH0031's VIDEO CONTROL 0 register (address 55h). Figure 1 shows an example using dual VCXOs for V_{CLK} to handle both standard and high definition video.

Table 1. LMH0031 Pin Functions for Normal Mode and VCXO Mode

Pin Name	Normal Function	VCXO Function
V_{CLK}	Output recovered clock	Input VCXO clock (for phase locking)
R_{BB}	Bias for SDI input pins	Control voltage for VCXO

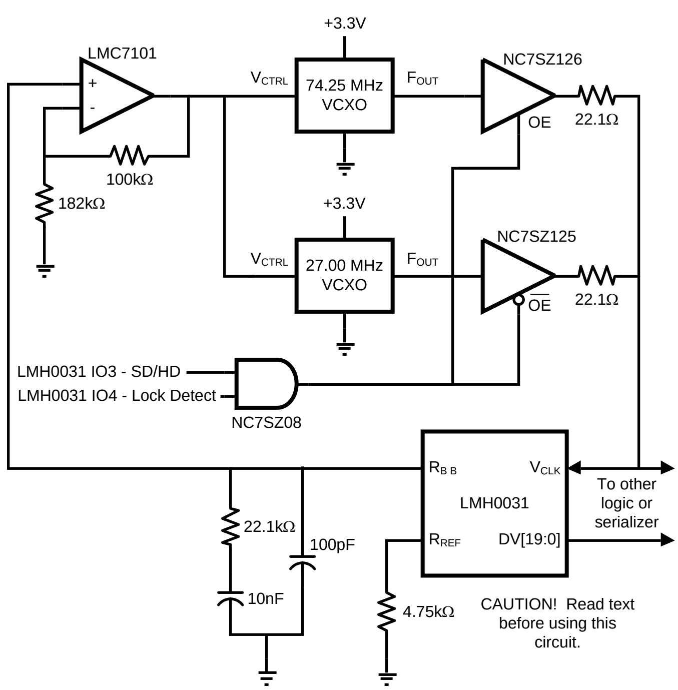

Figure 1. Using Dual VCXOs for V_{CLK}

In this example, the control voltage output from R_{BB} is externally filtered by the loop filter consisting of a 22.1kΩ resistor in series with a 10nF capacitor, combined in parallel with a 100pF capacitor. This gives a loop bandwidth of 1.5 kHz. Since the control voltage is limited to around 2.1V, it requires a level shifter to get the entire pull range on the VCXO. National's LMC7101 is recommended with 100kΩ and 182kΩ resistors as shown in Figure 1 to provide a gain of 1.55, sufficient to drive a 3.3V VCXO.

Dual VCXOs require some supporting logic to select the appropriate VCXO. This requires the use of Format[4] (SD/HD) and Lock Detect, which are mapped at power-on to I/O Port Bit 3 and I/O Port Bit 4 of the LMH0031, respectively. These two signals pass through an AND gate (Fairchild Semiconductor's NC7SZ08 or similar). Its output is high when both Lock Detect and Format[4] are high, which indicates a valid high-definition signal is present. The VCXOs are buffered to control the transition times and to allow easy selection. The output of the AND gate is used to control the Output Enable (OE) function of the buffers. The 74.25 MHz VCXO is buffered with the NC7SZ126 with the AND gate output connected to the OE pin of the NC7SZ126, and the 27.00 MHz VCXO is buffered with the NC7SZ125 with the AND gate output connected to the $\overline{OE}$ pin of the NC7SZ125. This circuit uses the 27.00 MHz VCXO as default and enables the 74.25 MHz VCXO when a valid high-definition signal is present. The outputs from the buffers are daisy-chained together and sent to the LMH0031's V_{CLK} in addition to other devices, such as the LMH0030 SMPTE 292M/259M Digital Video Serializer.

Tested VCXOs from SaRonix (www.saronix.com) include the ST1308AAB-74.2500 for high definition and the ST1307BAB-27.0000 for standard definition. The ST1308AAB-74.1758 may be substituted for the 74.25 MHz VCXO for applications requiring a 74.1758 MHz parallel clock. Recommended VCXOs are listed in Table 2.

Table 2. Recommended VCXOs

Supplier	Web Site	VCXO Part No.		
		74.25 MHz	74.1758 MHz	27.00 MHz
SaRonix/Pericom	www.saronix.com	ST1308AAB-74.2500	ST1308AAB-74.1758	ST1307BAB-27.0000
Vectron	www.vectron.com	JDLGCEP @ 74.25MHz	JDLGCEP @ 74.1758MHz	JDLHCA @ 27MHz
Valpey Fisher	www.valpeyfisher.com	VF594L-T @ 74.25MHz	VF594L-T @ 74.1758MHz	VF294L-50 @ 27MHz

1.1 *Jitter Measurement Results*

LMH0031 V_{CLK} jitter was measured with the LMH0031 in both normal mode and VCXO mode. Jitter was also measured with the LMH0031 and LMH0030 connected back-to-back, both with and without the VCXO, in order to determine the net effect of input clock jitter on a serializer such as the LMH0030. See Figure 2 .

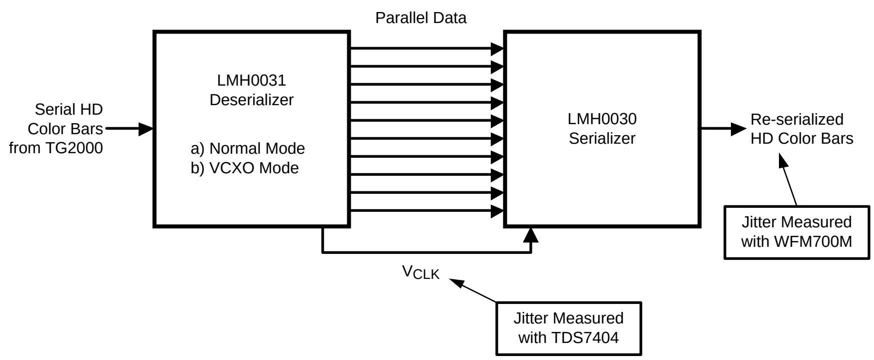

Figure 2. Jitter Measurement Setup

The Tektronix TG2000 was used to generate an HD color bar pattern (1080i/30 color bars) for the serial signal source. This was fed to the LMH0031 and deserialized, with the parallel data and clock connected directly to the LMH0030 and re-serialized. V_{CLK} jitter was measured with the Tektronix TDS7404 oscilloscope and TDSJIT3 jitter measurement software, and LMH0030 output jitter was measured with the Tektronix WFM700M set for a 100kHz high pass filter. This was done for both the normal LMH0031 operation and the LMH0031 in VCXO mode (configured as shown in Figure 1). The results are shown in Table 3.

Table 3. Jitter Measurement Results

Measurement Point	Measurement Method	No VCXO	With VCXO
V_{CLK}	TDSJIT3 Clock Period, 1K samples	656 ps_{P-P}	101 ps_{P-P}
V_{CLK}	TDSJIT3 Clock Time Interval Error (TIE), 1K samples	509 ps_{P-P}	65 ps_{P-P}
LMH0030 output	WFM700M with 100kHz HPF	434 ps_{P-P}	79 ps_{P-P}

1.2 Summary

Adding a VCXO significantly reduces jitter on the LMH0031 output clock. This also decreases the jitter in a serializer when connecting the LMH0031 and a serializer such as the LMH0030 back-to-back. It is recommended to use a VCXO to reduce jitter when using the LMH0031 back-to-back with a PLL-based serializer such as the LMH0030. However, it is unnecessary to use a VCXO with the LMH0031 in standalone mode or while using the LMH0031 to clock logic blocks or other non-PLL circuits.

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