User's Guide

How to Phase Synchronize Multiple LMX2820 Devices

ABSTRACT

In applications such as phase array antenna where the phases of multiple synthesizers must be aligned, it would be beneficial if each synthesizer can phase-align its output and input without complex and time-precision circuitry. The LMX2820 is one of the RF synthesizers in TI's product portfolio that can support phase synchronization.

In this user's guide, we will explain the theory of phase synchronization, the limitations of phase synchronization, and demonstrate how to set up synchronization in a step-by-step guide.

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Trademarks

1 Introduction

Phase synchronization of the LMX2820 means that the delay from the rising edge of the reference clock signal to the output signal is deterministic. If multiple LMX2820 devices share the same reference clock, it is possible to have all the outputs from LMX2820 devices phase-aligned. Depending on the input and output signal frequencies, a SYNC signal may be necessary to assist phase synchronization.

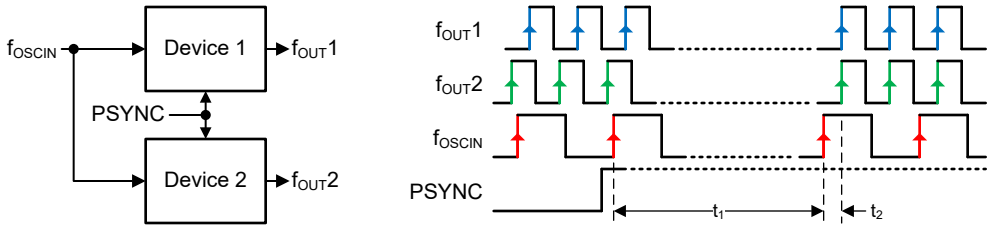

Figure 1-1. Phase Synchronization Concept

Initially, the LMX2820 devices are locked to the input reference clock (f_{OSCIN}), but are not synchronized. The user sends a synchronization pulse that is reclocked to the next rising edge of f_{OSCIN}. After a certain time (known as t_1), the phase relationship from f_{OSCIN} to f_{OUT} will be deterministic. t_1 is dominated by the sum of the VCO calibration time, the analog setting time of the PLL loop, and the register MASH_RST_COUNT, if used in fractional mode. t_2 is the deterministic delay between f_{OSCIN} and f_{OUT} after synchronization.

2 SYNC Category

The requirements for phase synchronization depend on certain LMX2820 setup conditions. To use phase synchronization, first determine the SYNC category using the flow chart below.

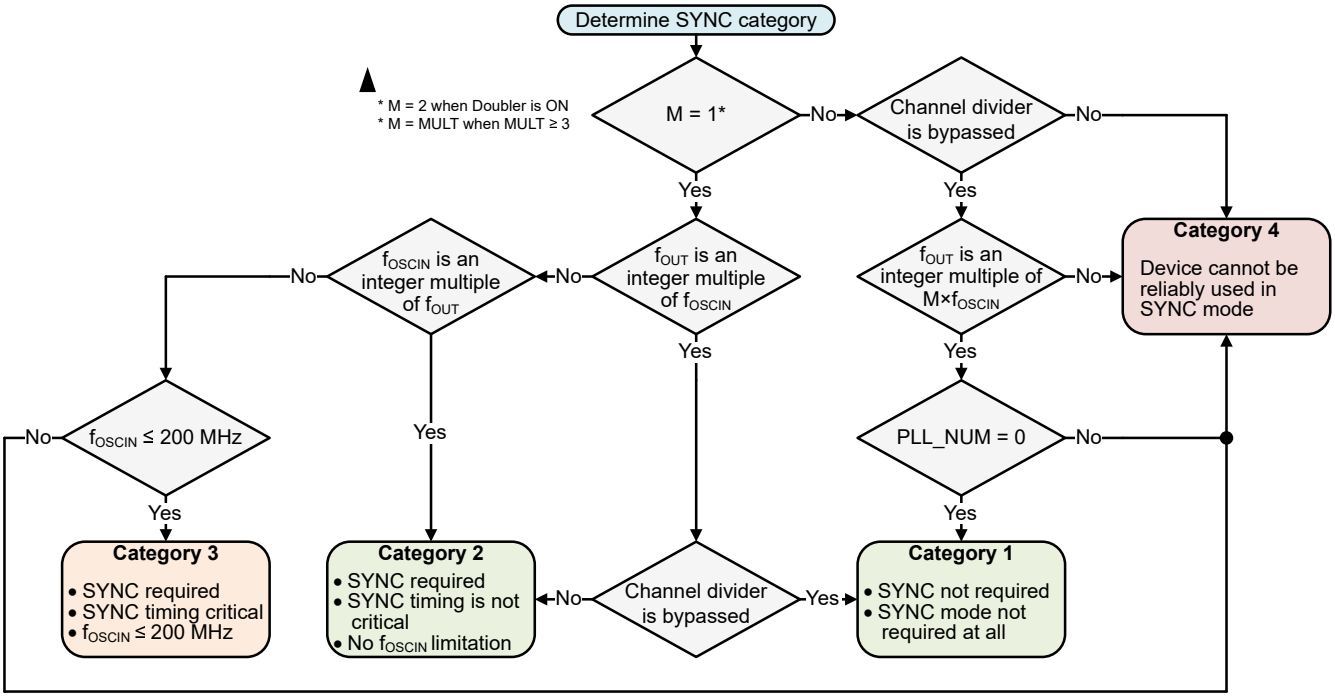

Figure 2-1. SYNC Category Flow Chart

For Category 1 SYNC, there is no restriction at all. We do not need to enable SYNC mode (that is, we can keep register PHASE_SYNC_EN = 0). A SYNC signal is also not required.

In Category 2 SYNC, we must make PHASE_SYNC_EN = 1 and provide a SYNC signal to LMX2820. The SYNC signal is not time-critical, therefore a Low-to-High transition at the PSYNC pin is good enough.

When the LMX2820 configuration falls into Category 3 SYNC, we need both PHASE_SYNC_EN = 1 as well as a time-critical SYNC pulse. The setup and hold time of the SYNC pulse as specified in the data sheet must obey.

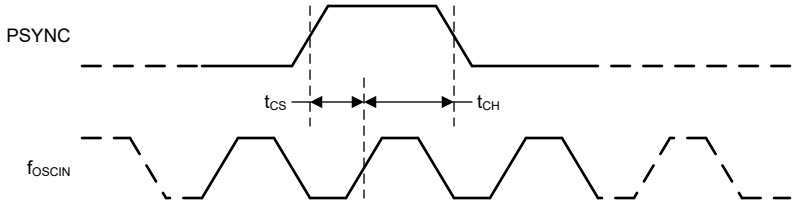

Figure 2-2. Time Critical SYNC Pulse

From the data sheet, the minimum t_{CS} and t_{CH} is 2.5 ns and 2 ns, respectively. Furthermore, the maximum f_{OSCIN} is restricted to 200 MHz.

A reliable phase synchronization is not possible if the configuration of LMX2820 does not fall into the above categories.

3 SYNC Examples

In the following sections, we can see how to synchronize the outputs from two LMX2820 devices. Below is the block diagram of the test setup.

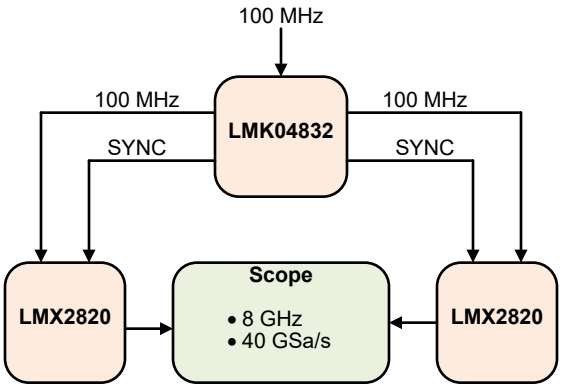

Figure 3-1. Test Setup

The LMK04832 is operated in Single Loop Mode. That is, PLL1 is not used. PLL2 takes the 100-MHz input clock to lock the VCO. Output from the VCO is divided down to 100 MHz, which is used as the reference clock of the LMX2820. SYSREF of the LMK04832 is used to generate a time-critical SYNC pulse for Category 3 SYNC.

The LMK04832 is able to phase align all of the output clocks. All the clocks and SYNC pulses are phase-aligned before feeding them to the LMX2820 devices.

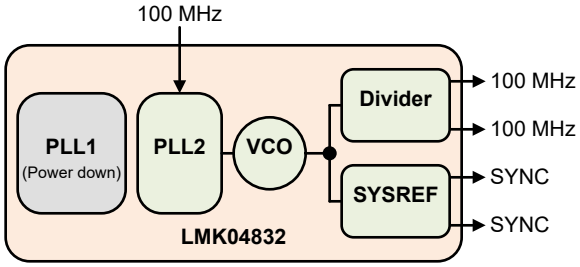

Figure 3-2. LMK04832 Configuration

The output channel-to-channel skew of the LMK04832 is around 100 ps. As such, the two 100-MHz clocks are not exactly in phase. This skew is eventually carried forward to the output of the LMX2820 devices. For better illustration purpose, the data in the following sections has this skew written off.

3.1 Category 1 SYNC Example

The following is a Category 1 SYNC configuration, because:

- M = 1 (Doubler and MULT are not used)

- f_{OUT} is an integer multiple of f_{OSCIN} (6000 / 100 = 60)
- Channel divider is bypassed (output frequency = VCO frequency)

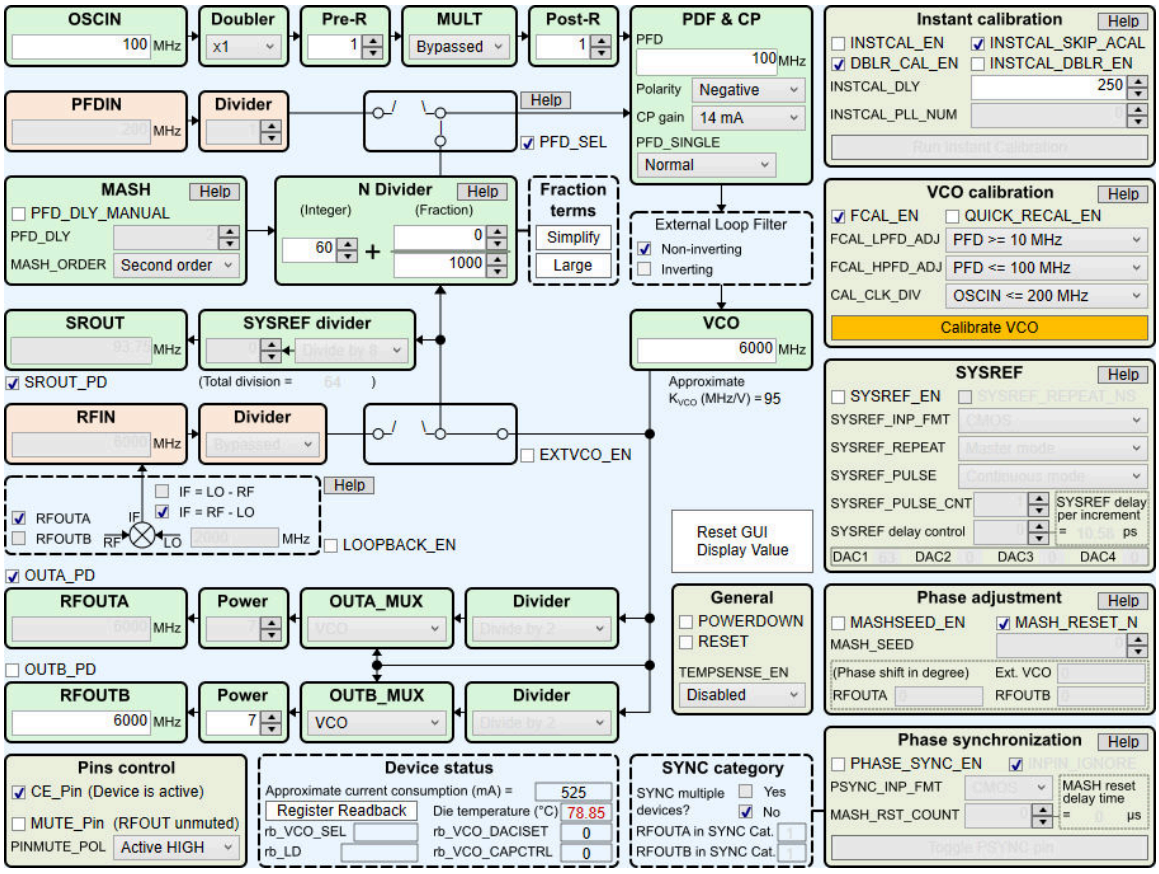

Figure 3-3. Category 1 SYNC Configuration

With this configuration, the outputs are in phase after programming the LMX2820 devices. The output phases remain constant if:

- LMX2820 is powered down and powered up again
- VCO is calibrated again
- LMX2820 is reset and re-programmed

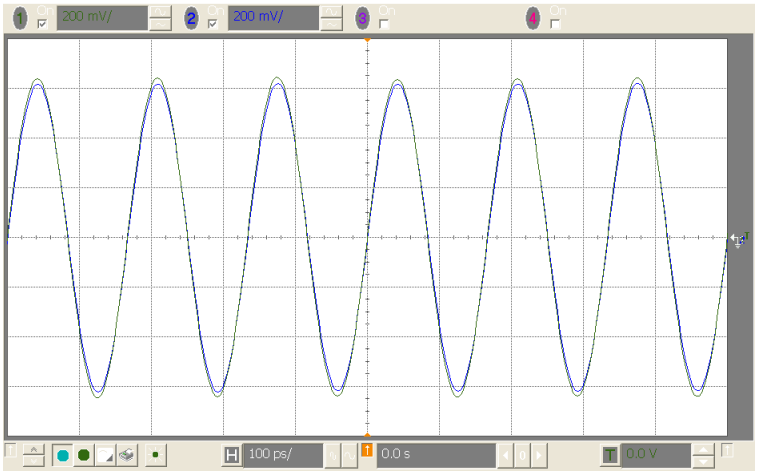

Figure 3-4. Category 1 SYNC Result

Below is another Category 1 SYNC configuration example. This configuration has enabled the Doubler:

- M = 2 (Doubler is enabled)

- Channel divider is bypassed
- f_{OUT} is an integer multiple of M × f_{OSCIN} (6000 / 200 = 30)
- PLL_NUM = 0

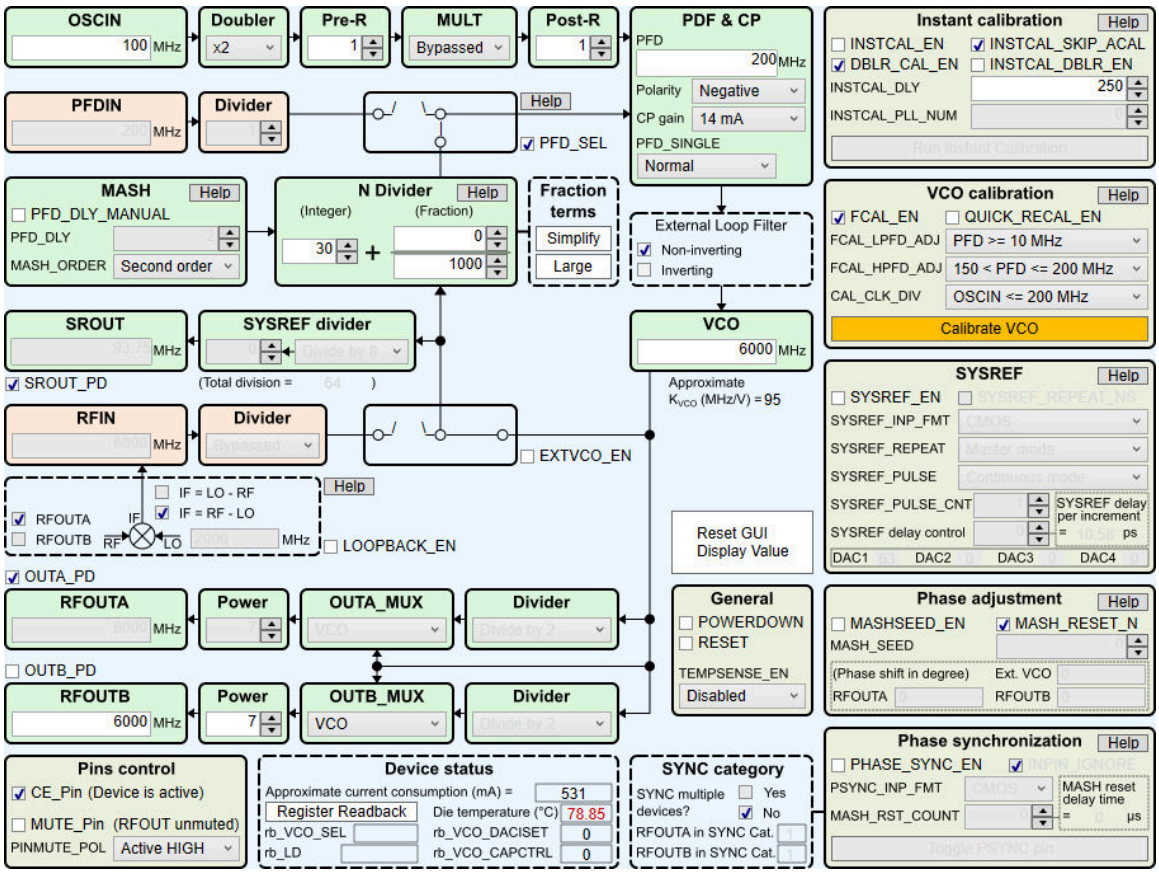

Figure 3-5. Category 1 SYNC With Doubler

If only one of the LMX2820 devices has the Doubler enabled, although both configurations are Category 1 SYNC, the Doubler introduces addition delay in the input path. This delay is carried forward to the output. As a consequence, the phases of the LMX2820 outputs are not exactly in phase. To get exact phase match between multiple LMX2820 devices, the configurations should be identical.

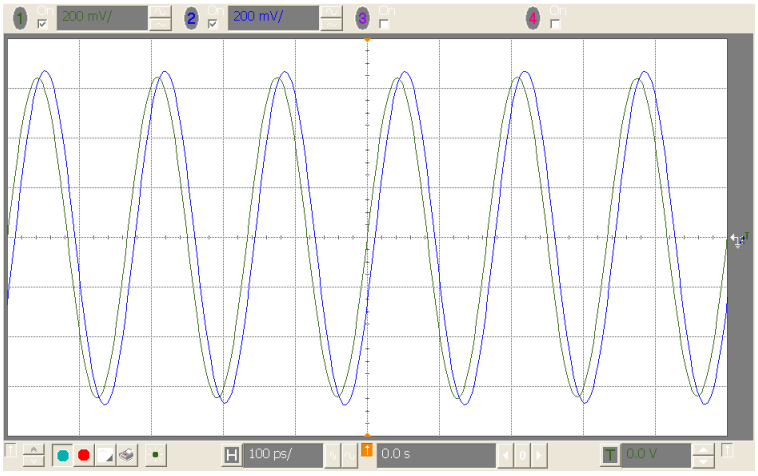

Figure 3-6. Phase Offset Due to Unsymmetrical Configuration

3.2 Category 2 SYNC Example

According to the SYNC category flow chart, there are two possible paths that a configuration can fall into Category 2 SYNC.

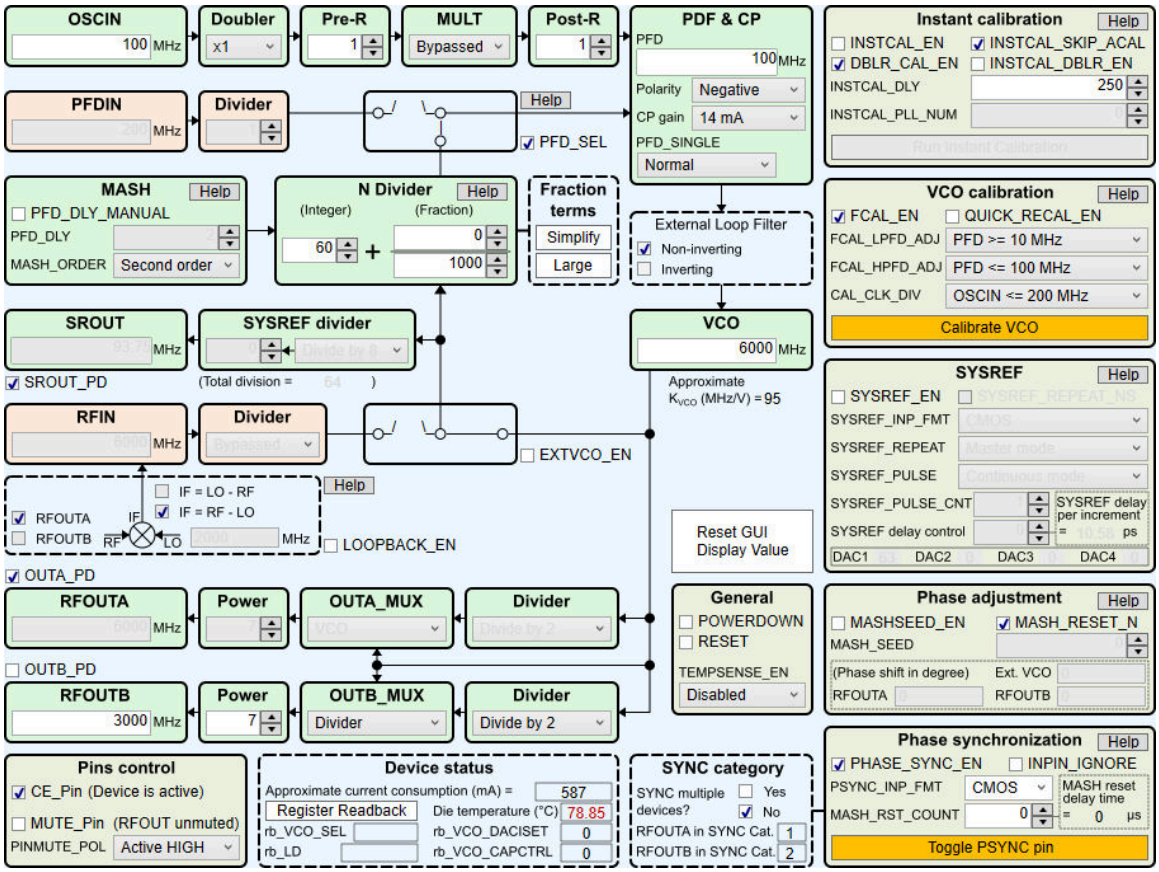

Figure 3-7. Category 2 SYNC Configuration

The above configuration is a Category 2 SYNC, because:

- M = 1
- f_{OUT} is an integer multiple of f_{OSCIN} (3000 / 100 = 30)
- Channel divider is not bypassed

With the channel divider set to divide by 2, there are two possible output phases: 0° or 180° (read the application note in Section 5 for details). In other words, every time we setup the test, we have a 50% chance that both LMX2820 devices are phase-aligned.

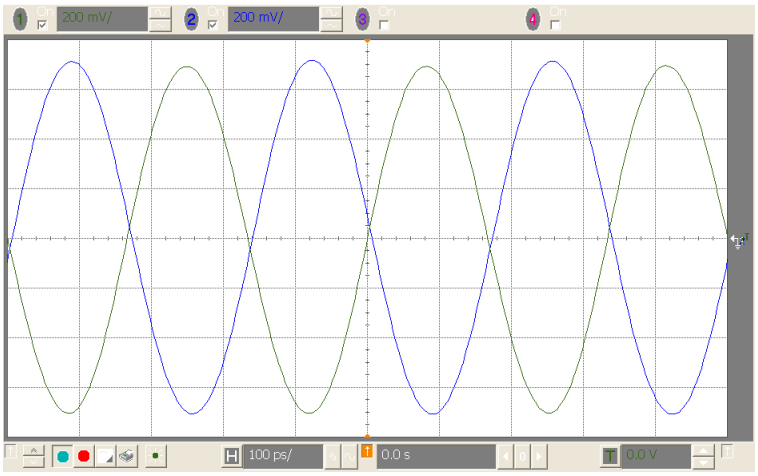

Figure 3-8. Before Phase Synchronization

To get both LMX2820 devices phase synchronized, first we must put both devices in SYNC mode and set PHASE_SYNC_EN = 1. We require a SYNC pulse to trigger phase synchronization, therefore set INPIN_IGNORE = 0 to activate the PSYNC input pin (pin 5). The timing of the SYNC pulse is not important. As long as there is a Low-to-High transition at PSYNC pin, the synchronization process is executed. If we are using TICS Pro and USB2ANY to control the LMX2820 EVM, we can press the *Toggle PSYNC pin* button once and the USB2ANY will set the PSYNC pin from Low to High and then High to Low.

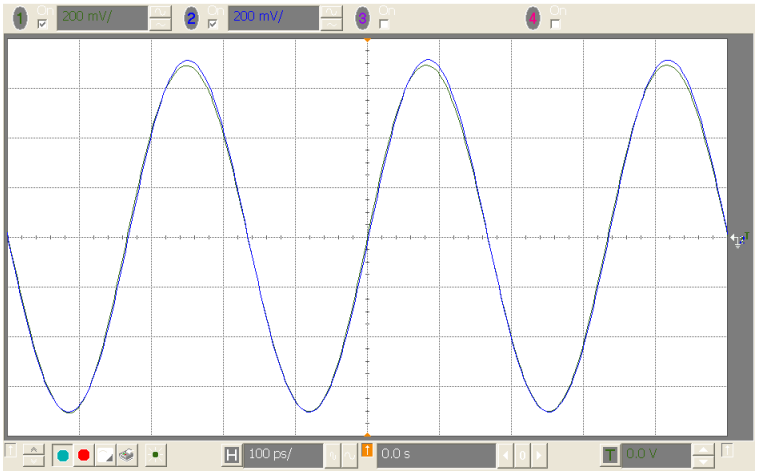

Figure 3-9. After Phase Synchronization

Below is another Category 2 SYNC example. This time, the output frequency is smaller than the reference clock frequency:

- M = 1
- f_{OUT} is not an integer multiple of f_{OSCIN}
- f_{OSCIN} is an integer multiple of f_{OUT} (100 / 50 = 2)

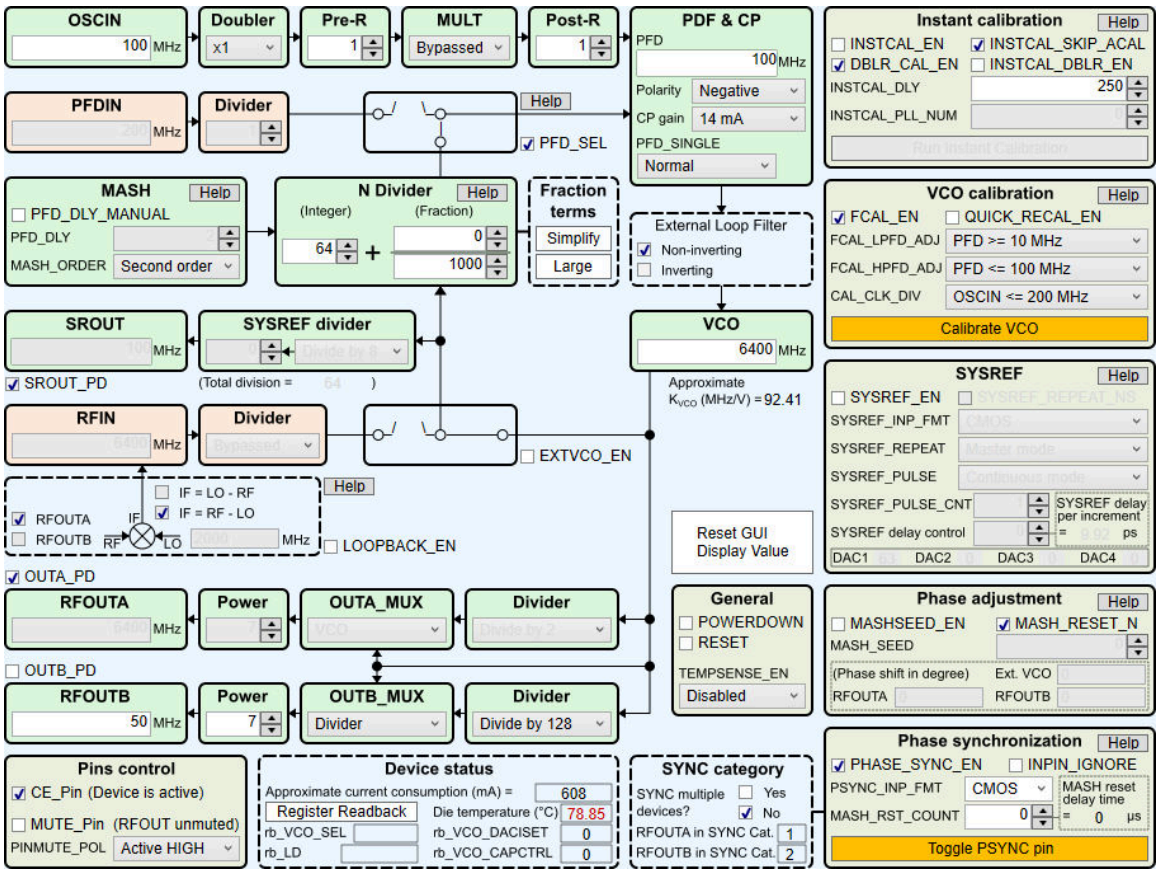

Figure 3-10. Another Category 2 SYNC Configuration

The output is heavily divided down to 50 MHz, therefore there are many possible phase relationships between the two LMX2820 devices.

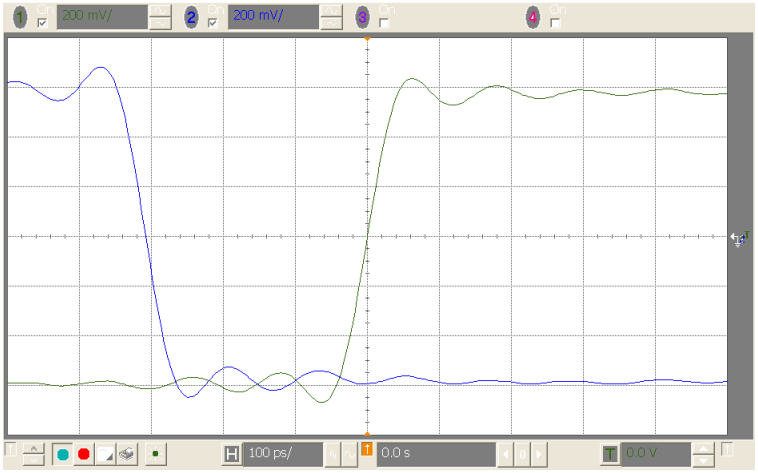

Figure 3-11. Possible Phases Before Synchronization

Again, a non-timing critical SYNC pulse is required to get the outputs synchronized.

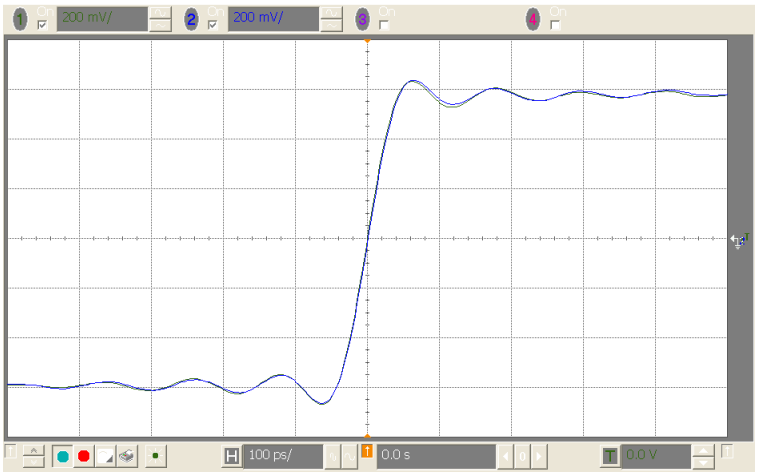

Figure 3-12. Phases Matched

In Category 2 SYNC, the LMX2820 devices must be synchronized again if:

- LMX2820 is powered down and powered up again
- VCO is calibrated again
- LMX2820 is reset and re-programmed

3.3 Category 3 SYNC Example

When the LMX2820 configuration comes to a fractional channel, the category of SYNC is likely 3, if not 4.

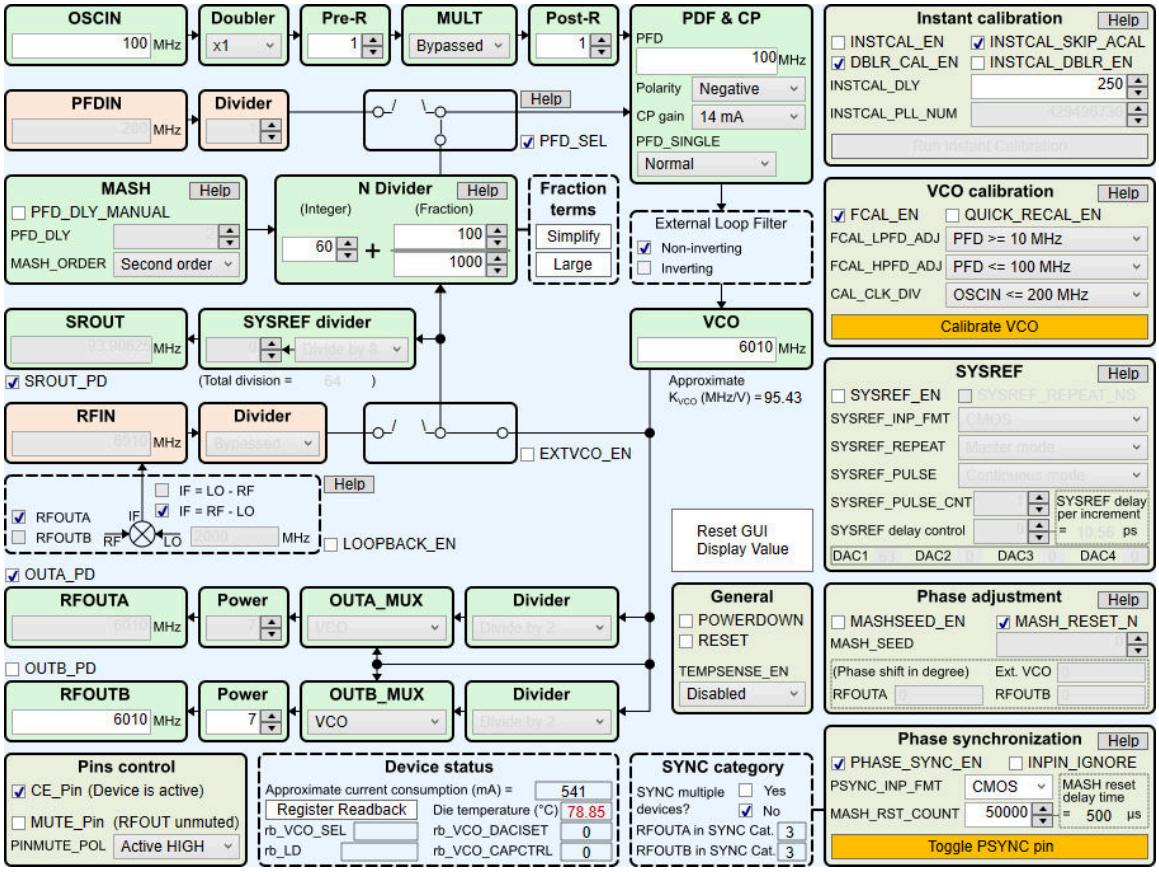

Figure 3-13. Category 3 SYNC Example

- M = 1
- f_{OUT} is not an integer multiple of f_{OSCIN}

- f_{OSCIN} is not an integer multiple of f_{OUT}
- f_{OSCIN} is less than 200 MHz

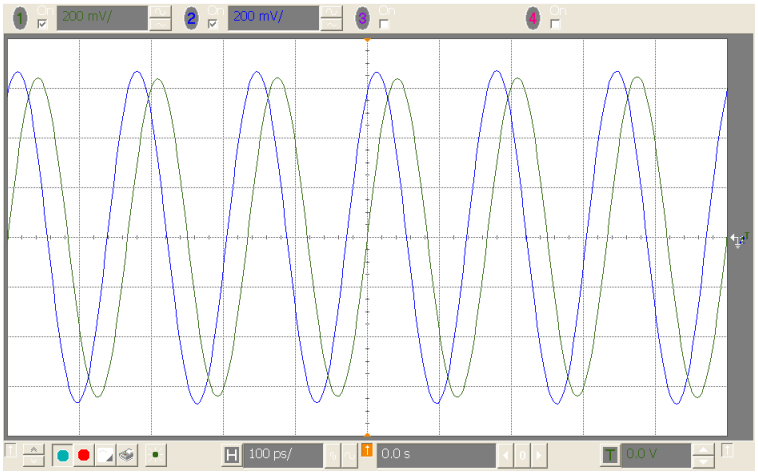

Figure 3-14. Category 3 SYNC (Before SYNC)

Similar to Category 2 SYNC, we must put the LMX2820 in SYNC mode (set PHASY_SYNC_EN = 1) and activate the PSYNC pin (set INPIN_IGNORE = 0). Furthermore, we also must "reserve" some delay time for the synchronization engine to align phase. This delay time, as defined in register MASH_RST_COUNT, must be sufficiently large or otherwise the synchronization engine is not able to complete phase alignment before time out. Delay time = MASH_RST_COUNT × $2^{CAL\_CLK\_DIV}$ / f_{OSCIN}. A 500-µs delay time is recommended. This is not an absolute wait time that adds to the total time taken for phase synchronization (t_1 in Figure 1-1). Depending on the LMX2820 configuration, the phase synchronization engine may actually require a 100-µs or 200-µs delay time, for example. That would mean t_1 is 100 µs shorter if, for a certain configuration, the phase synchronization engine only requires a 100-µs instead of a 200-µs delay time.

As for the SYNC pulse, this example requires a time-critical SYNC pulse to phase synchronize the LMX2820 devices. We cannot use the *Toggle PSYNC pin* button in TICS Pro anymore.

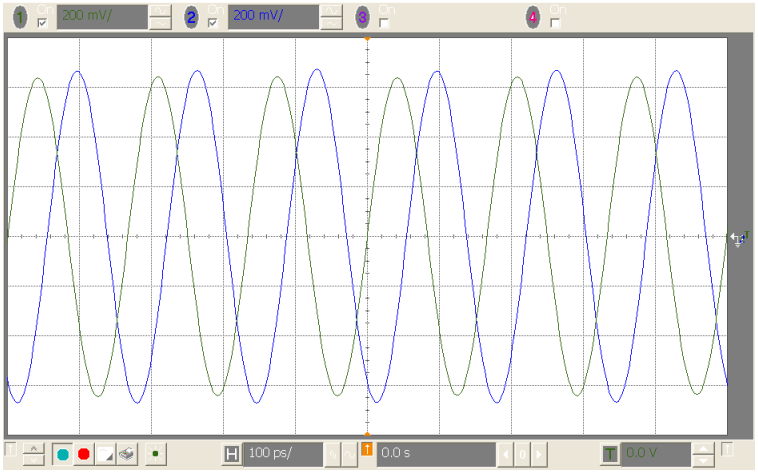

Figure 3-15. Unable to SYNC With Non-Time Controlled SYNC Pulse

The LMK04832 device in Figure 3-1 is used to generate the time-critical SYNC pulse.

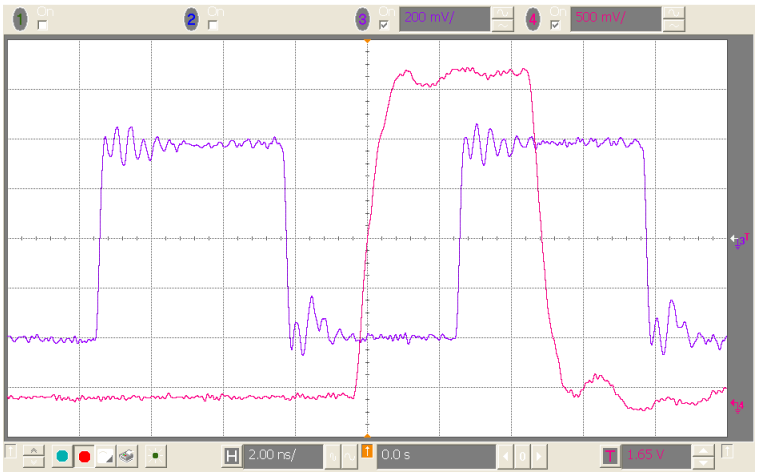

Figure 3-16. Time-Critical SYNC Pulse

After synchronization with a time-critical SYNC pulse, both LMX2820 outputs are in phase again.

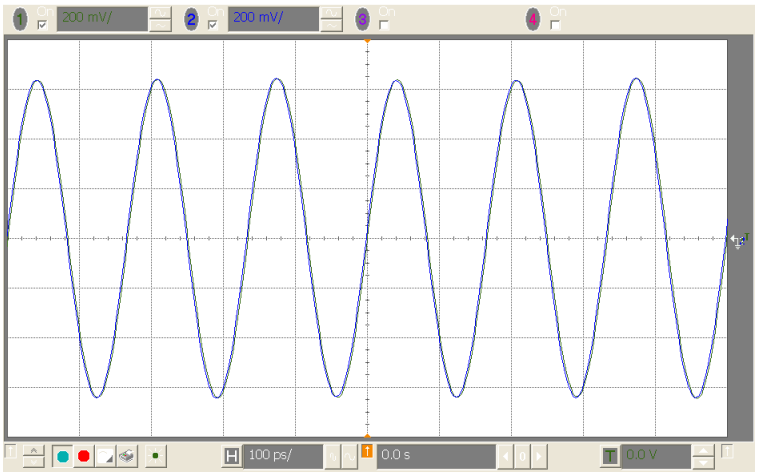

Figure 3-17. Category 3 SYNC (After SYNC)

As a reminder, toggling the POWERDOWN bit, a RESET, or a VCO calibration requires re-synchronization with a time-critical SYNC pulse.

4 Other Considerations When Using SYNC

1. Without VCO Calibration:

   The LMX2820 supports faster VCO frequency switching without a VCO calibration. This can be implemented manually (like in full-assist mode) or automatically (Instant Calibration). When the LMX2820 operates in these modes, phase synchronization is still supported with a slightly different behavior or with some additional requirements.

   Category 1 SYNC:

   - Input-output phase may shift after a POWERDOWN cycle. This problem can only be fixed by doing a RESET and then programming all the registers once.
   - Input-output phase remains deterministic after VCO frequency is changed.

   Category 2 and 3 SYNC:

   - Synchronization requires register FCAL_EN = 1. Before feeding the SYNC signal to LMX2820, program register R0 with FCAL_EN = 1.

2. MASH_RST_COUNT:
   - Can be equal to 0 when PLL_NUM = 0.
   - Must be sufficiently large when PLL_NUM is not equal to 0.

3. Use both RF Outputs:

   When both outputs are used and the frequencies are not identical, the category of SYNC on each output can be different. Provide the appropriate SYNC pulse according to the highest SYNC category output.

5 References

- Texas Instruments, *LMX2820 22.6-GHz Wideband PLLatinum™ RF Synthesizer With Phase Synchronization and JESD204B Support* data sheet
- Texas Instruments, *LMK04832 Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner With Dual Loop PLLs* data sheet
- Texas Instruments, *Phase Synchronization with Multiple Devices and Frequencies* application note

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