ADC10080

High Performance, Scalable ADC Solves Many Circuit Problems Without the Expense of Power

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Technology Edge

High Performance, Scalable ADC Solves Many Circuit Problems Without the Expense of Power

By: Bob LeBoeuf, Application Engineer

ADCs are finding themselves in an increasingly vast number of applications. This increases the demand for versatility, and of course, the demand for lower and lower power. Certain systems may require certain dynamic ranges on the input of the ADC, and it is usually preferred not to scale the input voltage. Amplifying the input signal offers challenging THD and bandwidth issues, and attenuating typically lowers the SNR, and may pose transmission line problems. In battery applications, lower power consumption becomes a dominating concern, and powering down the ADC becomes attractive. In the digital domain, an ASIC designer might prefer the option of a 2's complement data format instead of the traditional offset binary format. The ADC10080 offers solutions to many of these problems, without the expense of high power.

The ADC10080 is a 10-bit, 80 MSPS analog-to-digital converter that consumes only 78.6 mW (Typ) of power. It has a high degree of versatility, which is best summarized by the circuit shown in Figure1:

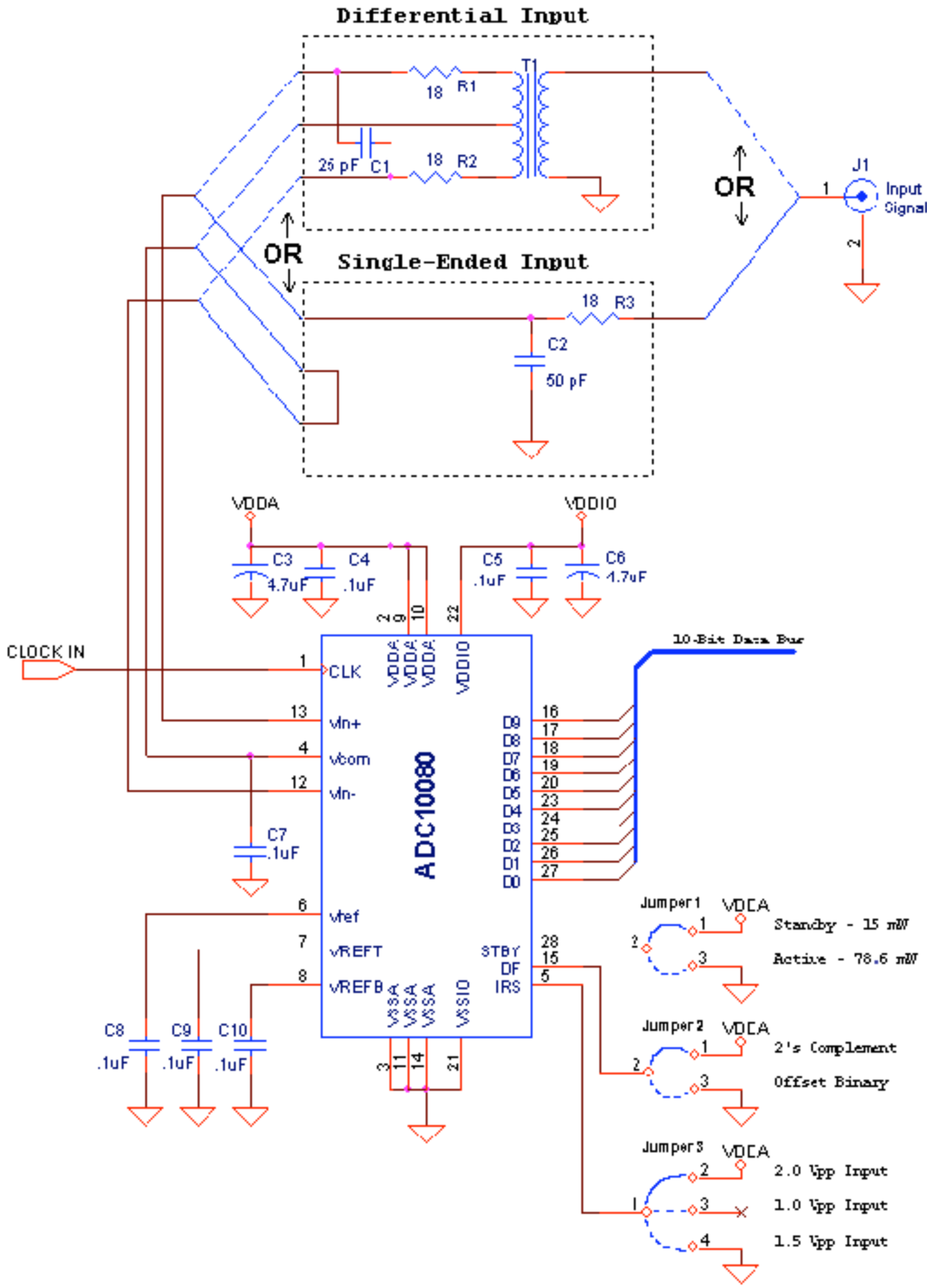

Figure 1

The input may be driven differentially, or single-ended, as shown in the top part of Figure 1. For a differential signal, a center-tapped transformer is sometimes employed because the center tap may be used to bias the input signal to the common mode voltage. This voltage is supplied by the chip at pin 4 (VCOM). R1, R2 and C1 form a low-pass filter that is used to limit the noise input. The -3 dB roll off occurs at 1/(2*p*(R1+R2)*C1). C1 also serves the purpose of dampening the charge 'kick-back' present in most ADCs.

For a single-ended input, the VIN- is tied to VCOM, and VIN+ is used for the input signal. A simple RC low pass filter (R3 &

C2) may be used to address the noise cut off, and charge kick-back.

In addition to the choice of differential or single-ended input, the peak-to-peak voltage is scalable using pin 5 (IRS - Input Range Select). By adjusting jumper 3, 2 V, 1.5 V or 1 V peak-to-peak is realized. The part may be powered down to 15 mW by applying VDDA to pin 28 (STBY - Standby).

The output format may be 2's complement, or offset binary by applying VDDA or VSSA to pin 15 (DF - Data Format) respectively. Each output data format has its advantages. The offset binary offers a simple direct scale that is proportional to the magnitude of the peak-to-peak input voltage. In some cases, it might be easer to divide the scale in half and assign the upper half to represent negative numbers. This would mean if the MSB is a '1', the number is negative, and the remaining 9 bits are understood to be the complement of the number. This is what the 2's complement format offers. A binary output of 0000000000 through 0111111111 is straight binary as usual, and maps to 0 through 511 in decimal. A 1000000000 through 1111111111 maps to -512 through -1 in decimal. An advantage to using the 2's complement scale is that subtracting two numbers can now be done by adding.

The ADC10080 also has a well-placed tod specification to make it easy to capture the data. Figure 2 shows typical data lines and the clock:

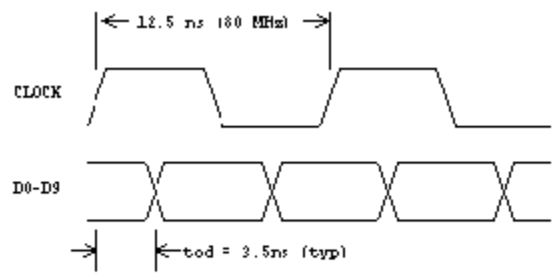

Figure 2

With all of these combinations available, the ADC10080 is suitable for many applications, including DTV, ultrasound, basestations, or general data acquisition. High performance specifications are preserved for even the most demanding systems, while consuming only 78.6 mW (Typ) of power.

For more information visit the ADC10080 product folder.

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