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Introduction

The *Analog Applications Journal* (AAJ) is a digest of technical analog articles published quarterly by Texas Instruments. Written with design engineers, engineering managers, system designers and technicians in mind, these “how-to” articles offer a basic understanding of how TI analog products can be used to solve various design issues and requirements. Readers will find tutorial information as well as practical engineering designs and detailed mathematical solutions as they relate to the following applications:

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AAJ articles include many helpful hints and rules of thumb to guide readers who are new to engineering, or engineers who are just new to analog, as well as the advanced analog engineer. Where applicable, readers will also find software routines and program structures and learn about design tools. These forward-looking articles provide valuable insights into current and future product solutions. However, this long-running digest also gives readers archival access to many articles about legacy technologies and solutions that are the basis for today’s products. This means the AAJ can be a relevant research tool for a very wide range of analog products, applications and design tools.

Adjusting the soft-start time of an integrated power module

By Chris Glaser

Member Group Technical Staff, Low-Power DC/DC

Introduction

With the shrinking amount of available board area and the trends for shorter design times, power modules are becoming increasingly common in the industrial market. Power modules in test and measurement devices, programmable logic controller (PLC) systems and optical modules can shorten design time by reducing design effort so that engineers have more time to devote to other design tasks.

A power module integrates much of the power-supply circuitry, including some components that are normally external to the power-management integrated circuit (IC). A power module may include one or both power MOSFETs, the control loop compensation, the power inductor, the input and output capacitors, and so on. The result of all this integration is that power modules do simplify the design. However, because of their small physical size and limited pin count, a power module may have fewer features than an equivalent discrete-IC power supply.

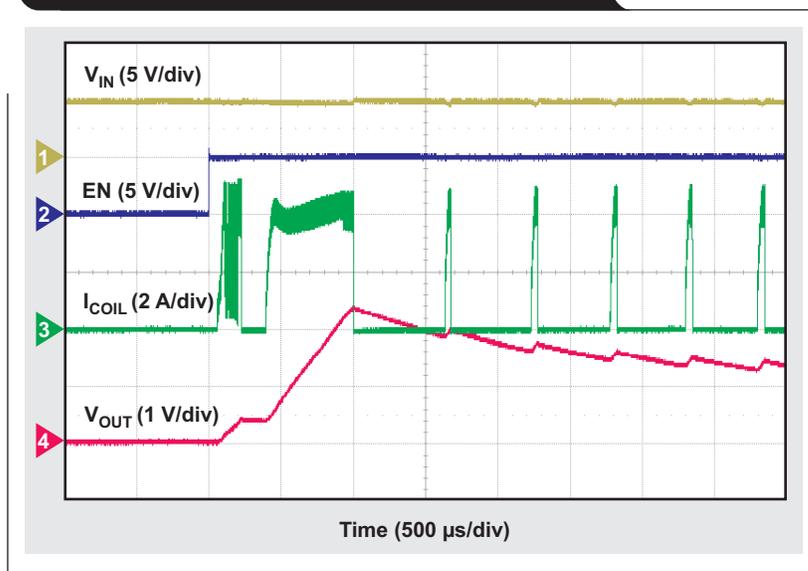
One example is the ability to adjust the soft-start time. This is fixed inside many power modules but may be configurable through a soft-start (SS) pin on a discrete-IC power supply. This fixed soft-start time, also known as output-voltage slew rate, may create unacceptable behaviors in certain applications—particularly in FPGAs, which have lots of output capacitance or may draw large currents during the soft-start time. Even with the integration of a power module, there are still several external circuits that can provide clean, acceptable soft-start times in such applications.

The challenge: Soft-start time is too long or too short

When designing with a power module with a fixed soft-start time, it is possible that the soft-start time creates an output-voltage slew rate that is unacceptable for a particular load on the output bus. For example, an FPGA may require that its input voltage rise has a slew rate of 1 mV/μs ±50%. Since its input voltage is the output voltage of the power module, this dictates the power module's soft-start time, which may be either too long or too short for the FPGA specification.

A different scenario occurs when there is no specific slew-rate requirement, but certain application conditions

Figure 1. Example of soft-start output into a 1-A load with two 470-μF output capacitors



converge to create a system-startup issue. Figure 1 shows the startup of a power module with a 5-V input voltage, the output voltage set to 2.5 V, and two 470-μF capacitors added to the output.^[1] With a 1-A resistive load added to the output, the output voltage never enters regulation because of current-limit and hiccup current-limit protection. Thus, the device remains in hiccup current-limit operation.

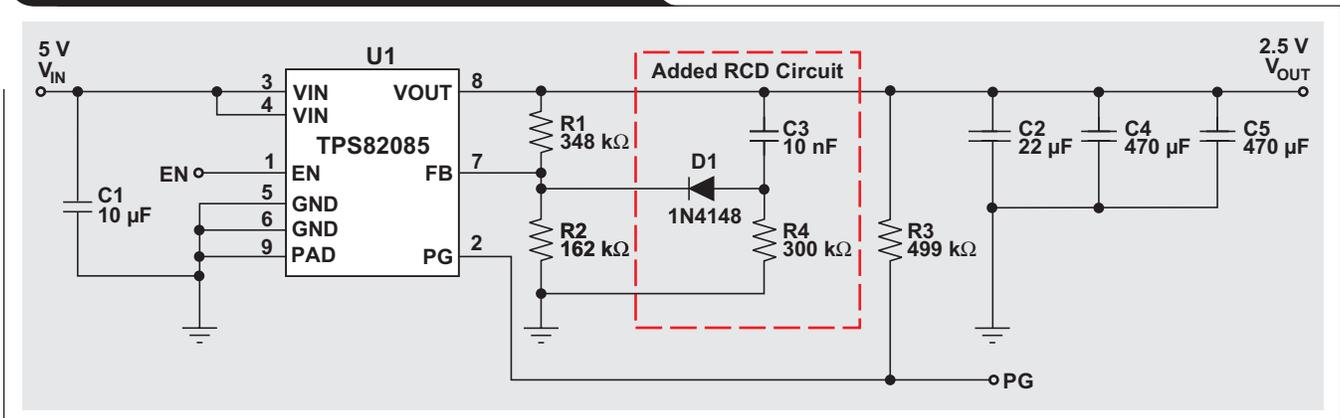
The device's internal soft-start time is fixed at 800 μs. The device tries to ramp up the output voltage from 0 V to its set point in this time. This requires charging the output capacitance, which creates an output current shown by Equation 1.

$$I_{\text{OUT(Cap)}} = C_{\text{OUT}} \times \frac{dV}{dt} \quad (1)$$

where dV is the output voltage, dt is the soft-start time, and C_{OUT} is the total output capacitance. From the measured setup described above, the total C_{OUT} is 962 μF (including the 22-μF ceramic capacitor already on the output). Therefore, the output current into just the output capacitance is about 3 A.

The 1-A load current is added to this amount to obtain the entire output current of the power module. To determine the peak inductor current for the module's peak current-limit topology, half of the inductor ripple current must be added to the total output current. This value is

Figure 2. Power module with RCD circuit added



well above the 3.7-A minimum current-limit value specified in the data sheet and near the 4.6-A typical current-limit value. Figure 1 confirms this through the I_{COIL} waveform, which shows currents above 4 A. Clearly, this 3-A rated device is reaching its current limit.

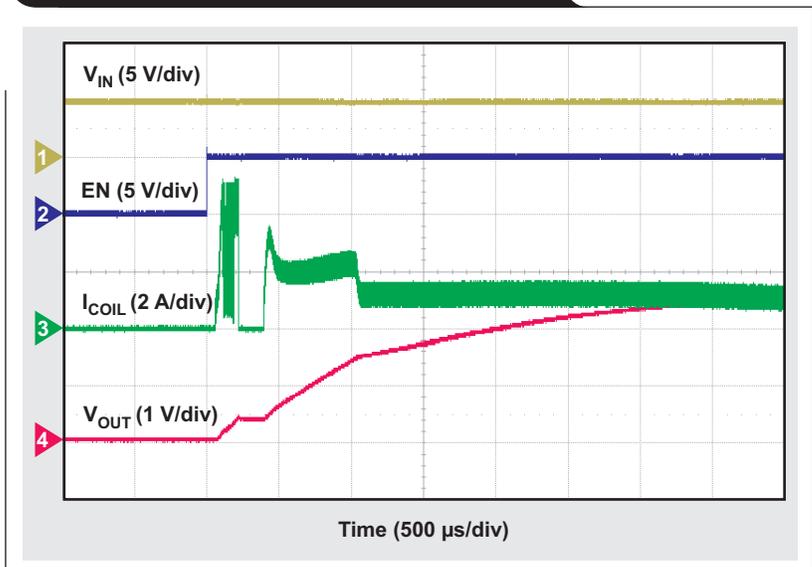
For some devices, reaching current limit during startup simply extends the soft-start time since the device operates in current limit instead of entering hiccup operation. The output voltage enters regulation for these devices. This power module behaves differently because it incorporates the hiccup current-limit protection. This type of protection turns off the device for a fixed time during a current-limit event, which limits the power dissipation and corresponding temperature rise. This keeps the overall system safer for the user in a severe fault condition. However, the fixed off-time of the hiccup current limit creates a problematic condition during startup such that the device gets stuck and the output voltage never enters regulation.

In summary, devices with hiccup current limit and a fixed soft-start time may have difficulty starting if there is a large amount of output capacitance or a heavy load present during startup.

Solution #1: A resistor, capacitor, and diode extend the soft-start time

In applications where the soft-start time needs to be lengthened, a resistor, capacitor, and diode (RCD) circuit are added around the feedback (FB) pin in order to bias the FB pin higher and slow the startup.^[2] The resistor and capacitor values are empirically tuned to lengthen the soft-start time enough for a specific application configuration. Figure 2 shows the tested schematic and Figure 3 shows the resulting startup waveform. The device enters regulation because the output-voltage slew rate and corresponding peak inductor current is reduced.

Figure 3. Soft-start with RCD circuit added



The advantage of this circuit is its simplicity, flexibility and low cost. Just three small, commodity components are required and the circuit is tunable for nearly any configuration. However, this circuit has three main disadvantages:

- This circuit only increases the soft-start time, but cannot reduce it.
- The power good (PG) output is activated before the output voltage is in regulation. Because the RCD circuit adds a voltage onto the FB pin, and this is where the PG threshold is measured. Thus, the FB and PG circuits see a voltage higher than the actual output voltage and react accordingly.
- The device still reaches its hiccup current limit, as shown by the flat part of the output-voltage ramp at around 500 mV. Since the diode does not conduct at such low voltages, the soft-start extension circuit has no effect until the output voltage is high enough. While the output voltage ramp is still mostly monotonic, this particular step may not be acceptable for all loads.

While this solution uses the same power module IC plus some extra circuitry, these disadvantages may not make it usable for every application.

Solution #2: Use a power module with soft-start time control

The best technical solution for adjusting the soft-start time may be using a power module with an externally adjustable soft-start time. This allows adjusting the soft-start time slower or faster for almost any application configuration that specifies output-voltage slew rate. The TPS82130 is such a module that also delivers 3 A of current in the same size device. However, it is not pin-to-pin compatible due to the different feature set. Figure 4 shows its smooth startup into the same 1-A load with two 470- μ F output capacitors and a 6.8-nF soft-start capacitor.

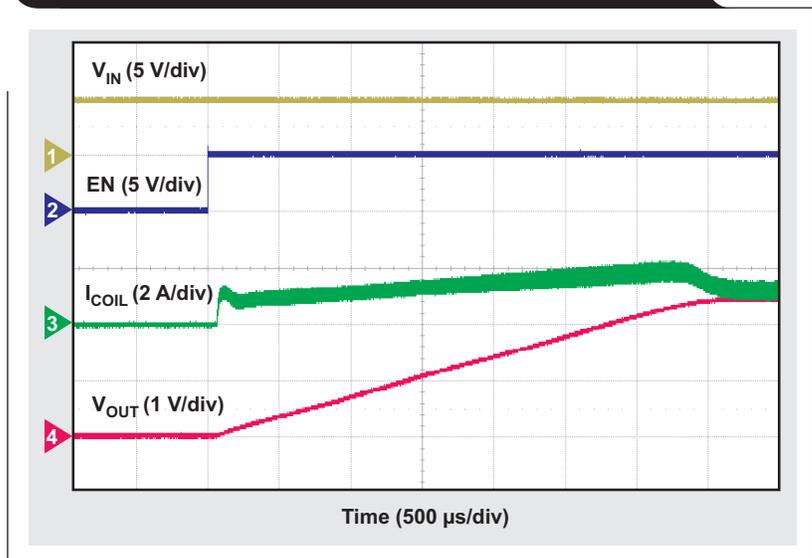
While a different power module IC addresses nearly all soft-start time concerns, there may be some disadvantages. Comparing the TPS82130 to the TPS82085, the extended input voltage range of the TPS82130 presents these downsides: lower efficiency, higher cost, taller height, and larger quiescent current (I_Q).^[3] These are the trade-offs made when selecting a different device.

Both of these power modules use the DCS-Control™ topology.^[4] This topology, though internally compensated, is very tolerant of larger output capacitances.^[5] Therefore, control-loop stability does not typically limit the performance with larger output capacitors. This is not always the case for other control topologies.

Solution #3: Use a load switch to decouple loads and adjust soft-start time

A third solution uses a load switch to decouple the load from the power module. With this solution, the power

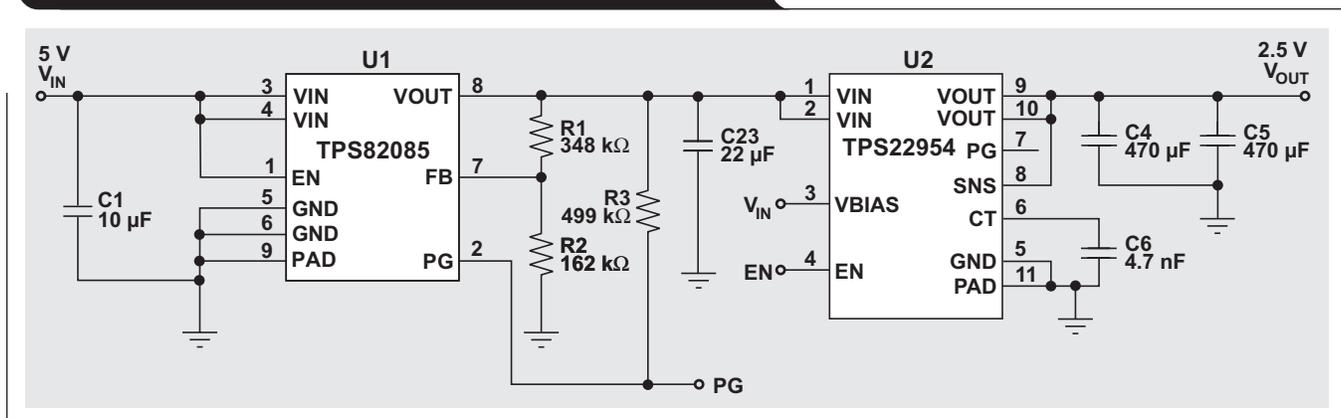
Figure 4. Power module with adjustable soft-start time



module can start up as usual without the heavy load current or the large amount of output capacitance. Alternatively, the power module can remain always on because the load switch will provide the soft-start function. Figure 5 shows an example implementation with an always on power module and the TPS22954 load switch.

A load switch with an adjustable soft-start time provides the same advantages as solution #2. Also, a load switch is useful for removing leakage currents of the load from the output voltage to reduce the standby power consumption of the system. The primary disadvantages are added cost and board area of another IC, reduced efficiency due to the conduction losses in the load switch, and decreased output voltage because of the voltage drop across the load switch. However, for systems late in the design phase and unable to make major changes to the power module device, a load switch is the simplest option to solve a soft-start issue.

Figure 5. A load switch decouples the load from the power module and adjusts the soft-start time



Conclusion

Even with all the integration in modern power modules, engineers still have flexible solutions to overcome difficult soft-start problems found in many FPGA-based and other industrial systems with large capacitances or high startup currents. Simple and low-cost application circuits, other power-module ICs, and load switches are each able to address certain startup requirements. These options, in addition to others not listed here, are readily available to balance the trade-offs made in every design.

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Related Web sites

Product information:

TPS82085

TPS82130

TPS22954

How to select input capacitors for a buck converter

By Manjing Xie

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Introduction

Electromagnetic interference (EMI) can create serious issues for manufacturers in an industrial environment. A buck converter generates a pulsating ripple current with high di/dt at the input. Without input capacitors, ripple current is supplied by the upper power source. Printed circuit board (PCB) resistance and inductance causes high-voltage ripple that disrupts electronic devices. The circulating ripple current results in increased conducted and radiated EMI. Input capacitors provide a short bypass path for ripple current and stabilize bus voltage during a transient event.

In recent years, the advancements in power-MOSFET technology have dramatically increased switching frequency and gate driving speeds of switch-mode power supplies. Therefore, reducing the input-voltage ripple of a buck converter has become more challenging. This article uses a buck converter as an example to demonstrate how to select capacitors to achieve optimal performance.

Figure 1 shows the basic circuit of a buck converter. The converter input current (i_{IN_D}) consists of an alternating ripple current (Δi_{IN_D}) and DC current (I_{IN_DC}).

Design parameters:

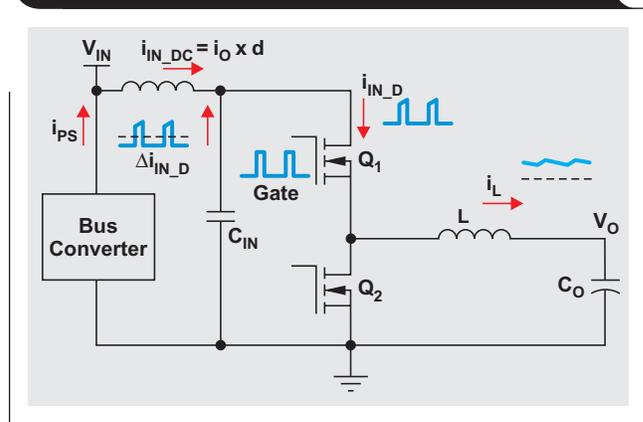
- Output voltage, $V_O = 1.2\text{ V}$
- Maximum load current, $I_O = 6\text{ A}$
- Estimated efficiency at maximum load, $\eta = 87\%$
- Switching frequency, $f_{SW} = 600\text{ kHz}$
- DC input bus voltage = 12 V with 5% tolerance
- Worst-case maximum input voltage, $V_{IN_max} = 16\text{ V}$
- Bus converter control bandwidth = 6 kHz
- Transient load step, $I_{Step} = 3\text{ A}$
- Worst-case board temperature = 75°C

Design requirements:

- Allowed input peak-to-peak ripple voltage, $\Delta V_{IN_PP} \leq 0.24\text{ V}$
- Allowed input transient undershoot or overshoot, $\Delta V_{IN_Tran} \leq 0.36\text{ V}$

The capacitor voltage rating should meet reliability and safety requirements. For this example, all input capacitors are rated at 25 V or above. The following discussion focuses on meeting electrical and thermal requirements, optimizing performance, and lowering size and cost.

Figure 1. The basic circuit of a buck converter



1. Select key ceramic capacitors to bypass input ripple current

Among the different types of capacitors, the multilayer ceramic capacitor (MLCC) is particularly good regarding allowable ripple current. A starting point is to select the key ceramic capacitors to meet the requirements for ripple voltage and current.

Table 1 shows five different ceramic capacitors that were chosen for this article. Due to DC bias capacitance degrading, the effective capacitance is not the same as the rated capacitance.

Table 1. Key electrical specifications of five ceramic capacitors

Designators	Size Code	Rated Capacitance (μF) at 0 VDC	Tolerance (%)	Temperature Code
A	SM1210	10	± 10	X5R
B	SM1206	10	± 10	X5R
C	SM0805	4.7	± 10	X5R
D	SM0603	1	± 10	X5R
E	SM0402	1	± 10	X5R

Figure 2 shows the AC current flowing through the input capacitors and the resulting voltage ripple across the ceramic capacitors, assuming the majority of the ripple current flows through these ceramic capacitors. Since the equivalent series resistance (ESR) of ceramic capacitors is very low, ripple resulting from ESR can be ignored.

Equation 1 is used to estimate the required effective capacitance that will meet the ripple requirement. The worst case for this example occurs at maximum duty cycle, which is less than 50%.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_O}{\Delta V_{IN_PP} \times f_{sw}} \quad (1)$$

Duty cycle, D, can be calculated with Equation 2. For this example, D ranges from 8.6% to 12.1% with maximum load.

$$D = \frac{V_O}{V_{IN} \times \eta} \quad (2)$$

The input capacitance should be greater than 4.43 μF as calculated with Equation 1. Taking 10% tolerance into consideration, the total effective capacitance should be greater than 4.92 μF with 12-V DC bias. Figure 3 shows the effective capacitance over DC bias of different capacitors in the inventory.

Besides the ripple-voltage requirement, the ceramic capacitors should meet the thermal stress requirement as well. A starting point is to estimate the maximum root-mean-square (RMS) of Δi_{IN_D} . Figure 4 shows the ratio of input ripple current RMS over load current (I_{IN_RMS}/I_{Load}) as a function of the duty cycle.

For this example, the maximum input ripple current RMS occurs at full load and with duty cycle of 12.1%, according to Figure 4. Now calculate $I_{IN_RMS_max}$ using Equation 3. $I_{IN_RMS_max} = 1.97 \text{ A}_{RMS}$.

$$I_{IN_RMS_max} = I_O \times \sqrt{D \times (1 - D) + \frac{1}{12} \times \left(\frac{V_O}{L \times f_{sw} \times I_O} \right)^2 \times (1 - D)^2 \times D} \quad (3)$$

Figure 2. Input ripple current and ripple voltage waveforms

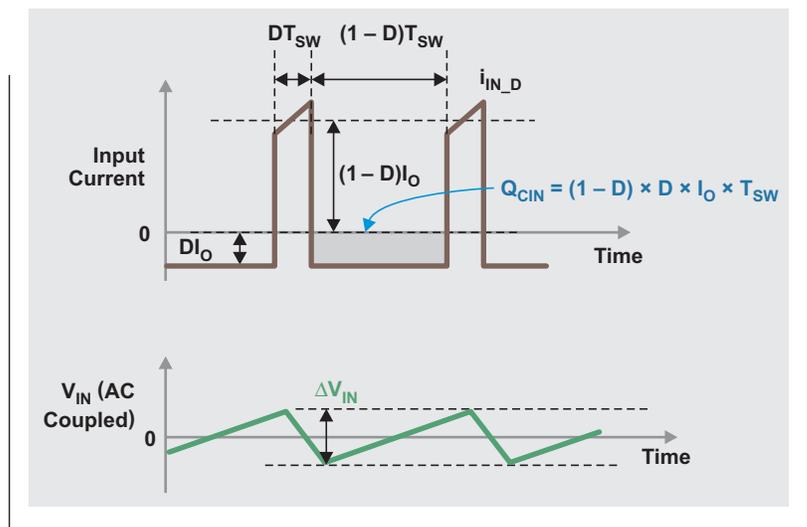


Figure 3. Capacitance using ceramic capacitors versus DC bias

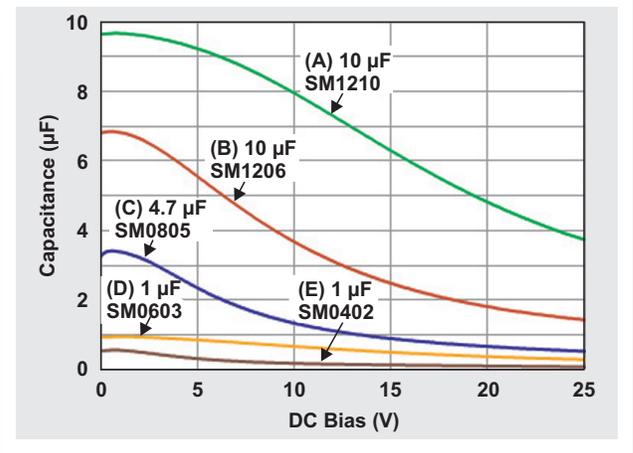
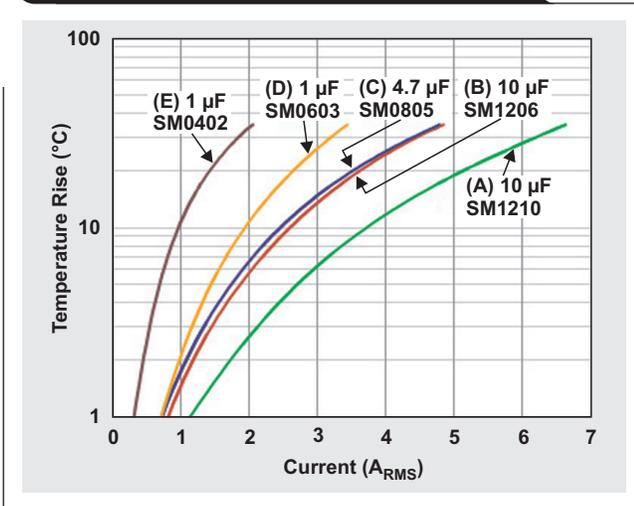


Figure 4. Input RMS/Load current ratio versus duty cycle



Figure 5. Temperature characteristics of different capacitors



Since the board temperature is 75°C and the X5R MLCC is rated for 85°C, capacitor temperature rise should be lower than 10°C. Figure 5 shows the temperature rise characteristics of different ceramic capacitors.

According to Figures 3 and 5, the ripple and thermal stress requirements can be met by combining two (B) capacitors or one (A) capacitor. Both selections have a similar cost and solution size. At this point, a third factor, the equivalent series inductance (ESL) should be included. Figure 6 shows the ESL of all five capacitors.

With two (B) capacitors in parallel, the combined ESL is about 0.3 nH, while one (A) capacitor has an ESL of 0.5 nH. Two (B) capacitors were selected for a total effective capacitance of 6 µF, and an allowable ripple current of 5.2 A_{RMS} with a 10°C temperature rise.

2. Add small ceramic capacitor(s) with low ESL to alleviate input spikes and phase-node ringing

With MOSFET technology advancement, transition time is dramatically reduced which improves efficiency. This leads to a high di/dt slope of the input current and high-voltage spike at the input and phase node. The ESL of the ceramic capacitors plays a significant role. Thus, it is desirable to further lower the input capacitor ESL. This can be achieved by adding a small capacitor with low ESL. Despite the fact that ESL varies with material and structure, a common rule of thumb is that a capacitor with a smaller case has a lower ESL (Figure 6).

Figure 6. Equivalent series inductance of multilayer ceramic chip capacitors

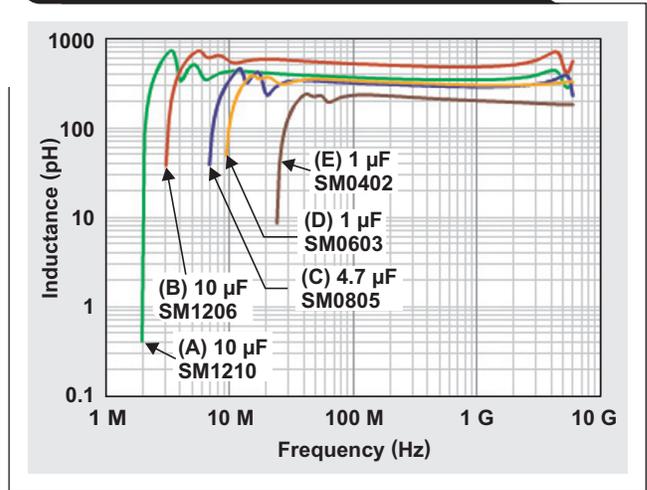
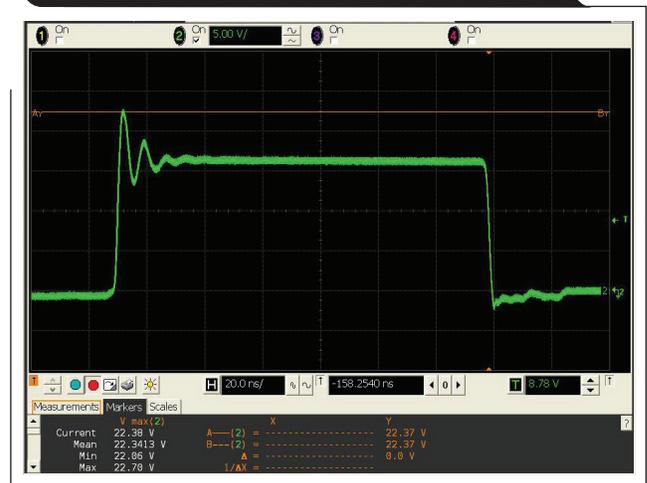


Figure 7. Switch-node waveform without additional small input ceramic capacitor



For phase-node ringing, it is common practice to use a boot resistor to slow down the gate speed and a snubber circuit for alleviation. However, both methods incur additional power loss and sacrifice efficiency. Phase-node ringing can be reduced without the penalty of lower efficiency.

Figure 7 shows the phase-node waveform of the TPS53318 with two (B) capacitors as the only input capacitors. V_{IN} is 16 V and the load is 6 A. The phase-node voltage spike is 22.7 V.

Under the same test conditions, one (D) capacitor was added to the input. As shown in Figure 8, the spike voltage was reduced from 22.7 V to 20.5 V. This is a significant improvement without sacrificing efficiency.

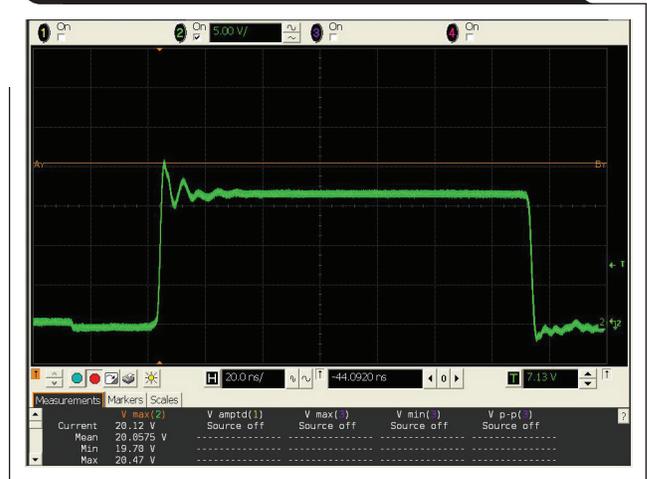
While an additional small ceramic capacitor can alleviate phase-node ringing, it can take up precious PCB space and in some cases increase cost. It is a trade-off of cost, size and performance. However, in this example, the added (D) capacitor did not increase the solution size.

3. Select bulk capacitors

While the MLCC is excellent regarding allowable ripple current, it is notorious regarding effective capacitance that is necessary to meet transient response requirements. Bulk capacitors with high capacitance are more cost-effective than using all ceramic capacitors. Aluminum electrolytic and polymer are popular capacitors for this purpose. There are two key factors for selecting bulk input capacitors: 1) overshoot and undershoot requirement of transient response; and 2) allowable ripple current requirement.

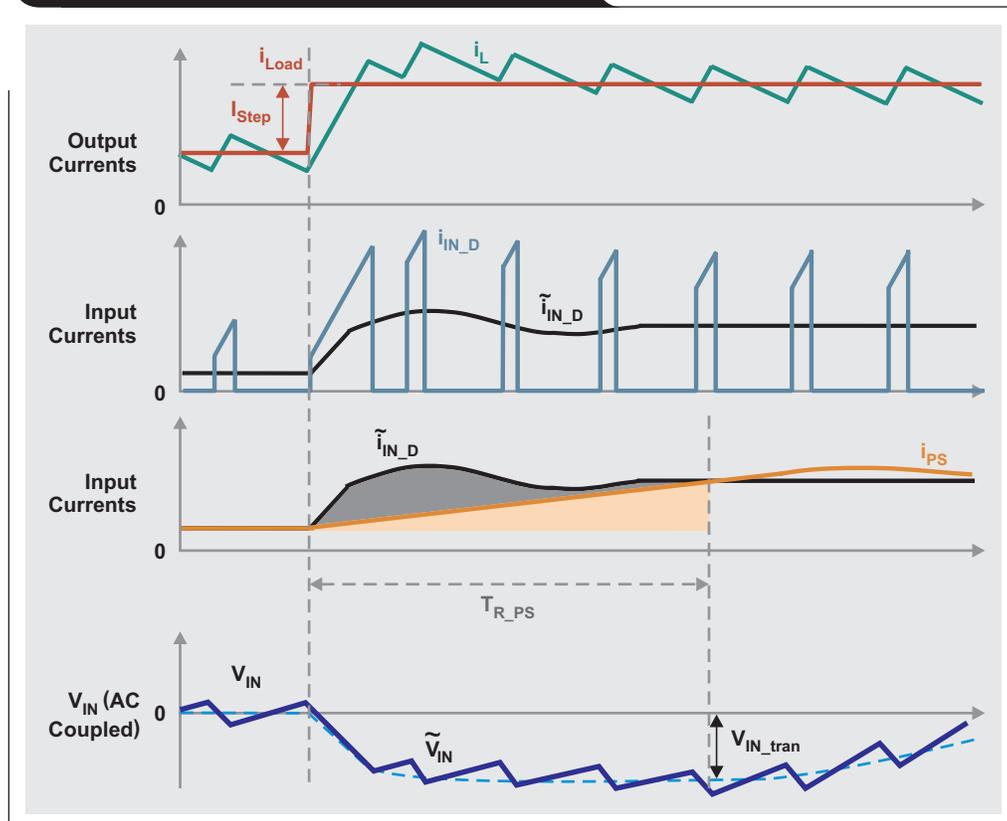
The ESR of the bulk capacitor (ESR_B) and the capacitance (C_B) need to meet the transient response requirement. Figure 9 shows the idealized load-transient current (i_{Load}), inductor current (i_L), input-transient current (i_{IN_D}) and bus-converter current (i_{PS}). The average input current (\tilde{i}_{IN_D}) can be approximated by the product of i_L and the duty cycle, D .

Figure 8. Switch-node waveform with additional small input ceramic capacitor



There could be two V_{IN} spikes during the transient: the first spike is related to the ESR_B ; and the second spike is caused by the difference between the buck-converter input current (\tilde{i}_{IN_D}) and the bus-converter output current (i_{PS}). Both spikes should be lower than the V_{IN} undershoot or overshoot requirement (V_{IN_tran}).

Figure 9. An idealized transient current plot



The ESR_B should be lower than that calculated with Equation 4.

$$ESR_B \leq \frac{V_{IN_Tran}}{I_{Step} \times D_{max}} \quad (4)$$

With $D_{max} = 12.1\%$, $I_{Step} = 3$ A, and $\Delta V_{IN_tran} = 0.36$ V, ESR_B should be less than 0.99Ω .

The second spike is related to the response of the bus converter. The converter output-current rise time during a transient event, T_{R_PS} , can be approximated by Equation 5.

$$T_{R_PS} \cong \frac{1}{f_{BW_PS} \times 4} \quad (5)$$

T_{R_PS} is about $41.67 \mu s$ with a control bandwidth of 6 kHz.

The capacitance of the bulk capacitor (C_B) should be greater than that calculated with Equation 6.

$$C_B \geq \frac{\frac{1}{2} \times I_{Step} \times D_{max} \times T_{R_PS}}{V_{IN_Tran}} - C_{CE_Total} \times (1 - Tol.) \quad (6)$$

Where C_{CE_Total} is the total capacitance of the ceramic capacitors, and the tolerance of the capacitors is 10%. Also, C_B should be greater than $15.07 \mu F$. Given a 20% tolerance, the rated capacitance of the bulk capacitor should be greater than $18.84 \mu F$.

Another factor for selecting a bulk capacitor is the allowable ripple current. It is a common practice that most low-cost electrolytic capacitors have an impedance that is much higher than the ceramic capacitors used for ripple-current bypassing. Thus, it can be assumed that the ripple voltage is not affected by the bulk capacitor. Figure 10 shows the idealized ripple current through the bulk capacitor.

The bulk capacitor ripple current (Δi_{CB}) can be approximated by the input ripple voltage divided by the ESR_B . Since the current-ripple waveform is triangular, the RMS of the ripple current (I_{CB_RMS}) can be estimated with Equation 7.

$$I_{CB_RMS} = \frac{1}{2 \times \sqrt{3}} \times \frac{\Delta V_{IN_PP}}{ESR_B} \quad (7)$$

The input ripple voltage can be calculated with Equation 8.

$$\Delta V_{IN_PP} \approx \frac{D \times (1 - D) \times I_O}{C_{CE_Total} \times f_{SW} \times (1 - Tol.)} \quad (8)$$

When selecting the bulk capacitor, I_{CB_RMS} should be less than the allowable ripple current, $I_{CB_RMS_Allowed}$.

$$I_{CB_RMS_Allowed} \geq I_{CB_RMS} \quad (9)$$

Thus, the allowable ripple current and bulk-capacitor ESR should meet the constraint specified with Equation 9 as shown by Equation 10.

$$I_{CB_RMS_Allowed} \times ESR_B \geq \frac{1}{2 \times \sqrt{3}} \times \Delta V_{IN_PP_max} \quad (10)$$

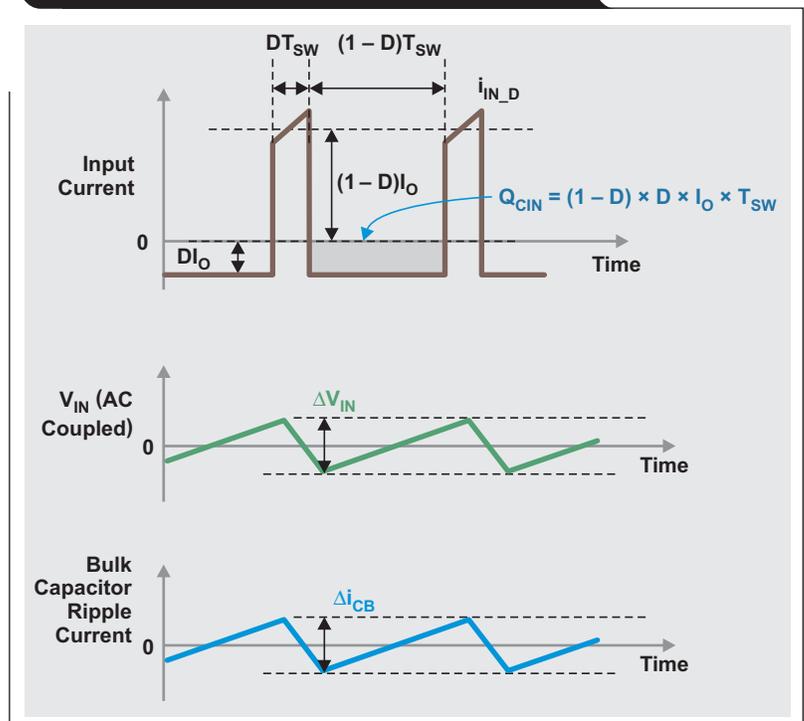
With $D_{max} = 12.1\%$, $C_{CE_Total} = 6.6 \mu F$ and tolerance = 10%, the maximum input ripple voltage ($\Delta V_{IN_PP_max}$) is about 179 mV. Thus, the product of the allowable ripple current and the ESR should be greater than 51.7 mV by Equation 9. Table 2 shows the parameters of five different electrolytic capacitors.

Table 2. Electrical performance of bulk capacitors

Designators	Rated Capacitance (μF)	Ripple Current (100 kHz) (105°C) (mA) (RMS)	Impedance (100 kHz) (+20°C) (Ω)	Tolerance (%)
F	10	90	1.35	± 20
G	22	160	0.7	± 20
H	33	160	0.7	± 20
I	33	240	0.36	± 20
J	47	240	0.36	± 20

To meet both the transient and ripple current requirements, capacitor G was selected from Table 2 for the input bulk capacitor. For applications where one electrolytic capacitor is not sufficient, multiple electrolytic capacitors can be put in parallel to meet transient requirements.

Figure 10. Idealized input ripple currents and input ripple voltage



However, the criterion for the product of the allowable ripple current and the ESR_B remains the same. If no electrolytic capacitor meets the ripple-current requirement, extra ceramic capacitors are necessary. The extra ceramic capacitance can be estimated by solving Equations 8 and 9.

The proper PCB layout is also critical for the performance of the switch-mode converter. Robert Taylor demonstrated the recommended input capacitors placement in his Power Tips post.^[1] Please refer to his blog post for input capacitor PCB layout recommendations.

Conclusion

The combination of ceramic and electrolytic capacitors renders a cost-effective solution for bypassing high-di/dt input ripple current and meeting load-transient response requirements. Following the tips and processes described could help you to select the proper input capacitors for a reliable, highly-efficient and compact DC/DC converter.

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Related Web sites

Product information:
TPS53318

Low- I_Q synchronous buck converter enables intelligent field-sensor applications

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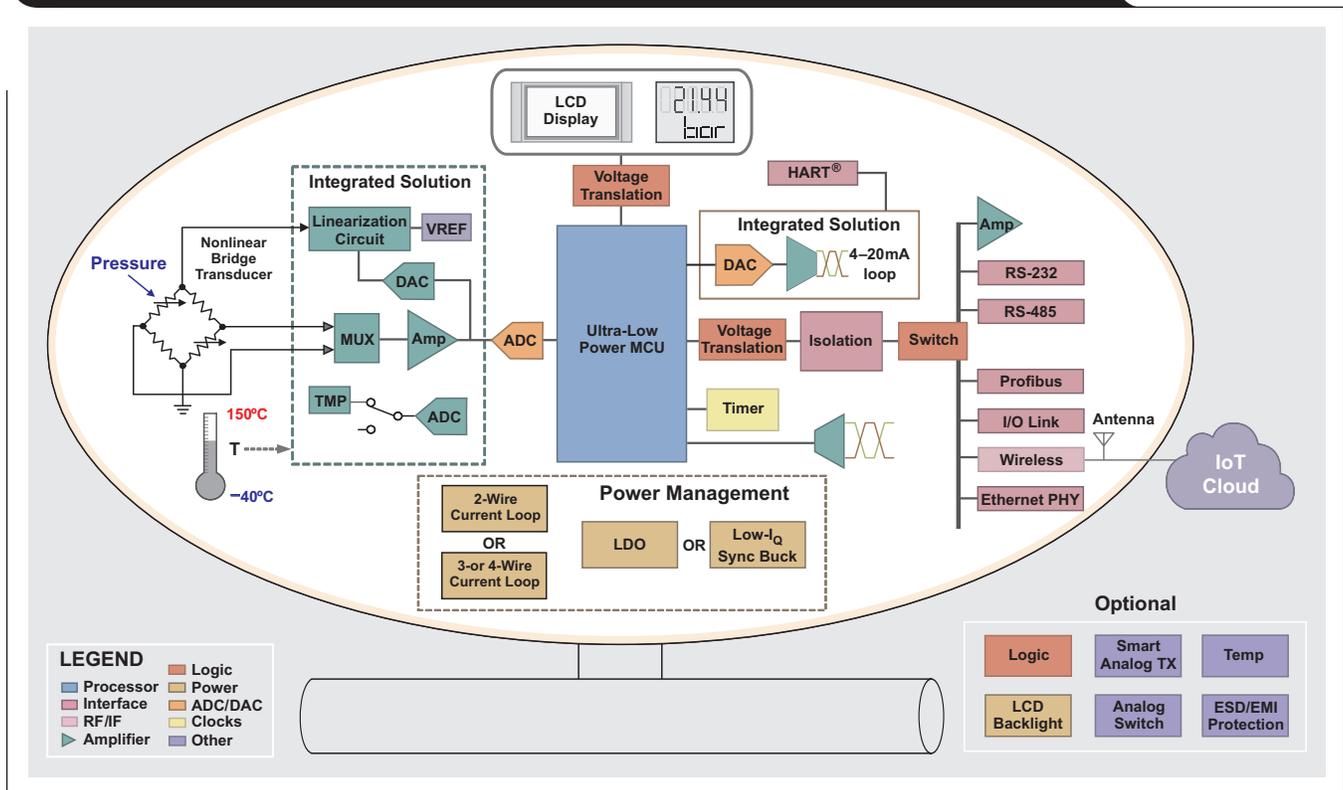
Introduction

There are several dimensions to the functionality of field-sensor transmitters used in industrial automation and control equipment to measure temperature, pressure, flow, level, and many other process variables. To provide some perspective, Figure 1 is a block diagram of a pressure-sensor transmitter. Included are a quarter-bridge strain-gauge transducer, microcontroller (MCU), data converters, input amplifiers, output drivers, isolators, display unit, connectivity options and power management. The primary challenge of sensing in industrial environments is the ability to condition low-amplitude signal

levels from sensors in the presence of high noise and large surge voltages.^[1]

The input signal from the pressure-sensor transducer needs to be converted to a precise electrical representation and transmitted from the field via a robust interface to a central control unit. An example of such an interface is the traditional two-wire, 4–20-mA current loop that remains a popular choice for long-distance communication in noisy industrial environments. The analog loop communicates the sensed primary variable (PV) in addition to supplying power to the transmitter circuit, as long as a minimum loop-current threshold is not exceeded.^[2]

Figure 1. Strain-gauge pressure transmitter in a factory monitoring application



Intelligent sensor systems with high current demand

While the MCU and data converters of a fundamental sensor-transmitter circuit are typically optimized for low operating current as shown in Figure 2, the feature set and increased functionality of high-performance sensor applications lead to increased current demand. Such intelligent sensor systems may not be able to meet typical under-scale current thresholds or zero-scale level of 4 mA as required by the 4–20-mA current loop. For example, a programmable digital-to-analog converter (DAC) and loop driver, such as the DAC161S997, has a default ERROR_LOW current threshold of 3.375 mA. Currents below this level are used as a diagnostic failure information range.^[3]

To increase the available power for a loop-powered sensor transmitter, a high-voltage switching DC/DC converter with high efficiency provides an inherent current-multiplication feature not possible with a classic low-dropout (LDO) linear regulator.

An increased current budget, in excess of a 3.375-mA low-alarm setting, offers developers of intelligent sensing applications the agility to deploy new capabilities. Following are several examples.

1. Input-isolated transmitters

Input-isolated sensor transmitters require a galvanically-isolated power rail from the loop supply to power the sensor. The sensor typically communicates across the isolation barrier via serial peripheral interface (SPI) through a digital isolator. Both the digital isolator and the isolated power stage need relatively high current and the system still requires an analog-to-digital converter (ADC), MCU and a DAC, all within the sub-4-mA current budget.

An increased current resource from a supply also lets multichannel digital isolators operate with higher-speed digital signals.

2. High-performance MCUs

Sensor output linearization is an essential task to meet accuracy specifications. In general, high-performance MCUs are required to perform complex calculations and deliver different levels of computational capabilities. This opens up a range of MCU options that involve processor speed, memory, connectivity, peripherals, and power optimization.

3. Calibration and advanced diagnostics

Device status information, calibration and diagnostic coverage also increases current demand. For instance, the HART[®] protocol operates by superimposing a 1-mA peak-to-peak signal on top of the DC current level of the 4–20-mA loop.^[4] Also, WirelessHART[®] adapters access and wirelessly communicate diagnostic information. These adapters also use power drawn from the wired-transmitter current loop.^[5]

4. Multivariable sensing

Many applications sense two or more (primary and non-primary) process variables.^[6] Often, the primary variable is dependent on one or more secondary variables. For example, mass flow transmitters for natural gas and steam applications sense differential pressure (raw flow) combined with process static pressure and temperature measurements for compensated mass flow readings. Monitoring non-primary variables may be advantageous if one or more of the variables is especially important to the safety or quality of the process.

Figure 2. Top-level hardware architecture of loop-powered temperature transmitter

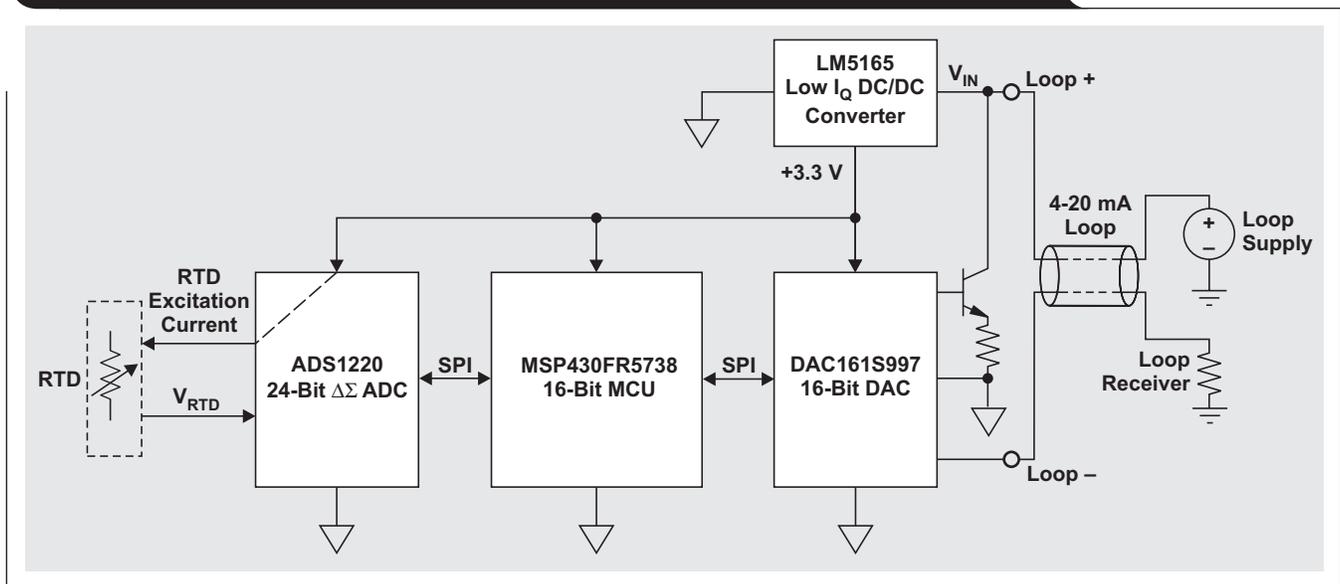
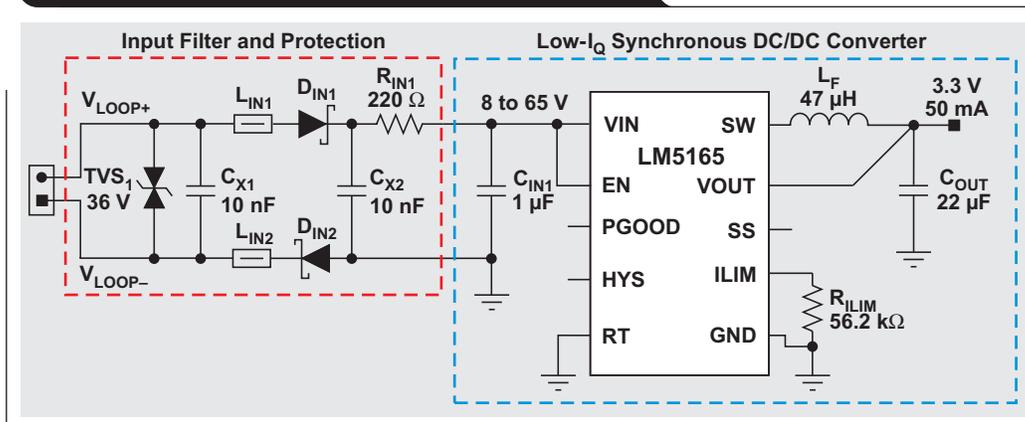


Figure 3. Low- I_Q synchronous buck converter includes input filter and protection circuit



5. Remote display and interface

Some two-wire transmitters have the ability to display information or take user input from an operator interface panel. The remote display unit and sensor transmitter may consume greater than 4 mA, depending on the complexity of the display.

6. Low-impedance bridges with high excitation currents

Common bridge impedances for strain and pressure sensors range from 120 Ω to 10 k Ω . The 120- Ω bridge consumes 40 mA of current with a 5-V supply. Some solutions use resistors in series with the bridge to increase bridge impedance and reduce current consumption at the expense of sensor output sensitivity. Having a larger current budget facilitates a higher sensor output that reduces the gain requirement of the analog front end (AFE).

Powering sensors with a high-efficiency buck converter

A synchronous buck converter must reliably power the sensor circuit, even during minimum input-power conditions when the transmitter is operating at its compliance voltage, typically 10 V or lower. This corresponds to the voltage between the Loop+ and Loop- terminals (Figure 2). Ultra-high efficiency within a 1- to 20-mA range of output current is thus imperative. Additionally, to deal with supply transient voltages such as those described in the IEC 61000-4 suite of tests, a DC/DC solution with a wide range for the input voltage (wide V_{IN}) offers an outsized voltage rating and operating margin.^[7, 8]

The LM5165 is an example of a synchronous buck converter that produces a tightly-regulated output, even in volatile voltage environments. This 150-mA monolithic step-down solution has high efficiency and ultra-low quiescent current, I_Q . Operating from a 20:1 wide- V_{IN} range and capable of sustaining repetitive 65-V surges, this buck converter's output voltage is immune to large and noisy voltage swings at the input. Such transient immunity is critical in sensor applications where high reliability and extended product life cycles are compulsory.

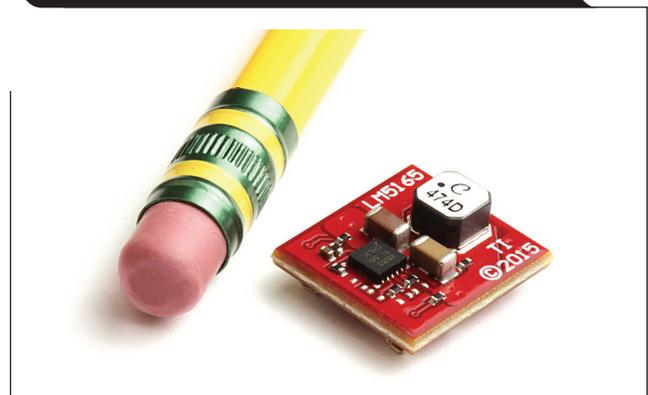
Figure 3 shows a converter schematic when configured with minimum component count. An input filter that includes reverse polarity and surge protection was added to achieve IEC 61000-4 compliance.

Provided in a compact 3- × 3-mm, WSON-10 package with integrated power MOSFETs, the LM5165 is extremely easy to use and it requires no components for loop compensation. The 3.3-V and 5-V fixed-output versions need only a filter inductor and two capacitors for operation and an adjustable set point is configured with just two 0402 feedback resistors.

Robust, reliable buck-converter implementation

Figure 4 shows a high-density converter implementation. Integrating the feedback resistors for the fixed-output versions allows the use of high values of resistance. This integration achieves a lower no-load supply current without compromising noise performance. The design minimizes system-generated noise because the high-impedance divider is integrated and proper layout practices were used to shield the sensitive nets from any system- or converter-level noise sources.^[9]

Figure 4. Implementation of a high-density synchronous buck converter



Various features incorporated for enhanced reliability and safety include an internally-fixed or externally-adjustable output soft-start (SS), and precision enable with customizable hysteresis for programmable line under-voltage lockout (UVLO). Other features included are thermal shutdown with automatic recovery and an open-drain PGOOD indicator for sequencing and fault reporting. The device's cycle-by-cycle, peak-current-limit threshold provides inherent fault protection from output overload and short circuits. Moreover, the device is easily configured to reduce its peak current limit such that smaller inductors and capacitors are viable for high-density, lower-current applications.

Input UVLO configuration

The precision enable input supports adjustable input UVLO with hysteresis, which can be programmed independently via the HYS pin for application-specific power-up and power-down requirements. An external logic signal can be used to drive the EN input to toggle the output on and off and for system sequencing or protection. Sensor applications in particular can benefit from using a resistor divider from V_{IN} to EN to establish precision input-voltage turn-on and turn-off levels. The HYS pin in tandem with the EN setting is used to increase the UVLO voltage hysteresis as needed to prevent unwanted UVLO triggering due to noisy loop voltage, high source impedance due to long loop wiring, or high-voltage coupling in harsh operating environments.

Achieving high efficiency with large step-down ratios

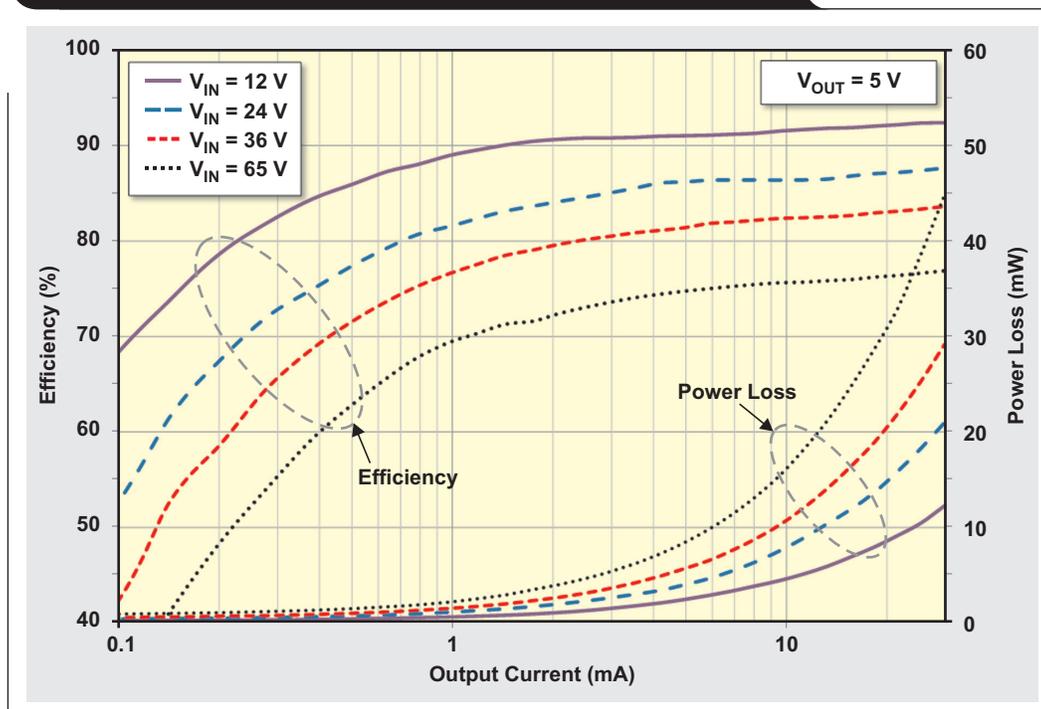
Unlike a high-voltage LDO, a synchronous buck converter does not incur a large power loss or increase in junction temperature as a result of the voltage difference between V_{IN} and V_{OUT} . Maintaining a low increase in junction temperature above ambient is paramount for reliable power solutions.

High efficiency is achieved at light loads by virtue of low I_Q in both sleep and active operating modes, in addition to the diode emulation and pulse-skipping to reduce switching activity and minimize switching power losses. High efficiency also continues at heavier loads through optimized switching of the integrated power MOSFETs. Figure 5 shows a relatively constant efficiency profile over the critical operating region when the load current is between 1 mA and 30 mA.

Conclusion

With the increasing demand for intelligently-connected sensing in applications such as industrial process control and analytics, home/building automation, healthcare/medical, smart metering and many others, wired and wireless connectivity enable a new level of scalability. Reliable buck converters with wide V_{IN} capability, high efficiency, small form factor and high immunity to line transients are finding increasing relevance to power these applications. Within the context of high density 4–20-mA loop-powered sensor nodes, the total bias current is limited to 3.6 mA or lower.

Figure 5. Typical efficiency performance of a buck converter



The total current budget must be sufficient to power all functional blocks of the transmitter: sensor interface and excitation, linearization method (MCU), galvanic barrier jump (if needed), 4–20-mA loop driver, and so forth. The solution presented was an integrated and robust DC/DC buck converter that has ultra-high efficiency across wide supply-voltage and load-current ranges. The resulting compact solution was achieved with minimal design effort.

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Related Web sites

Product information:

LM5165

LM5165-Q1

ADS1220

DAC161S997

The intricacies of signal integrity in high-speed communications

By Rick Zarr

Member Group Technical Staff, Signal Chain Applications

Introduction

As communication rates continue to increase, data is being moved within systems at ever higher speeds, which leads to issues with how engineers design equipment and printed circuit boards (PCBs). In the past 15 years, the industry has seen interconnection speeds increase from 1 Gbps to over 28 Gbps. Modern processors may have over 100 lanes of PCI Express® (PCIe), each running at 8 Gbps. The amount of raw throughput of systems today dwarfs the throughput of just 10 years ago. Back then, signaling rates were slow enough so that signal integrity was somewhat unaffected by passive interconnections. Today, that is no longer true. In most cases, transmission lines are now absolutely part of the circuit.

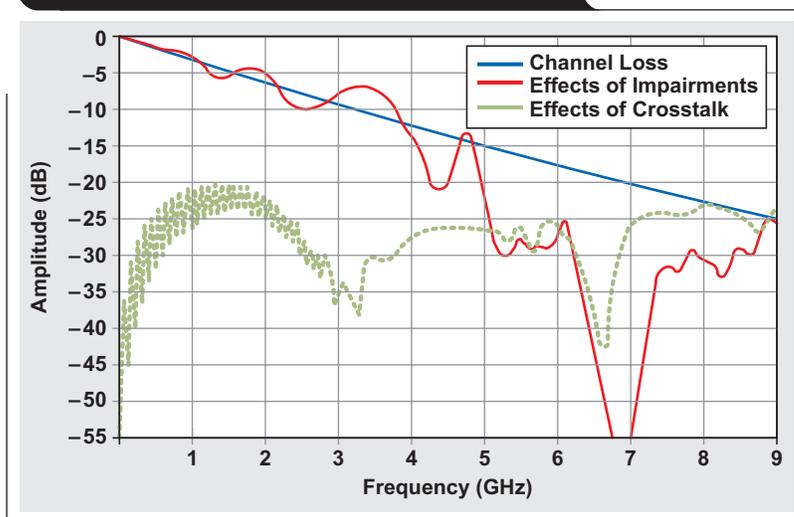
Many engineers have never had to consider what happens to the signals routed between integrated circuits. It was more of a challenge of cabling between systems, which may have required physical layer devices or special wiring. With field-programmable gate arrays (FPGAs) having increased capability and processors routinely using very high-speed interface standards such as PCIe, the system design must take into account the effects of PCB materials, transmission line design and connectors.

With the ever increasing speed of communications, the need to understand the effects caused by board layout, connectors and other parasitics is more important than ever. This article addresses the issues with high-speed signals and how to mitigate problems through proper component selection and board layout. Included in the discussion are standards such as SAS, SATA and Ethernet, as well as data converter interfaces such as JESD204B and other high-speed standards.

Signal integrity basics

All signals transmitted through a medium such as a PCB trace or coaxial cable are affected by various physical phenomena. As the signal's frequency content increases, these effects become more significant. For example, board capacitance, which is nominally very low (in the picofarad range), has little to no effect on low-frequency signals. But as the frequency increases, this capacitance begins to form a path to other signals or ground planes on the PCB. Other effects include impedance changes that cause reflections. These reflections affect the transmitted signal

Figure 1. Example signals showing various transmission-line effects



amplitude in ways that can appear random, but are actually deterministic.

At the highest level, loss of signal-to-noise ratio (SNR) directly affects the channel's capacity to carry information. Equation 1 shows this capacity relationship as presented by the Shannon-Hartley theorem. As SNR declines, channel capacity also declines. So anything that degrades the signal (assuming the channel noise remains constant) affects the channel's ability to carry information error free.

$$C = BW \times \text{LOG}_2 \left(1 + \frac{S}{N} \right) \quad (1)$$

where C is the channel capacity in bits per second, BW is the bandwidth of the channel in Hertz, S is the average signal power, and N is the average noise power.

Transmission loss is caused by a combination of things (Figure 1). These effects include linear loss (blue line), impedance discontinuities such as connectors or vias that cause peaks and valleys on the linear-loss line (red line), as well as coupling between signals known as crosstalk. All of these effects contribute to the channel insertion loss, also known as S₂₁ or S₁₂ scattering parameters. The most dominant loss is the bandwidth limitation of the PCB traces or cables.

Further, this bandwidth limitation is a function of the dielectric loss, which is directly proportional to frequency, and the skin effect, which is proportional to the square-root of the frequency. Skin loss is a phenomenon where

the higher-frequency current flows on the outside of the conductor. This causes the effective resistance to increase with frequency. Additionally, the dielectric loss of the insulating material varies with frequency, thus adding complexity to the actual absorption characteristics.

To solve the insertion-loss issue, designers have several choices. The first and most straight forward is to select a low-loss, high-performance dielectric material for their PCB. Examples of high-performance materials are NY9000 or MEGTRON 7, which have excellent loss characteristics. These materials are polytetrafluoroethylene-based (for example, Teflon®) with extremely low loss, but are fairly expensive and may have limited availability from fabricators. Lower-cost alternatives will require some understanding of the channel characteristics to make the best selection.

Alternatives to expensive dielectric materials are to use active equalization on the receiver side or the addition of pre-distortion (also known as emphasis) to the transmitted signal to compensate for the linear loss. In effect, both circuits boost the high-frequency components of the signal that are absorbed by the transmission line, which results in a somewhat flat response in the required bandwidth. These devices are often protocol/physical-layer dependent, such as the DS80PCI402, which is specifically engineered to equalize PCIe (gen 3) channels.

Another effect that can degrade a channel is jitter, or the uncertainty of when the crossing point of the signal's bit state will occur at the receiver. In an ideal transmission line, there would be no impedance discontinuities to create reflections. In reality, the slightest imperfection in the PCB or simply routing a transmission line across an isolation boundary will result in discontinuities and reflections. These imperfections add up as the signal propagates down the transmission line before it reaches either a terminated receiver or a connector. Connectors are notorious for issues with mismatching impedances simply due to the mechanical structure and how it interfaces to the transmission lines.

Jitter effects can be divided into two major categories: deterministic and random. Deterministic jitter is further divided into periodic jitter, data-dependent jitter, and bounded uncorrelated jitter. Periodic jitter is caused by things such as switching power supplies and clocks leaking into the signal. Data-dependent jitter is caused by sources such as inter-symbol interference (ISI) or duty-cycle

distortion (DCD), which affects when the receiver detects the state of the bit. Bounded uncorrelated jitter is a function of mostly layout where channels are placed close to one another. This is also called crosstalk and occurs when an aggressor signal leaks into a victim channel. All of these types of jitter can be corrected mostly through either equalization at the receiver, pre-distortion at the driver, or a combination of both.

Random jitter caused by various effects such as thermal noise will continue to increase within a given sample time, also referred to as “unbounded” jitter. Random jitter becomes an issue as transmission rates increase where the period of each bit, also known as the unit interval (UI), decreases, which allows less time for a bit to stabilize. Equalization cannot remove this type of jitter and, if severe enough, will require a re-timer device such as the DS100RT410 designed for 10-Gbps Ethernet to “re-clock” the data. The effect of re-clocking removes all jitter with a slight penalty in delay through the device. Re-clockers cannot be used on protocols such as serial AT attachment (SATA) or serial attached SCSI (SAS) where out-of-band (OoB) signaling is used to train the channel drivers and receivers (more on this later).

Protocol dependencies

With the introduction of serialized physical layers and protocols, standards have emerged that simplify system interoperability. Most serialized standards include the physical-layer electrical properties. It may be based on other standards such as current-mode logic (CML) or low-voltage differential signaling (LVDS) electrical specifications. This will dictate the drivers and receivers as well as the type of termination used. Other parts of the standards include a link or transport layer with specific protocols for training the channel or synchronizing the data fields. This can affect which types of signal-integrity components can be used to improve channel performance. Some standards include the physical connectors such as small form-factor pluggable (SFP) and quad SFP (QSFP), which also dictates the interconnect's form factor.

For most high-speed interconnections, using advanced board materials or active repeaters works to improve channel performance. Some protocols, however, actively train the channel due to variability of the transmission lines. An example is PCIe, which has connectors for

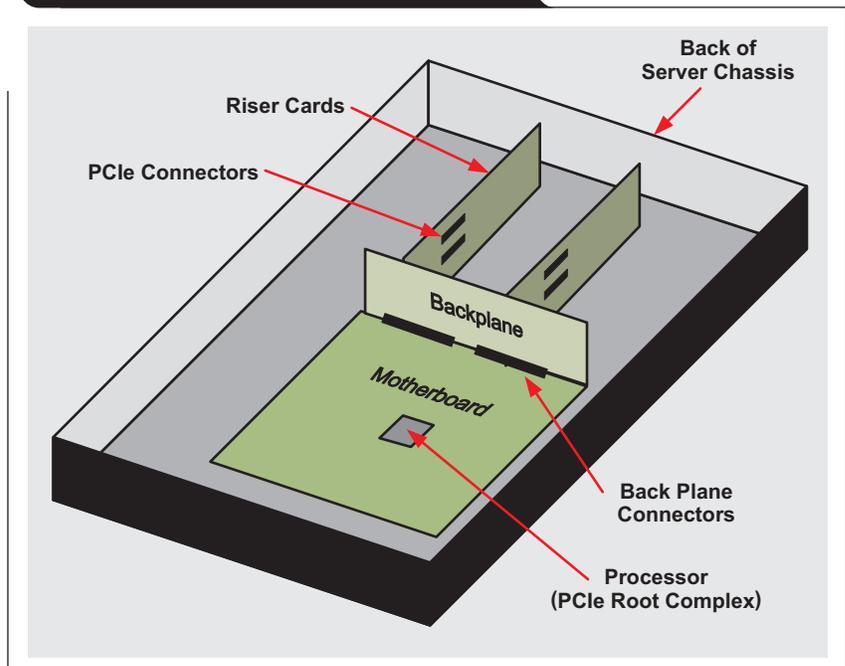
adapter cards with no knowledge of the channel characteristics until the adapter is running. For example, in a server, the communications adapter cards are normally placed at the back of the chassis along a riser card that plugs into a back-plane (Figure 2). The adapter card, known as the end node (EN), and processor side contains the root complex (RC). During initialization of each lane, the EN talks with the RC through a series of lower-frequency exchanges on the very channel that carries the high-speed data. This is referred to as out-of-band (OoB) signaling since the communication takes place at a lower rate than the normal transfer of data.

For passive channels this is not a problem, but active devices used to improve signal integrity cannot block these signals or the link will fail. For example, the DS80PCI402 allows OoB signals to pass, allowing the RC and EN to train normally. At both ends, the channel appears to have less loss.

The alternative is to completely recreate the EN and RC somewhere in the middle, effectively splitting the transmission lines into two independent PCIe channels. This method can add significant delay (30+ UIs) in each direction, resulting in a decline of performance during short bus transactions such as reading a single location in memory. Devices are available to implement this solution, however, they can also draw significant power since the device must completely recreate the root complex and end-node per PCIe lane (in both directions).

Some protocols are simpler and have no ability to train the channel dynamically. These are used in fixed point-to-point applications, such as running 10-Gbps Ethernet inside of a router to quad small-form-factor pluggable (QSFP) connectors. The length of the transmission lines are fixed and known. Issues may arise due to strict jitter specifications of optical modules that plug into these connectors. If the jitter specification cannot be met passively, then a buffer repeater can be used to adjust for the transmission loss before the connector. If this is still problematic due to excessive jitter, a re-timer can be inserted just prior to the connector at the edge of the chassis. The re-timer works in this scenario because no OoB signals are present. The great advantage of the re-timer is twofold: first it can recreate somewhat

Figure 2. Example server chassis with a back-plane and riser cards



jitter-free data at the output; and second, many re-timers include “eye” monitors that can sample the connection’s signal integrity. This could be useful on high-end routers that want to monitor the health of a channel without running bit-error rate (BER) tests, which require the connection to be taken off-line.

Protocols beyond data communications

Many interfaces such as SATA, SAS, Fiber Channel, Ethernet, PCIe and a host of others are used for storage or connectivity applications. These are all dedicated to moving bits throughout a computer or enterprise. There are, however, other interface standards such as Common Public Radio Interface (CPRI™) or JESD204B that are designed to move data between specific functions. For example, JESD204B was designed to simplify the inter-connection of high-speed analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). It has both a physical layer (CML) and several protocol layers (such as link and transport layers). Each lane is designed to be “one way” with a transmitter and receiver side. That is, there are sets of lanes for the ADC side (such as ADC to digital processing element) and another set of lanes

used to transmit to a DAC (such as digital processing element to DAC) along with a set of clocks and control lines (Figure 3). Line rates for the standard have a maximum of 12.5 Gbps, but future versions (for example, revision C) will be faster, on the order of 16 to 25 Gbps.

In direct-sampling RF applications, it can be advantageous to place the data converters near the edge of the PCB, while having the FPGA or processor located closer to other digital elements. The JESD204B standard inherently does not have specifications for driver de-emphasis or receiver equalization, but implementations may have these features. If the built-in signal-integrity features are insufficient because of longer trace lengths or discontinuities, then either improved board materials or an active solution can be applied to improve channel performance.

In the case of an active solution, there are two issues to consider. First, if an application requires phase coherency across multiple data-converter devices, deterministic latency is required (or system calibration) for you to know when all information from the coherent samples has arrived at the receiver. Adding any delay in the path also delays when the receiver can release the data to the processing element, if not symmetric. The second consideration is actually a benefit in that the JESD204B standard does not require OoB signaling, so component selection can include re-timers if channel jitter is excessive.

Conclusions

As data rates continue to increase, there is a growing need for engineers to understand the impact of signal integrity in their designs. With careful material selection and layout, many of these issues can be mitigated. When cost, material availability, or path loss becomes an issue, then active solutions such as repeaters or re-timers can be employed to restore the channel's signal integrity.

References

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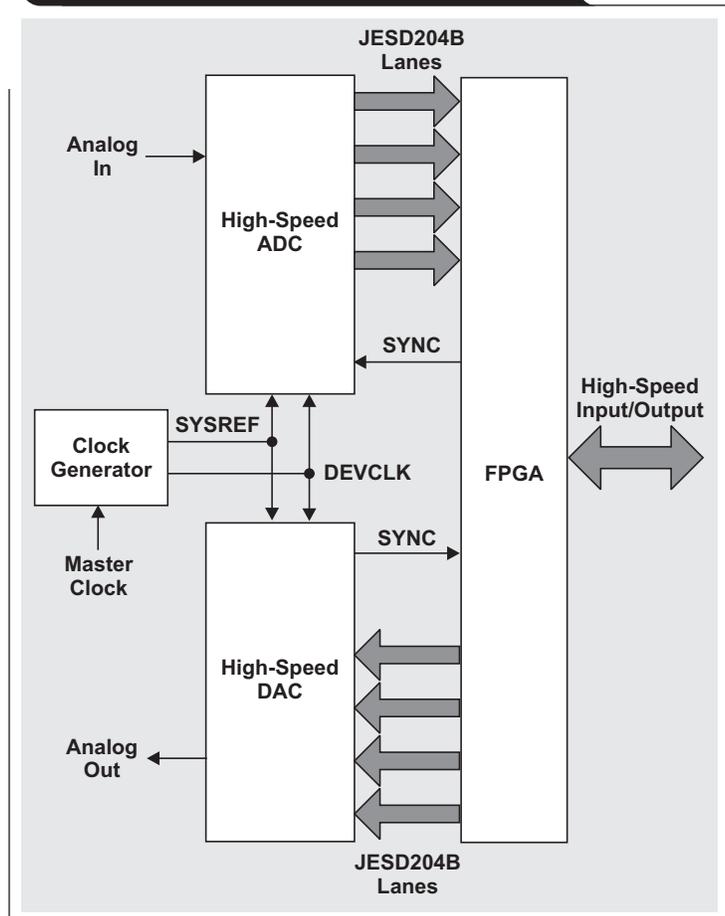
Related Web sites

Product information:

DS100RT410

DS80PCI402

Figure 3. Example JES204B system showing high-speed lanes and clocking



Increase power factor by digitally compensating for PFC EMI-capacitor reactive current

By Bosheng Sun

Application Engineer, High Power Controller Solutions

Introduction

Many articles have been written on how to improve power factor (PF). For the most part, they focus on power factor correction (PFC) current-loop tuning, or how to match the phase tracking of the PFC inductor current to the input voltage as closely as possible. This article explores a different angle. Poor PF mostly occurs at high line voltage and light load. Under these conditions, the PFC electromagnetic interference (EMI) filter has a big effect on PF. Because traditional current-loop tuning cannot do much to improve PF, a new method is required to deal with this low-PF issue.

PF is defined as the ratio of real power in watts (W) to apparent power, or the product of the root-mean-square (RMS) current and RMS voltage in volt-amperes (VA) as shown by Equation 1.

$$PF = \frac{\text{Real Power}}{\text{Apparent Power}} \quad (1)$$

Power factor indicates how efficiently energy is drawn from the AC source. Ideally, PF should be 1, then any electrical load appears as a resistor to the voltage source. However, in practice, electrical loads cause distortions in the current waveforms, resulting in poor PF. With a poor PF, the utility must generate more current than the electrical load actually needs, which causes elements such as breakers and transformers to overheat. In turn, this reduces their lifespan and increases the cost of maintaining public electrical infrastructure.

To attain a good PF, PFC is generally required at the front end of the power supply for electrical appliances with input power levels of 75 W or greater. A typical PFC circuit diagram is shown in Figure 1, which consists of three major parts: an EMI filter, a diode bridge rectifier, and a boost converter.

Figure 1. Typical power correction supply with PFC

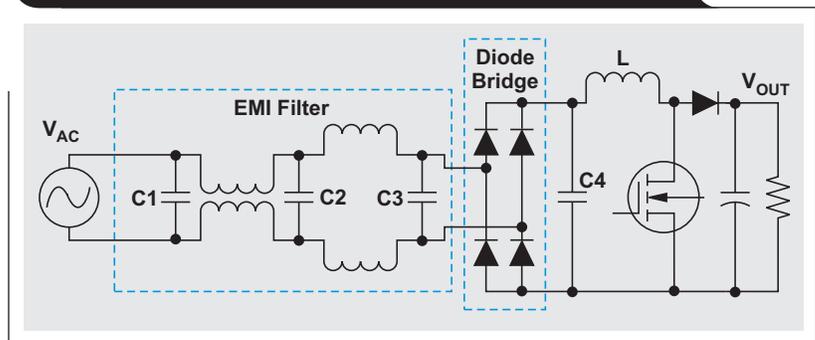
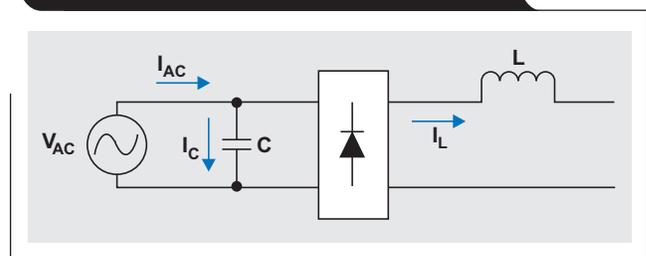


Figure 2. Simplified electromagnetic interference filter



A power supply with PFC has two purposes. The first is to rectify the AC voltage (V_{AC}) into a DC voltage (V_{OUT}) and maintain V_{OUT} at a specific level. The second is to control the input current to follow the input voltage so that a good PF can be achieved. With the ever increasing PF requirements, especially in the server and telecommunications industries, it is a design challenge for a PFC to achieve an excellent PF with traditional control methods.

Figure 1 shows a typical EMI filter for PFC. C1, C2, C3 and C4, which are EMI capacitors. Inductors in the EMI filter do not change the phase of the PFC inductor current; therefore, Figure 1 can be simplified as shown in Figure 2. Note that C is the combination of C1, C2, C3 and C4.

The EMI filter's capacitor causes the AC input current to lead the AC voltage (Figure 3). The PFC inductor current is \vec{i}_L , the input voltage is \vec{v}_{AC} , and the EMI-capacitor reactive current is \vec{i}_C . The total PFC input current is \vec{i}_{AC} , which is also the current from where the PF is measured. Although the PFC current control loop forces the inductor current, \vec{i}_L , to follow \vec{v}_{AC} , the reactive current of \vec{i}_C leads \vec{v}_{AC} by 90°, which causes the total current, \vec{i}_{AC} , to lead \vec{v}_{AC} . The result is a poor PF. This effect is amplified at light loads and high line voltages because \vec{i}_C has more weight in the total current. As a result, it is difficult for the PF to meet a rigorous specification.

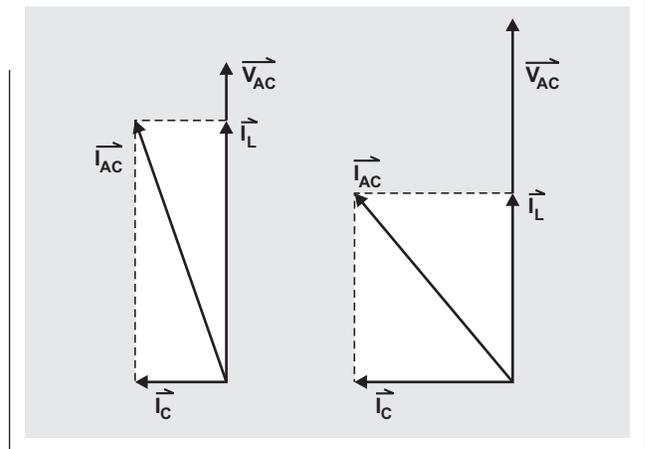
Traditionally, the poor PF caused by this EMI-capacitor leading current can be improved by forcing the induction current, \vec{i}_L , to lag \vec{v}_{AC} by some degree.^[1] To do this, the input AC voltage, \vec{v}_{AC} , is measured by an analog-to-digital converter (ADC), then delayed for an amount of time, Δt . The current reference is derived from this delayed \vec{v}_{AC} signal, which deliberately makes the inductor current, \vec{i}_L , lag \vec{v}_{AC} . This can compensate the leading EMI-capacitor reactive current, \vec{i}_C , and improve PF.

However, this method has several limitations. First, the delay period, Δt , needs to be dynamically adjusted based on the input voltage and output load. The lower the input voltage and the heavier the load, the smaller the Δt . Otherwise the inductor current, \vec{i}_L , will be over-delayed, making the PF worse than if there was no delay at all. Precisely and dynamically adjusting the delay time, Δt , based on the operating condition makes the design complex.

Second, the diode bridge blocks any reverse current, which is caused by a phase difference between voltage and current at AC zero-crossing. As a result, the current-feedback signal is clamped to zero, while the current reference is not zero. The inconsistency between the current feedback and its reference causes the control loop to accumulate to a large value. As a result, a current spike is generated when the diode begins to conduct again. The more PF is increased by the reference delay, the more distortion is generated, causing an increase in total harmonic distortion (THD).

There is a novel method to actively compensate for the reactive current caused by the EMI capacitor. Moreover, the PFC current-loop reference is reshaped at the AC zero-crossing to accommodate for the fact that any reverse current will be blocked by the diode bridge. Both PF and THD are improved as a result.

Figure 3. EMI-filter reactive current causes an AC current to lead the AC voltage



A novel EMI-capacitor compensation method

Poor PF is caused mainly by the EMI-capacitor reactive current, which can be calculated for a given EMI-capacitor value and input voltage. Therefore, if this reactive current is subtracted from the total ideal input current to form a new current reference for the PFC current loop, a desirable total input current can be obtained and a good PF achieved. To explain in detail, for a PFC with an ideal PF of one, \vec{i}_{AC} is in phase with \vec{v}_{AC} . The reactive current, \vec{i}_C , always leads \vec{v}_{AC} by 90°.

If \vec{v}_{AC} is depicted as:

$$v_{AC}(t) = V_{AC} \sin(\omega t) \tag{2}$$

then

$$i_{AC}(t) = I_{AC} \sin(\omega t) \tag{3}$$

Since capacitor current is

$$i_C(t) = C \times \frac{dv_{AC}(t)}{dt}, \text{ then}$$

$$i_C(t) = \omega \times C \times V_{AC} \cos(\omega t) \tag{4}$$

From Figure 2:

$$i_{AC}(t) = i_L(t) + i_C(t), \text{ so} \tag{5}$$

$$i_L(t) = i_{AC}(t) - i_C(t) \tag{6}$$

Combining equations 3, 4 and 6 gives:

$$i_L(t) = I_{AC} \sin(\omega t) - \omega \times C \times V_{AC} \cos(\omega t) \tag{7}$$

If $i_L(t)$ is calculated as the current reference for the PFC current loop, then the EMI-capacitor reactive current can be fully compensated, which improves PF (Figure 4). The blue waveform is the preferred input current, $i_{AC}(t)$, which is in-phase with $\overline{V_{AC}}$. The green waveform is the capacitor current, $i_C(t)$, which leads $\overline{V_{AC}}$ by 90° . The dotted black waveform is $i_{AC}(t) - i_C(t)$. The red waveform is the rectified $i_{AC}(t) - i_C(t)$. The proposed method for EMI-capacitor compensation uses this red waveform as its current reference. In theory, if the PFC current loop uses this as its reference, the EMI-capacitor reactive current can be fully compensated, and the PF can be increased.

The proposed current reference is further improved as shown in Figure 5. Because of the diode bridge rectifier used in the PFC power stage, any reverse current will be blocked by diodes. Referencing Figure 5, during the time period bound by T1 and T2, $v_{AC}(t)$ is in the positive half cycle, but the expected $i_L(t)$ (dotted black line) is negative. This is not possible, however, because the negative current will be blocked by the diodes, so the actual $i_L(t)$ remains zero during this period. Similarly, during the T3-to-T4 time period, $v_{AC}(t)$ becomes negative, but the expected $i_L(t)$ is still positive. So it also will be blocked by the diodes, and remains at zero. The red waveform in Figure 5 shows what the actual $i_L(t)$ would be, which will be used as the current reference for the PFC current loop.

Implementation

The proposed compensation method can be easily implemented by a digital PFC controller. In a traditional PFC with average current-mode control, the current reference is generated by:

$$I_{REF} = A \times B \times C \tag{8}$$

where A = voltage loop output, $B = 1/\sqrt{V_{AC_RMS}^2}$, and C = the sensed $V_{AC}(t)$ input voltage.

To use the proposed EMI-capacitor compensation method, the current reference needs to be modified according to Equation 7. The EMI-capacitor reactive current, $i_C(t)$, needs to be calculated first. With a digital controller, the input AC voltage is sampled by an ADC at a fixed sample rate. Thus, the frequency of an input AC voltage can be determined by calculating how many ADC samples are in two consecutive AC zero-crossings.

To get the cosine waveform, the ADC's input voltage measurements are stored in the random access memory (RAM). Note that the cosine wave leads the sine by 90° (a quarter AC cycle). Therefore, the cosine value of the input voltage can be found by reading from the previously stored ADC measurement, but shifted by a quarter AC cycle. Finally, the EMI-capacitor reactive current, $i_C(t)$, can be calculated using Equation 4, then subtracted from I_{REF} to get a new current reference. Special action is taken during subtraction to deal with AC zero-crossing distortion. The following steps outline the details:

1. Store the previous half-AC cycle, V_{AC} ADC measurements, depicted as $V_{AC}[0], V_{AC}[1] \dots V_{AC}[N]$, where N is the total ADC samples in a half AC cycle.

Figure 4. Proposed current reference curve for PFC current loop

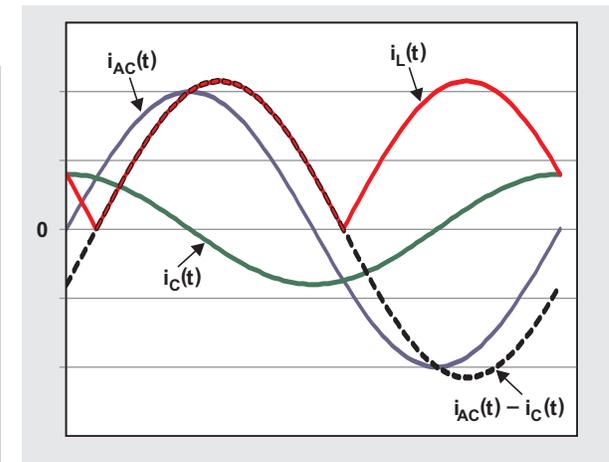
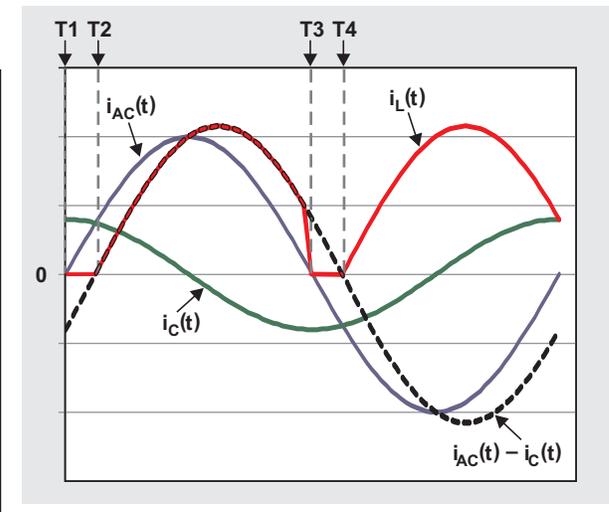


Figure 5. Proposed final current reference curve for PFC current loop



2. Detect the AC zero-crossing, which corresponds to the T1 time marker in Figure 5.
3. Read from the previously stored ADC values, starting from $V_{AC}[N/2]$.
4. Calculate $i_C(t)$ according to Equation 4.
5. Subtract $i_C(t)$ from I_{REF} to get the new reference I'_{REF} .
 - If $I_{REF} > |i_C(t)|$, then $I'_{REF} = I_{REF} - i_C(t)$
 - If $I_{REF} < |i_C(t)|$, then $I'_{REF} = 0$, which corresponds to the T1-to-T2 time period in Figure 5.
6. Once reading reaches the end of $V_{AC}[N]$, then start reading from $V_{AC}[0]$. This is because the AC waveform is symmetric in each half cycle.
7. Repeat the above for the next half-AC cycle.

Test results

The proposed compensation method for EMI-capacitor reactive current was tested on a modified 360-W, single-phase PFC evaluation module (EVM), UCD3138PFCEVM-026, which was controlled by a UCD3138 digital power controller. The input voltage for the test condition was $V_{IN} = 230\text{ V}$, 50 Hz. Figure 6 shows the actual PF test results at light load with and without EMI-capacitor compensation. Figure 7 shows the actual THD test results at light-load with and without EMI-capacitor compensation. Both PF and THD are improved with the proposed EMI-capacitor compensation method.

Conclusions

The proposed novel method to compensate EMI-capacitor reactive current reshaped the current reference during the AC zero-crossing area. Test results showed that both PF and THD were improved. Moreover, a digital controller was used to implementing this method, all changes were made in the controller's firmware, and no extra hardware was needed.

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Related Web sites

Product information:
UCD3138

Figure 6. Power factor versus load comparison

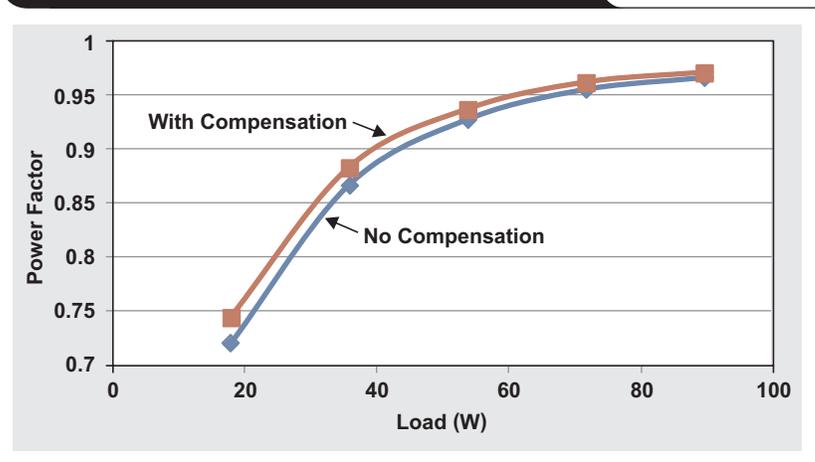
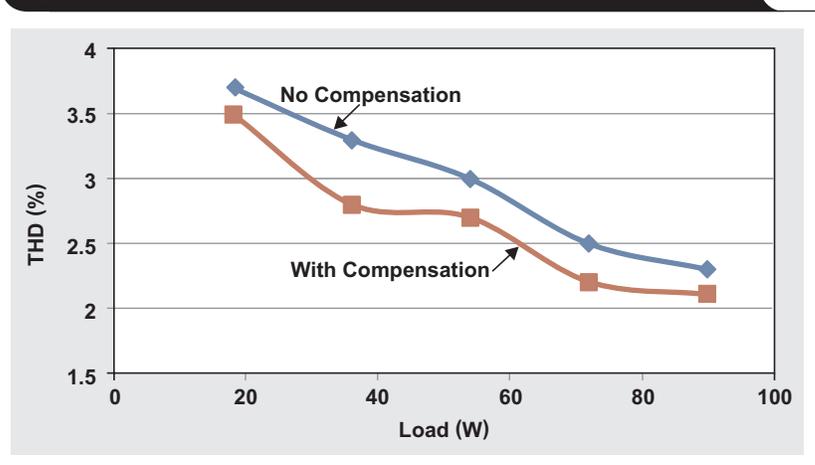


Figure 7. Total harmonic distortion versus load comparison



Battery-charging considerations for low-power applications

By Tahar Allag

Systems Engineer, Switching Charger Solutions, Battery Charging Products

Introduction

The wearable and personal-electronics industries are booming. Devices in this market vary wildly by application and use. These multifunction devices are designed to help people in their daily activities and make their lives comfortable. They can be found in different shapes, colors, sizes, and safety measures. They may differ significantly from each other, but they all have one thing in common—the need for a battery and a battery charger.

These portable devices are typically powered by batteries installed internal to the device, which must be charged efficiently and quickly on a regular basis. The user's charging experience also needs to meet the requirement of safety, comfort, and convenience.

This article presents the trade-offs between linear chargers and switch-mode chargers. Specific challenges arise with each topology when used to charge a battery pack in wearable applications. The differences between linear and switch-mode topologies are described with details about how each topology can address the requirements of wearable and personal electronic devices. These details range from thermal performance to cost, including size, application area, features and flexibility, electromagnetic interference (EMI), bill-of-material (BOM) counts, charge time, and so on. Finally, there is an evaluation for which charger topology serves which type of requirement best. Understanding charger-related system-level details enables the designer to save both time and cost.

Introduction to battery chargers

Battery chargers can be generally classified into two topologies: switch and linear-mode. Figures 1 and 2 show the basic architecture of each control topology. As expected, both topologies have pros and cons.

Switch-mode chargers use two power FETs (high-side and low-side) to control the current going into an inductor. Compared to linear chargers, they are more complex and require a larger application area with a higher BOM count. They also require an external inductor and additional capacitors. However, the efficiency of switch-mode chargers will be higher and thermal performance will be better than linear chargers. Switch-mode chargers are also better suited for applications that require higher charge currents. In addition, the switch-mode topology is more flexible and easier to adjust.

Figure 1. Block diagram of a switch-mode charger

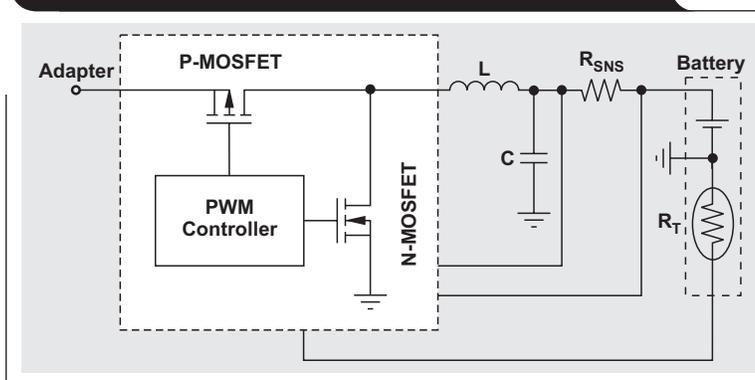
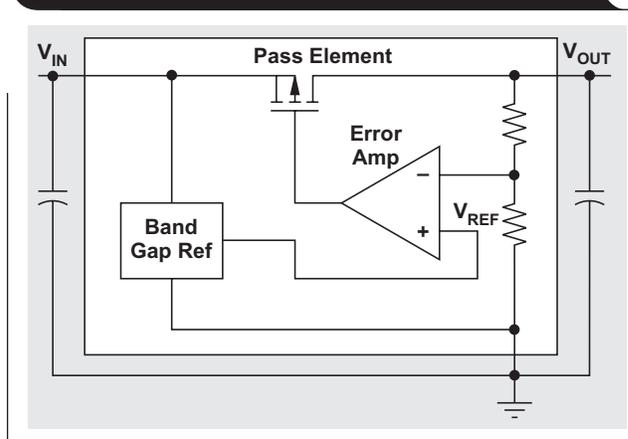


Figure 2. Diagram of a linear-mode charger



Alternatively, the linear charger uses a pass transistor to drop the adapter voltage down to the battery voltage. These are simple chargers that require a small application area and low BOM count, and are limited to a few capacitors and resistors. No inductor is required and no additional capacitors are needed. Efficiency and thermal performance are inferior when compared to switch-mode chargers in high-power applications. These chargers work well for low-power applications where size, BOM, and cost are important.

As shown by Figure 2, a linear charger has the battery pack and the system connected to the device's same V_{OUT} pin. This non-power-path architecture provides a simpler and lower-cost charger solution, but with some limitations like inadvertent charge termination and system operation with a deeply discharged battery.

Thermal performance

Many wearable devices are required to touch human skin. For example, a smart watch has direct contact with the wearer's skin while being worn. It would be uncomfortable if the device's temperature rises above a certain threshold. The thermal budget during use and after charge should be contained. Thus, during device charging, the battery charger's thermal performance is important and should be as low as possible.

A battery charger's thermal rise is due to power losses that manifest as thermal rise on the printed circuit board (PCB). The efficiency and power dissipation of a switch-mode charger is well contained, whereas a linear charger depends on the voltage drop across the linear regulator times the delivered current.

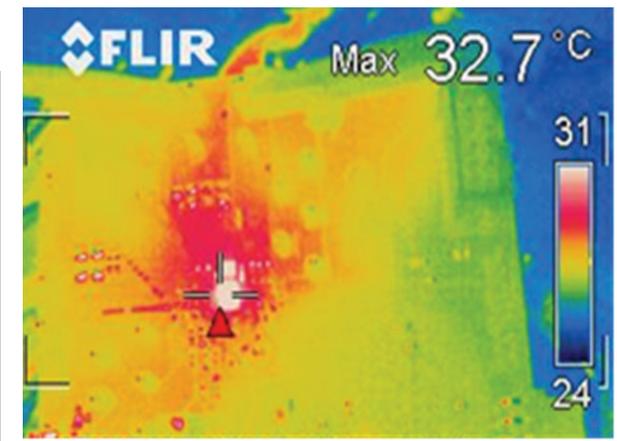
The power losses of a linear charger reduce significantly as the charger current drops below 300 mA. Figure 3 compares the thermal performance of a linear charger to that of a switch-mode charger with a 300-mA charge current, a battery voltage of 4.0 V, and 5-V input from the adapter. There is only 1°C difference between the two topologies.

The thermal difference between the two chargers in Figure 3 is negligible; however, as the power increases, a switch-mode charger becomes more suitable. Note that thermal performance of any charger depends on many other factors. For instance, the package type dictates the thermal dissipation of the die, layout of power traces, number of board layers, the amount of copper in a layer, dimension of the board, number and the size of the vias, shape of the board, and so on. For example, the quad-flat no-lead (QFN) package has better thermal performance than the wafer-chip-scale package (WCSP). More layers in the PCB help to dissipate power more easily. Figure 3b, for example, shows that the thermal dissipation is spread evenly over the board. This board layout allows the IC heat to dissipate more easily, thus lowering the device's peak temperature.

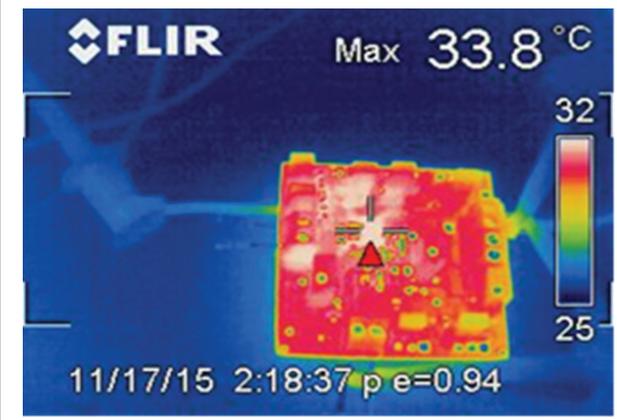
Application area and BOM cost

Application area of a charger is important as the total budgeted area for wearable devices is limited. Linear chargers are simple chargers that do not require additional inductor and complex circuitry around the device. Figure 4 compares the BOM count between switch-mode and linear chargers. It shows the minimum number of capacitors, ICs, resistors, and inductors required to design each of these charging topologies. In each of these comparison categories, the linear charger solution has overall fewer components. Nevertheless, switch-mode charger application areas have improved in the last few years and the BOM count has reduced significantly. The inductor is required for switching, but the size of the inductor can shrink with higher-performance devices, which reduces the footprint on the board.

Figure 3. Thermal performance of a switch-mode charger versus a linear-mode charger

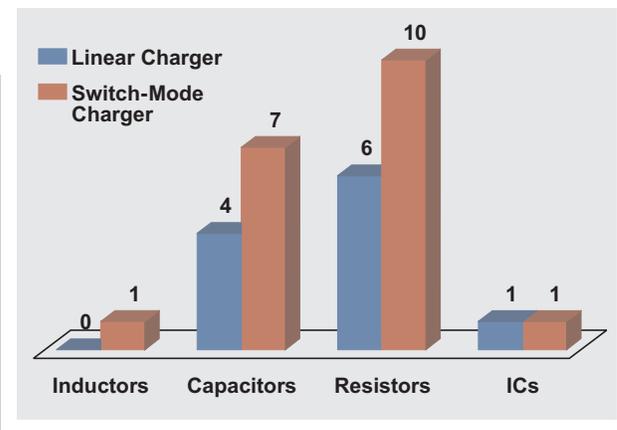


(a) Switch-mode charger



(b) Linear charger

Figure 4. BOM-count comparison for linear and switch-mode chargers



The lower BOM count in a linear charger can translate into application area savings. Any passive elements not used saves space needed for the charger. An inductor is not needed in a linear charger, which also saves space as shown in Figure 5. In low-power applications where space is critical, linear chargers can be a better fit.

Vendors such as Texas Instruments (TI) are pushing the envelope of innovation to meet market demand by reducing the BOM cost and board space without sacrificing device performance. For example, the bq24250 is a highly integrated switch-mode, single-cell Lithium-Ion (Li-Ion) battery charger and system power-path management IC targeted for space-limited, portable applications with high-capacity batteries.

Electromagnetic interference

The simplest component of EMI is an electromagnetic wave that consists of two elements: electric (E-field) and magnetic (H-field) waves running perpendicular to each other. One of the key sources of emissions is a rapid change in a current flow in a loop. A current flowing through a loop can generate a magnetic field, which is proportional to the area of the loop. Loop area is defined as the trace length in a PCB times the distance to the ground plane.

As current changes rapidly in a switch-mode charger, commonly from the internal MOSFETs, an electric field is generated from the voltage transition. Thus, radiation occurs as a result of this current loop. Another source of conducted EMI is ripple in the switching converter's output. The ripple generally appears at the harmonics of the switching frequency.

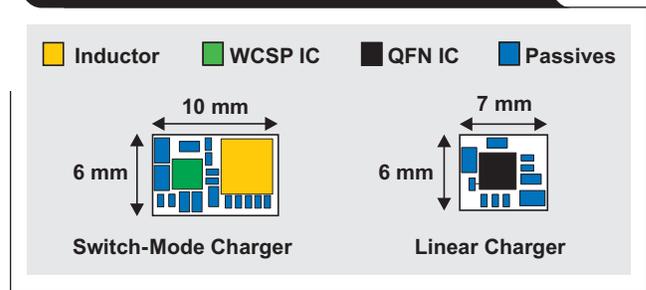
EMI can appear as electrical noise on the PCB traces. This high-frequency noise is not limited to just the charge area. Because capacitive and inductive crosstalk occurs between traces that run parallel for even a short distance, noise can propagate all over the PCB traces to cause further disturbances.

Many techniques can be used to reduce EMI in switch-mode chargers, such as the addition of shielding, relocating the PCB, changing the switching frequency, and so on. This can add to the cost and increase the application area. For low-noise applications, linear chargers are the safest and easiest solution to reduce EMI.

Design flexibility

Being able to repurpose the same chip for various products or multiple generations has a direct cost savings for expandable system designs. It also shortens the application learning curve and helps to avoid any unnecessary risk by using a known working solution.

Figure 5. Application areas of linear and switch-mode chargers



The market is pushing for a family of battery chargers that integrate several features to provide flexibility for different applications. The I²C interface can provide that flexibility because it allows each application to be tailored as needed. In I²C mode, designers can program various parameters such as charge current, input current limit, regulation voltage, and termination level. TI has many switch-mode chargers that support I²C bus control of charging parameters.

Switch-mode chargers are known as feature-rich devices. Earlier versions of linear chargers lacked flexibility, while the newer generation of linear chargers offers programmability using external components. The bq24072 and bq24232 linear chargers provide a great deal of design flexibility, including programmable fast charge, pre-charge current, current limit, safety timer, and termination current level. They also come with different regulation voltages and power levels. However, this flexibility adds some cost in the form of increased complexity, application area, and BOM count.

Charge time

The charge cycle of Li-Ion batteries is mainly composed of three phases: pre-charge (trickle), fast charge (constant current), and taper (constant voltage). The transition between one phase to another is not ideal for many chargers. Both voltage and current do not have a sharp transition. TI is the first manufacturer to develop charge-time optimization of the charge cycle for switch-mode chargers to improve this transition. This technique reduces charge time for a given charge rate compared to other solutions.

Also, switch-mode chargers can handle higher voltages from adapters and charge at higher rates without affecting thermal performance. Linear chargers are typically limited to applications with a low input voltage. With these two features, switch-mode chargers can deliver faster charge times compared to the linear topology.

Conclusion

Both linear and switch-mode chargers are attractive when using them to charge low-power applications. Linear chargers are simple and cost-effective to design and no inductor or switching circuitry is required, thus no EMI issues. On the other hand, switch-mode chargers are more efficient, and thermally perform better. They provide more features and improved flexibility. Their charge time is improved with a wider range of input voltages. In conclusion, it is up to the system designer to weigh the pros and cons of each topology with the requirements of the desired end product.

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Related Web sites

Product information:

bq24072

bq24232

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