Analog and Mixed-Signal Products

Analog Applications Journal

Fourth Quarter, 2002

Ⅰ TEXAS
INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Contents

To view past issues of the
Analog Applications Journal, visit the Web site
www.ti.com/sc/analogapps

Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Interfacing op amps and analog-to-digital converters

By Bruce Carter (Email: r-carter5@ti.com)
Advanced Linear Products, Op Amp Applications

Introduction

One of the most common questions asked of the TI High-Speed Amplifiers Applications team is what op amp to use with a given analog-to-digital converter (ADC). The ADC is often from a competitor. Answering this question is a challenging task—and there is no absolute answer, only a list of gray areas and trade-offs.

It would be handy to have a table with ADCs on one side and recommended op amps on the other. But this table will never exist; there are too many variables in system design that affect op amp selection. This article does not contain answers, but questions. The questions will help the designer organize his thoughts and define exactly what the op amp needs to do. He should be prepared to answer these questions before committing to a design.

The list of questions may look daunting at first, but it is divided into sections that break up the system into component parts: system, power supply, input signal, ADC, operational amplifier, and other considerations. The completion of each section is a piece of the puzzle, and by the end of the process the designer should have weeded out op amps that are unsuitable for the job.

System information

The overall characteristics of the system often yield valuable information. A clear understanding of the product and its function is imperative to design success.

- Exactly what is the end equipment and its application? Different systems have different requirements. For example, key concerns in a video system are completely different from those in a wireless communication system.

- In general terms, what is the function of this signal-acquisition chain in the system? Where does the input signal come from and what happens to it once it is digitized?

- How many signal-acquisition chains are used in the product? Channel density can influence system design in numerous ways, including space constraints, thermal requirements, and amplifier channel density per package.

- Will this signal chain be duplicated in other products? Is flexibility an advantage, or can the design be narrowly focused on the task at hand?

- Is the design forced to adhere to a particular standard?

- In what temperature conditions will the system operate (for example, –40°C to +85°C, 0°C to +70°C, or +45°C to +55°C)?

- Does the system have forced air flow from a fan to help with thermal dissipation?

- Is automatic gain control (AGC) functionality required? If so, is it digital or analog control? What is the gain range, etc.?

- Is a current solution unsatisfactory in some way? Why is the current solution unsatisfactory?

Figure 1. Focusing on power supply characteristics
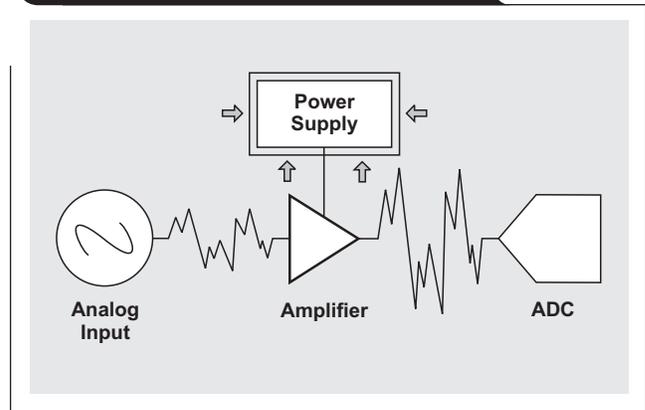
Power supply information

Power supply rails can quickly rule out amplifier solutions. This is similar to clothing shopping—the style may be desirable; but if the size doesn't fit, the style is useless. So a wise shopper finds the options in the size first, before becoming attached to a style. Similarly, an op amp with fantastic specifications at ±15 V may not operate at all from a +3.3-V power supply. Power supply information is collected first, because it will simply and unequivocally narrow choices. See Figure 1.

- What is the power budget for the overall system? Is power a concern, or is performance the ultimate goal?

- What power supply voltages are available in the design?

- Is there a preferred power supply voltage for the amplifier circuitry?

- Can an additional supply voltage be added if performance could be improved? Often, the best amplifier performance can be obtained with split supplies.

- Is a precision reference available in the system? In single-supply systems, it is important to supply a virtual ground to the op amp circuitry. If the system contains a reference, it would be advantageous to utilize it.

- Are there any special characteristics of the power supply? For example, is the power supply a switching power supply? Although op amps usually have excellent power supply rejection, it could be a concern in a high-resolution system. Any widely varying loads could also affect the op amp supply voltage.

Input signal characteristics

Understanding the input source is key to proper design of the interface circuitry between the source and the ADC (see Figure 2).

- What is used for the signal source to the amplifier block in front of the ADC? Is it another amplifier, a sensor, etc.?
- Describe the input signal. For example, is it continuous or discontinuous (i.e., pulsed)? The signal might be a QAM signal, an NTSC signal, a non-standard continuous wave signal, a random analog signal, etc.
- Are there any unusual characteristics of the signal source? Some sources have characteristics that will affect the performance of the amplifier circuit. For example, photodiodes have an associated capacitance, and the value of this capacitance plays an important role in how the associated amplifier circuit is designed.
- What is the output amplitude range of the source?
- Does the source produce a voltage or a current output?
- Is the signal source output single-ended or differential?
- What is the output impedance of the signal source?
- Is the input signal dc-referenced? If so, to what dc voltage is it referenced?
- What are the frequency characteristics of the input signal? For example, the signal might have a 10-MHz bandwidth centered around 25 MHz, or it might be a signal with frequency content from dc up to 20 MHz. If low frequency isn't important, this opens the possibility of ac coupling the input signal.
- What level of rejection is required out-of-band? Some applications have very strict requirements for out-of-band rejection, while others are less strict. The filter interface between the amplifier network and the ADC is dictated by this sort of information.
- Is there a known interfering frequency (system clock, sample clock, etc.) that must be filtered out? Are other large signals expected outside of the band of interest? A simple low-pass filter often may not have sufficient rejection of a particular interfering signal, forcing additional circuitry to produce a high Q notch filter.
- Is there a requirement for gain or phase flatness or error? This is a concern in video systems.
- Is there a matching requirement on the input impedance of the amplifier circuit? Some circuits require that the load be matched to a particular value for optimal performance (e.g., 50 Ω).

ADC characteristics

Once the power supply and input signal have been defined, it is time to focus on the device that the op amp will drive—the ADC (see Figure 3).

- Has the ADC been selected, or can it be changed to enhance performance?
- What is the desired sampling rate? Designers often assume that a data converter is going to be used at its maximum level of performance, but this typically isn't the case. For example, an 80-megasample-per-second (MSPS) converter might be given a sampling frequency of 60 MSPS.

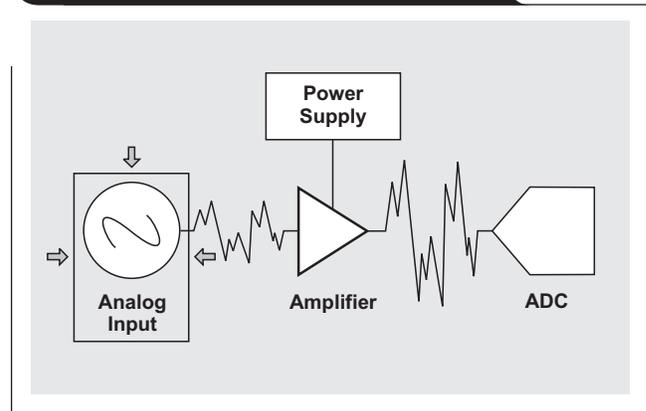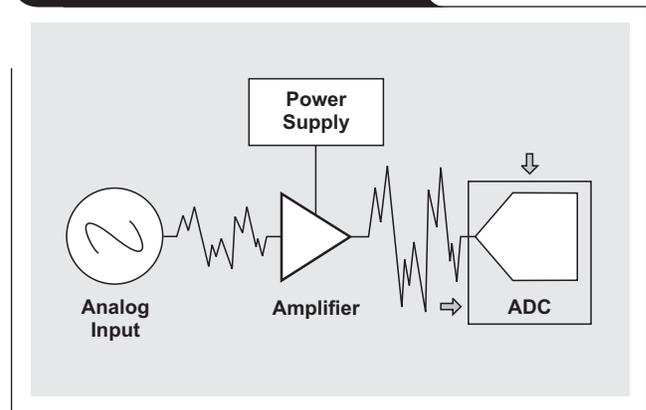**Figure 2. Focusing on the input signal**

Figure 3. Focusing on the ADC

- What is the desired resolution and effective number of bits? A 14-bit converter won't effectively yield 14 bits. The true resolution will probably be closer to 12 or 13.
- What is the full-scale input range of the data converter? Some data converters permit the input to be configured for different ranges.
- Will the data converter be used with single-ended or differential inputs? Typically, most high-performance data converters have differential inputs and require their use for optimal performance.
- Are there any other options on the data converter that could be an advantage? Data converters have lots of options that vary from part to part.
- Are there any compensation requirements for the input of the data converter? Normally, a small RC filter is required at the input of the data converter to compensate for its capacitive input. These components are usually specified in the converter data sheet and should be included as part of the interface. Otherwise, the op amp interface circuit may exhibit instability.

Operational amplifier characteristics

Although this article is intended to aid in the selection of the correct operational amplifier, it is possible that the nature of the system already defines some characteristics. See Figure 4.

- Has the operational amplifier already been selected, or can it be changed to improve system performance?
- Are there specific requirements for the package of the amplifiers? For example, must it be an 8-pin SOIC, or as small as possible, etc.?
- Does the cost of the operational amplifier interface or the physical size of the interface circuitry dictate that as few operational amplifiers as possible be used? Or would it be an advantage for the circuitry to be easily modified in the future, using more operational amplifiers for the flexibility?

Other pertinent considerations

This is the point at which the definition of the system should be complete. The wise designer, however, should take a step back. He should be asking, "Are there any other questions I should have asked? If questions were not asked, why not?"

The biggest consideration of all may be cost. This single concern has the potential of forcing a lot of good design work to be thrown on the trash heap. Yet a wise designer seldom goes wrong if he keeps the cost and number of components in mind when creating his design. Whether a million systems are produced, or only one, every manager will be pleased if the cost can be reduced without compromising system performance.

Conclusion

The design of a data acquisition system is a complex and time-consuming task. There are no universal solutions, nor are there any reliable lists of which op amp is matched to which ADC. There are a great number of factors affecting performance, and each design should be approached as if it were a custom design for which no precedent exists.

Figure 4. Focusing on the operational amplifiers
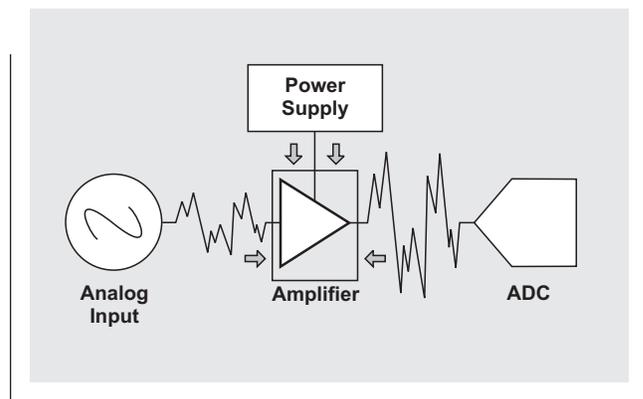
The designer must first answer the questions presented earlier to gain a good understanding of the true nature of his system and the scope of his design task. The next step is to visit **amplifier.ti.com** and look in the op amp selection guides for op amps that fit the application. As a general rule, the op amp should be much better than the data converter to which it is interfaced; otherwise, the designer is wasting money on the data converter.

In addition to the "Related Web sites" below, TI has a semiconductor technical support knowledge base to assist designers in finding products and services related to their technical questions. The direct link to this knowledge base is **support.ti.com/sc/knowledgebase**

For more general support information, visit **support.ti.com**

Related Web sites

analog.ti.com
amplifier.ti.com
dataconverter.ti.com

Using the UCC3580-1 controller for highly efficient 3.3-V/100-W isolated supply design

By Brian M. King (Email: b-king1@ti.com)

Advanced Analog Products

Power-supply modules offer an attractive solution for providing the bulk power conversion in telecom systems. Modules offer a ready-made solution in a single package but can be quite expensive. The alternative, of course, is to build a power supply from discrete components. A discrete design can dramatically reduce production costs but requires a more intense engineering effort. For those willing to invest the effort, Figures 1 and 2 present a discrete solution that provides up to 100 W at 3.3 V from an isolated 48-V input. This design matches or exceeds the performance, consumes less board area, and costs significantly less than many half-brick modules that have the same power requirements.

This design uses a UCC3580-1 to control an active-clamp forward converter with self-driven synchronous rectifiers. The topology allows the circuit to achieve efficiencies of up to 93%. Additional features included in the design are remote sense connections for point-of-load regulation, input undervoltage, input overvoltage, output overvoltage, and overcurrent protection.

Circuit description

Both an n-channel FET (Q1) and a p-channel FET (Q2) drive the 6-turn, primary winding of the active-clamp transformer. The UCC3580-1 controller provides the drive

for both MOSFETs. The n-channel drive is provided straight from the UCC3580-1, while the p-channel drive is inverted through the circuit of C7, D9, and R100. Figure 3 shows the drain-source waveforms of the primary and secondary MOSFETs.

While Q1 is on, power is delivered to the secondary, and magnetizing energy is being stored in the transformer. During this time, Q2 is off, and the clamp capacitor (C2) is out of the circuit and remains charged at a constant voltage level. When Q1 turns off, the leakage and magnetizing currents charge up the drain-to-source capacitance of Q1. Once the drain-to-source voltage of Q1 exceeds the voltage across the clamp capacitor, the body diode of Q2 begins to conduct. With the body diode of Q2 conducting, the magnetizing current now begins to charge the clamp capacitor.

Some time after the body diode of Q2 has begun to conduct, the controller turns on Q2. This provides zero-current switching for Q2. The clamp capacitor continues to charge until the magnetizing current is reduced to 0 A. At this point, the magnetizing current reverses, and the clamp capacitor begins to discharge until the controller turns off the p-channel FET. After Q2 turns off, the clamp capacitor remains at a fixed voltage. There is a fixed delay before Q1 turns on. During this delay, the energy in the parasitic components discharges the V_{DS} of Q1 towards

Figure 1. Power stage schematic

Figure 2. Control stage schematic

V$_{IN}$. This allows softer turn-on and reduces switching losses in Q1 (see Figure 4).

The secondary power stage consists of the synchronous rectifiers (Q5, Q6, Q8, and Q9) and the output filter (L1, C1, C11, C12, and C102). When Q1 is on, the voltage on the secondary of T1 ensures that both Q8 and Q9 are on, while Q5 and Q6 are off. During this time, a voltage equal to the input voltage divided by the turns ratio of the

transformer is applied across the gate-to-source of Q8 and Q9, and also across the drain-to-source of Q5 and Q6. Also during this time, the gate-to-source voltage of Q5 and Q6 is essentially 0 V and is equal to the inductor current times the $r_{ds(on)}$ of Q8 and Q9.

When Q2 is off, the voltage on the secondary of T1 reverses, and ensures that both Q5 and Q6 are on, while Q8 and Q9 are off. During this time, the magnitude of the

Figure 3. Power MOSFET drain waveforms

Q1: 50 V/div

Q2: 50 V/div

Q5 & Q6: 10 V/div

Q8 & Q9: 10 V/div

Time Scale: 1 µs/div
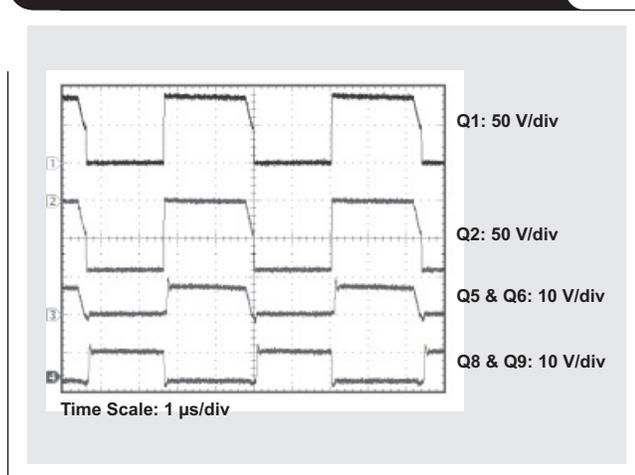
Figure 4. Turn-on of primary-side n-channel MOSFET

V$_{DS}$: 50 V/div

V$_{GS}$: 5 V/div

Time Scale: 100 ns/div
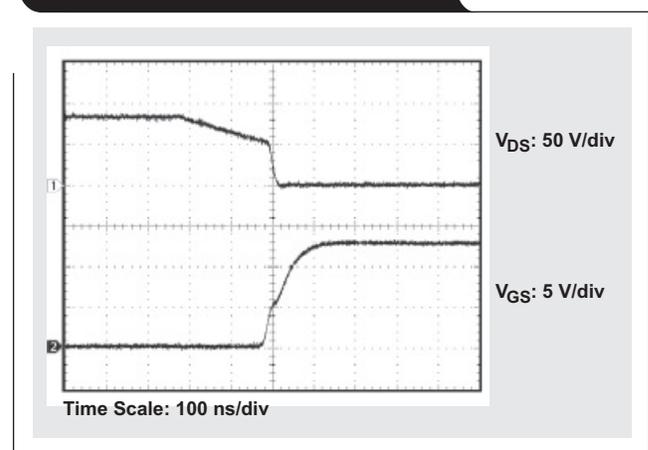
transformer secondary voltage is equal to the clamp capacitor voltage minus the input voltage, divided by the transformer turns ratio. The peak clamp capacitor voltage will determine the maximum voltage stress across the gate-to-source of Q5 and Q6, and also across the drain-to-source of Q8 and Q9. During this time, the gate-to-source voltage of Q8 and Q9 is essentially 0 V and is equal to the inductor current times the $r_{ds(on)}$ of Q5 and Q6.

Two bias voltages are used in this active-clamp design, one for the primary side and one for the secondary side. The circuit composed of C8, D2, D3, L1, Q3, and R12 produces the primary-side bias. D2, R12, and Q3 form a linear regulator, which is functional only during startup, or during a fault condition. L1 contains an auxiliary winding that is used to produce the primary-side bias during normal operation. The main winding of L1 has 4 turns, while the auxiliary winding has 16 turns. The auxiliary winding charges C8 to a voltage equal to the output voltage times the 16:4 turns ratio of the inductor, minus the diode drop of D3.

The circuit composed of C100, C101, D100, D101, Q100, and R101 produces the secondary-side bias. This bias is required to drive the feedback optocoupler (U7) and the TLV431 (U2). D100 and C100 peak detect the transformer secondary voltage. R101, D101, and Q100 form a linear regulator. The linear regulator is necessary to ensure that the bias voltage is independent of the input voltage. Without the linear regulator circuit, a second feedback loop is introduced into the compensation circuit, which complicates the compensation design.

Breaking the feedback path with R19 and R20 provides remote sensing. By connecting the remote sense terminals directly to the desired regulation point, the converter compensates for any voltage drops between the output of the supply and the load. The remote sense terminals must always be connected to the converter output and output return. If remote sensing is not required, R19 and R20 may be shorted, in which case regulation will be provided directly at the converter output filter.

Figure 5. Line and load regulation

Figure 6. Output ripple voltage
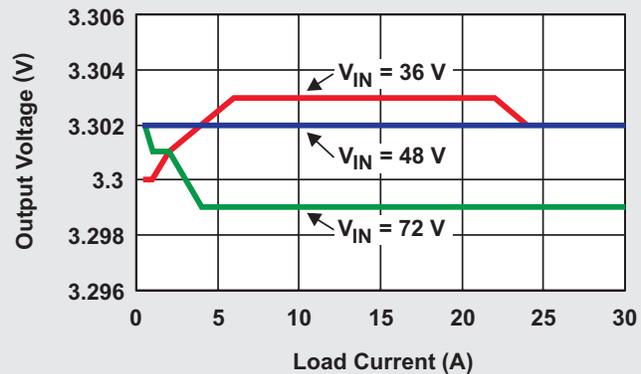
The feedback network is typical of most isolated forward converters. The TLV431 (U2) incorporates a voltage reference and transconductance error amplifier into one package. Providing type III compensation around U2 compensates the voltage-mode converter. The current transfer ratio of U7 and the values of R27 and R28 determine the gain of the optocoupler circuit. The error amplifier of the UCC3580-1 is used in an inverting configuration, with a gain of 1 V/V.

The shutdown pin of the UCC3580-1 provides overcurrent protection. The current is sensed at the source of Q1 by resistors R2 and R103. Resistor R16 lowers the shutdown threshold voltage, which improves the converter's efficiency by decreasing the required resistance of R2 and R103.

The UCC3580-1 and resistors R8 and R9 control the input undervoltage protection. The comparator circuit of U4 controls input overvoltage protection. Both input overvoltage and input undervoltage circuits provide hysteresis. The circuit of U5 and U6 provides output overvoltage protection. When the input to U6 exceeds the TLV431 reference voltage, the converter shuts downs until the overvoltage condition is gone, at which point a normal soft-start cycle is initiated.

Performance

The circuit operates from input voltages between 36 and 75 V and at load currents of up to 30 A. The output voltage typically varies by only 4 mV (0.1%) over the entire line and load range (see Figure 5). Most power modules with similar power requirements list line and load regulations below 0.2%. The output ripple voltage of this design is kept below 26 mV (0.8%) over line and load, as shown in Figure 6. Power modules offer similar ripple performance.

Figure 7 compares the efficiency of this design to the efficiency of modules from two leading module manufacturers. The data are given for a 48-V input and 25°C ambient temperature. Module A is typical of the majority of 3.3-V, half-brick, 100-W modules. Module B is an example of one of the few modules that list efficiency at greater than 90%. The discrete design competes very well with even the most efficient power-supply modules. The efficiency peaks at 93% at around 12 A and drops to 89% at full-rated load.

The efficiency, package, and thermal environment all conspire to limit the maximum load current for an application. While power modules may be rated for 30 A of load current, the current may actually be limited to a fraction of this by the internal device junction temperatures. The same is true of the discrete design. Modules have an advantage in this arena because they often are constructed with materials that provide good heat-sinking properties. With a discrete design, however, the designer has the opportunity to lay out the circuit board to accommodate for the power dissipation of hot components. Even with an excellent layout, at these power levels, both the modules and discrete solution typically require some forced air flow to achieve the maximum rated current.

To compare the thermal performance of the discrete design to that of the power modules, the circuit was constructed on a 2-oz. copper, 4-layer PCB in a half-brick footprint (2.3″ x 2.2″). The safe-operating-area (SOA) curves of the modules and the discrete design are shown in Figure 8 for a 48-V input and 300 linear feet per minute (lfm) of air flow. The good heat sinking and high efficiency of Module B allow it to operate at higher currents than both Module A and the discrete design. However, even the good heat sinking of Module A cannot make up for its low efficiency. Incorporating the discrete design into a larger PCB allows more copper to be tied to the hot components (the power MOSFETs) to provide a wider SOA.

Figure 7. Comparison of typical efficiencies
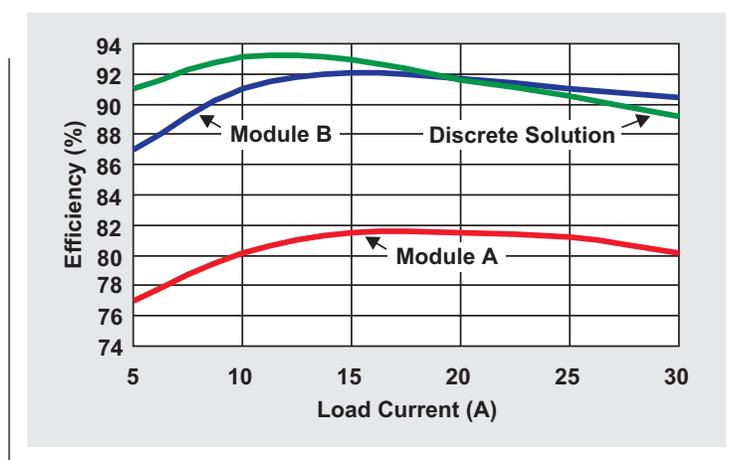
Conclusion

The decision whether to build a discrete power supply or to buy premanufactured modules involves trade-offs involving cost, schedule, and risk. Designing a power supply based on a reference design, such as the one presented here, significantly lowers the risk associated with the discrete approach. In situations where schedule is key, modules are the logical choice. However, migrating to a discrete power supply yields significant cost savings, particularly in high-volume applications.

Related Web sites

analog.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with TL331, TLV431A, UCC2580-1 or UCC3580-1

Figure 8. Comparison of SOA curves
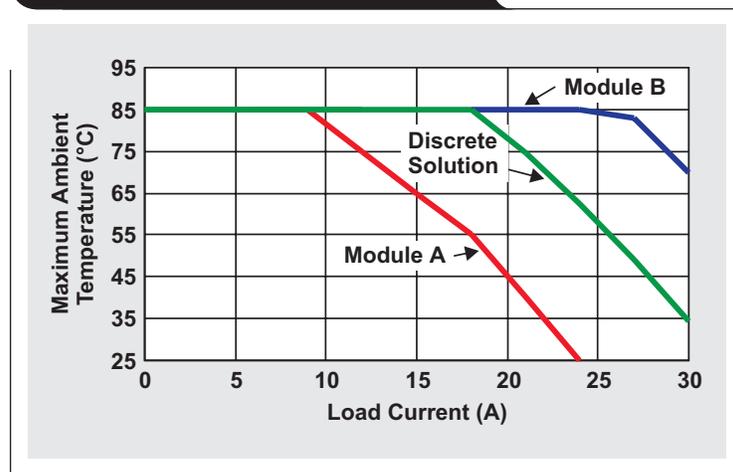
Power conservation options with dynamic voltage scaling in portable DSP designs

By Jeff Falin (Email: j-falin1@ti.com)
Low Power DC/DC Applications, High Performance Analog

Extending the useful life of the battery in portable electronics with a DSP core is a challenge for portable electronics manufacturers. The relationship $P_C \sim (V_C)^2 f$ describes the power consumption of a DSP core, where P_C is the core power consumption, V_C is the core voltage, and f is the core clock frequency.

Thus, power consumption can be reduced by lowering the internal clock frequency and/or even more by lowering the core supply voltage. Dynamic voltage scaling (DVS) is the term used to describe methods of adjusting core supply voltage to minimize power consumption. This article explains two generic methods of implementing DVS and highlights the advantages and disadvantages of each method.

Both methods require the use of a power IC with an adjustable output voltage and an externally applied control signal (V_X). As shown in Figures 1a and 1b, the first method uses FET switches and resistors in parallel with either the top or bottom feedback resistors to alter the feedback

Figure 1. Methods of implementing dynamic voltage scaling
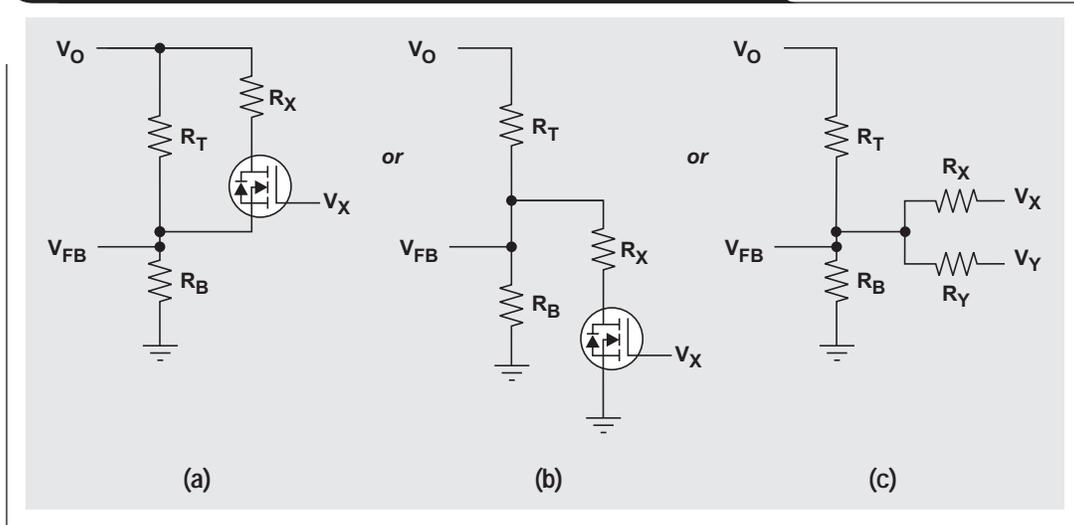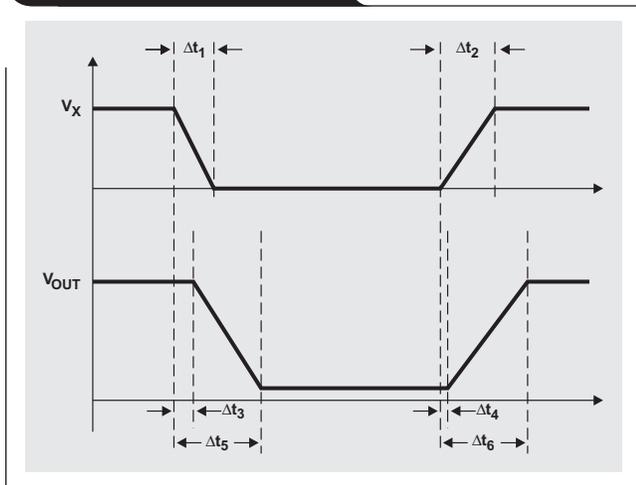
network. The second method, in Figure 1c, uses the control signal or signals and an additional resistor to alter the feedback network.

Figure 2 shows the timing of the control signals and of the output voltage. Table 1 explains the different delays and their respective causes.

Figure 2. Timing diagram

Table 1. Timing delays and their causes

	DESCRIPTION	INFLUENCING FACTORS
Δt_1	Fall time of V_X	Source of control signal
Δt_2	Rise time of V_X	
Δt_3	Response delay	Rise/fall time of V_X, IC response time, feedback network settling time
Δt_4	Response delay	
Δt_5	V_{OUT} fall time	Load current, output capacitance, IC response time
Δt_6	V_{OUT} rise time	

Each method in Figure 1 will be examined in detail. Although most adjustable power ICs can be used to implement DVS, the author chose the TPS62200 300-mA, synchronous buck converter because it maintains high efficiency over a wide load range by switching from PFM at light loads to PWM at heavy loads.

Switched bottom-side feedback resistor

The polarity of the control signal determines the placement of the FET switch. If a low signal triggers the step-down of the core voltage, then an NMOS FET switch and additional resistor can be placed in parallel with the bottom feedback resistor. An example application is shown in Figure 3.

Figure 4 shows an example of DVS using the circuit of Figure 3, where the input capacitance of Q2 is 110 pF. The input voltage is 3.3 V, and the output voltage switches between 1.5 V and 1.1 V with a 10-Ω load. The rise and fall times of V_X are 10 µs.

The overshoot during the transition from high to low voltage is due to the negative edge of the control signal being injected into the feedback pin, FB, by the gate-drain capacitance of the FET. Pulling FB low causes V_O to go high. Using lower-valued feedback resistors and higher-valued capacitive divider capacitors reduces the overshoot. Also, using a FET with lower input capacitance reduces the overshoot. Figure 5 shows an example of DVS using the circuit of Figure 3, where R_T = 200 kΩ, R_B = 165 kΩ, C_T = 100 pF, C_B = 220 pF, and Q_1 is a BSS123 with input capacitance of 30 pF.

If the control signal's ramp rate (Δt_1 and Δt_2 of Figure 1) can be slowed either at the source or by an RC filter, like the one created by R_F and C_F in Figure 3, the overshoot can be further minimized. Slowing the fall time of V_X to 150 µs removes the overshoot entirely, as shown in Figure 6.

Figure 3. Schematic with bottom resistor and high-cap FET
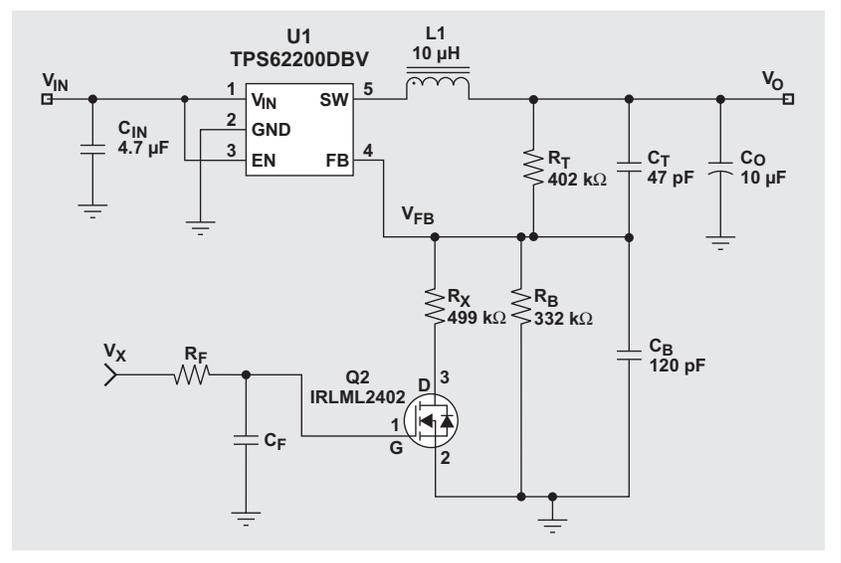
Figure 4. Bottom FET solution with overshoot
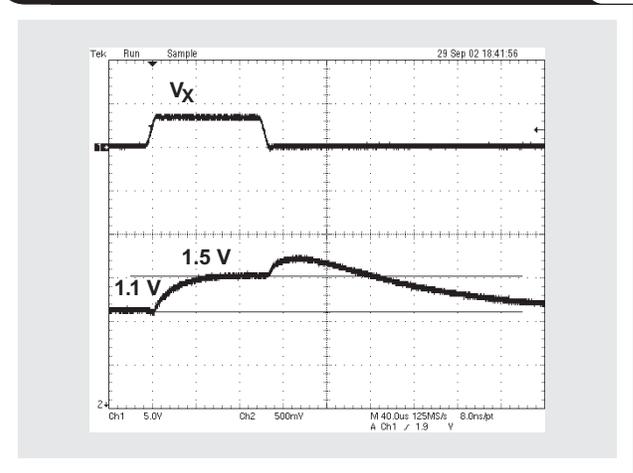
Figure 5. Bottom FET solution with reduced overshoot
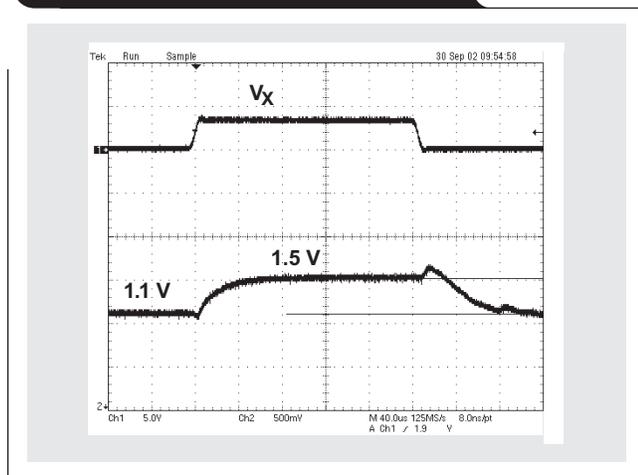
Figure 6. Bottom FET solution with no overshoot

13
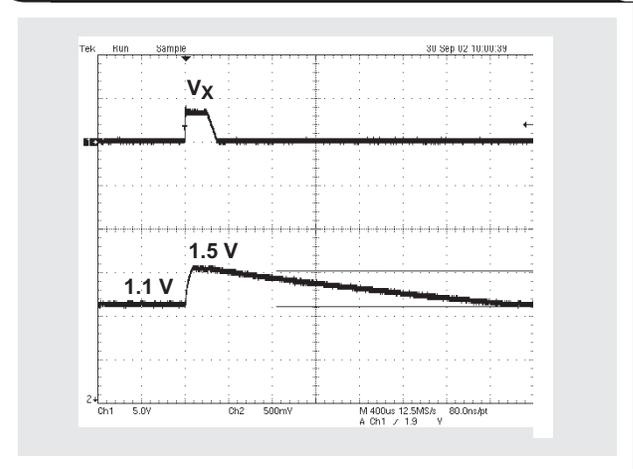
Figure 7. Schematic with top-side, low-cap FET and low-value feedback resistors
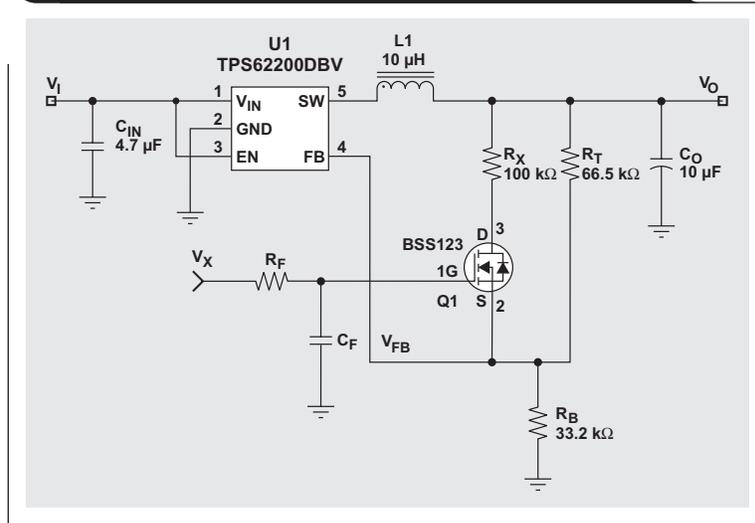
Switched top-side feedback resistor

If a high control signal triggers a step-down of the output voltage, then the NMOS FET must be placed in series with the high-side feedback resistor, as shown in Figure 7. The FET must be carefully selected to ensure that (1) V_X is higher than V_{FB} by at least the FET's threshold voltage and (2) the input capacitance is low to minimize injection of V_X onto V_{FB}. Unlike the low-side FET switch in Figure 2, the high-side FET's source pin connects directly to the converter's feedback pin. Since the FET's gate-source capacitance shorts V_X to V_{FB} during its transition, the output is susceptible to overshoot and undershoot; however, lower feedback resistors reduce both.

Figure 8 shows an example of DVS using the circuit of Figure 7, with V_{IN} = 3.3 V, a 10-Ω load, and control signal rise and fall times of 5 µs.

At output currents below 60 mA, the TPS62200 switches from PWM mode to PFM mode, and the observed under-shoot and overshoot change. If V_X's ramp rate (Δt_1 and Δt_2 of Figure 1) can be slowed either from the source or by an RC filter, like the one created by R_F and C_F in Figure 7, the overshoot is further minimized. Figure 9 shows results from using the same circuit as in Figure 7 but with a 1-kΩ load and control signal rise and fall times of 3 µs and 500 µs, respectively.

Although exact values for the feedback components and rise and fall times of the control signal are dependent on the specific application, the following generalizations can be made. Lower-valued feedback components reduce noise susceptibility at the feedback node and therefore reduce potential overshoot and undershoot caused by the switch-ing transistor. However, these lower-valued feedback components consume power and reduce efficiency at light load. The rise and fall times of the control signal affect overshoot and undershoot. The optimal rise and fall times should be determined experimentally for the specific application, especially for the load current and dc/dc converter operating mode.

Figure 8. Top-side FET solution with overshoot
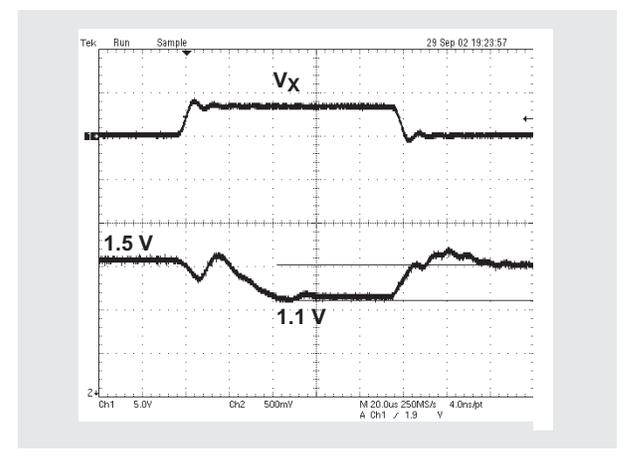
Figure 9. Top-side FET solution at low current and reduced overshoot
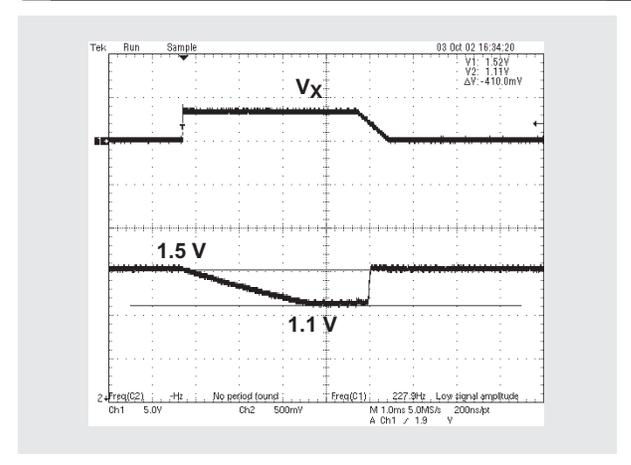
Two voltages with one additional resistor

A simpler alternative for generating multiple voltages is to use V_X to inject current into the feedback network through an additional resistor, thereby changing the output voltage. Figure 10 shows the circuit in Figure 11 transitioning between $V_{O1} = 1.5$ V and $V_{O2} = 1.1$ V, with only one additional resistor, R_X.

For the following discussion, refer to Equations 1–4 at the bottom of this page. Equations 1 and 2 were written by summing the currents at the feedback node, V_{FB}. Simultaneously solving Equations 1 and 2, then substituting back and solving for R_B, yields Equations 3 and 4. These equations show how to compute the values of the injection resistor, R_X, and bottom feedback resistor, R_B, in Figure 11, given $R_T = 402$ kΩ, $V_{O1} = 1.5$ V, $V_{O2} = 1.1$ V, $V_{X\_HI} = 3.3$ V, $V_{X\_LO} = 0$ V, and $V_{FB} = 0.5$ V.

Pulsing V_X with varying duty cycles varies its average dc level. This allows a single control voltage and one additional resistor, R_X, to generate multiple output voltages. Equations 1 and 2 can be solved to find R_X and R_B for the lowest desired output voltage and highest V_X. Then, solving Equation 4 for V_O and substituting in progressively lower values for V_{X_HI} results in progressively higher values of V_O. Figure 12 on the next page shows such an implementation.

Figure 10. Transition between two output voltages
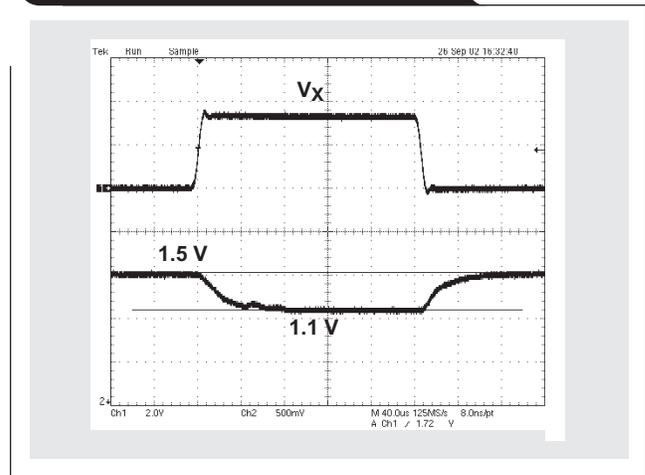
Choosing R_F in Figure 12 two orders of magnitude below R_X eliminates the need to include it in the computation of R_X. Choosing C_F to form a low-pass filter with –3-dB roll-off at least two orders of magnitude below the frequency of V_X makes the ripple being injected into V_{FB} negligible.

Figure 11. Schematic for switching between two voltages
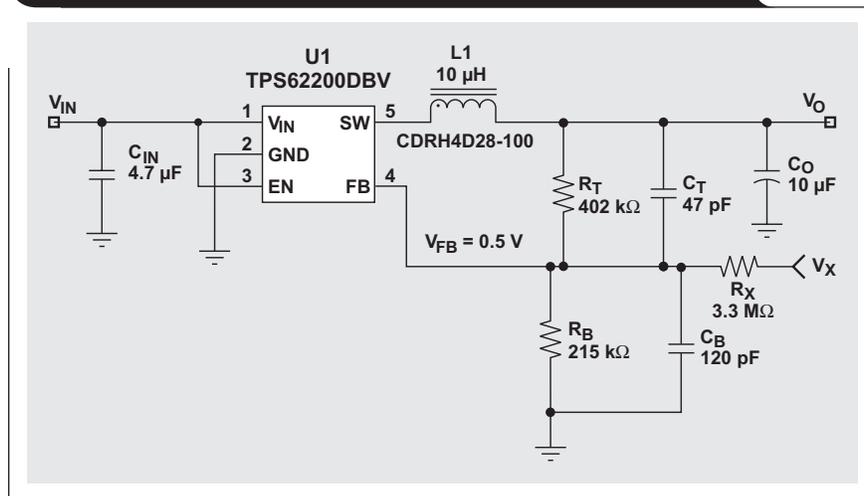
$$\frac{V_{FB}}{R_B} + \frac{V_{FB} - V_{O1}}{R_T} + \frac{V_{FB} - V_{X\_LO}}{R_X} = 0 \tag{1}$$

$$\frac{V_{FB}}{R_B} + \frac{V_{FB} - V_{O2}}{R_T} + \frac{V_{FB} - V_{X\_HI}}{R_X} = 0 \tag{2}$$

$$R_B = -V_{FB}R_T \times \frac{-V_{X\_HI} + V_{X\_LO}}{(-V_{O1} + V_{O2} + V_{X\_LO} - V_{X\_HI}) \times V_{FB} - V_{X\_LO}V_{O2} + V_{X\_HI}V_{O1}} \tag{3}$$

$$R_X = R_B \times R_T \times \frac{-V_{FB} + V_{X\_HI}}{V_{FB}R_B + V_{FB}R_T - V_{O2}R_B} \tag{4}$$

Three voltages from two additional resistors

If varying the duty cycle of V_X is not an option but additional control voltages (e.g., V_Y) are available, the converter can still be configured to switch between multiple voltages. In addition to the two feedback resistors, R_T and R_B, this solution requires one less resistor than the number of required output voltages. For example, if the application requires switching between three different voltages, the solution requires two injection resistors, R_X and R_Y, as shown in Figure 13.

As Table 2 shows, there are four logic states that can be derived from the two logic signals, V_X and V_Y; however, only three logic states are used.

Table 2. Control signal vs. output voltage

	V_X	V_Y	DESIRED V_O (V)	ACTUAL V_O (V)
V_{O1}	LO	LO	1.80	1.80
V_{O2}	LO	HI	1.50	1.50
V_{O3}	HI	LO	Don't care	1.40
V_{O4}	HI	HI	1.10	1.10

Figure 12. Filter for switching between multiple voltages
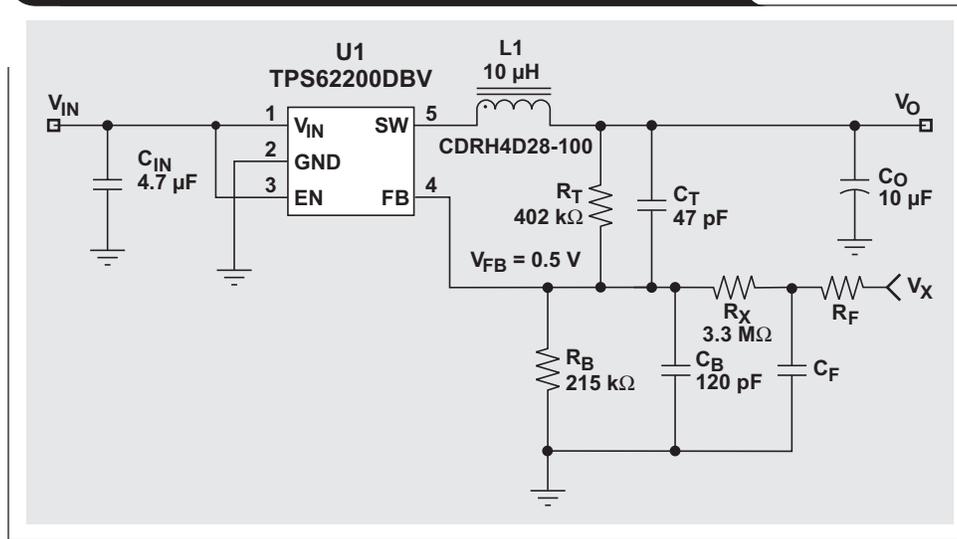
Figure 13. Switching between three voltages
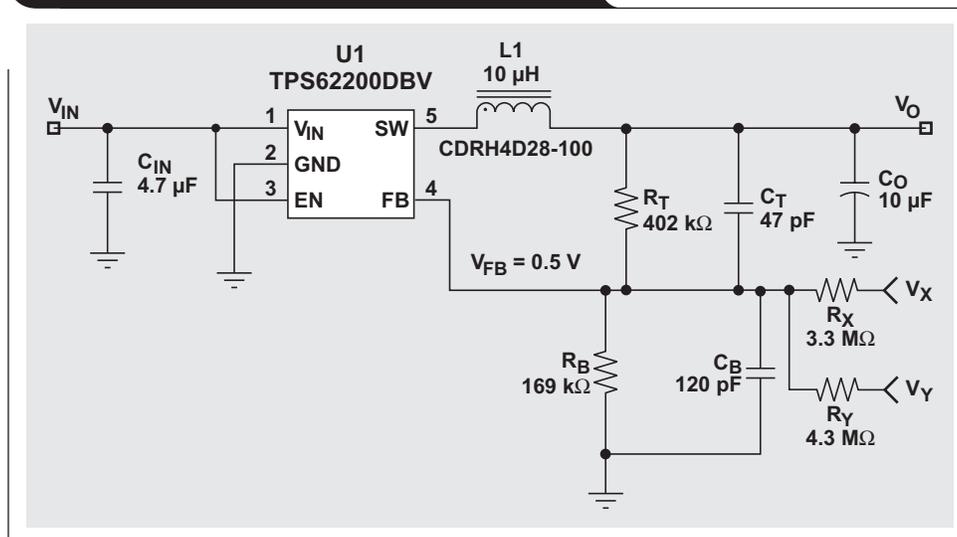
Similar to the computations for Figure 11, the circuit operation of Figure 13 can be evaluated with four nodal equations (one for each logic state), which can be solved for R_X, R_Y, and R_B in Equations 5, 6, and 7.

$$R_X = R_T \times \frac{V_{X\_LO} - V_{X\_HI}}{-V_{O2} + V_{O4}} \qquad (5)$$

$$R_Y = R_T \times \frac{-V_{Y\_LO} + V_{Y\_HI}}{V_{O1} - V_{O2}} \qquad (6)$$

$$R_B = \left(\frac{V_{O1}/V_{FB} - 1}{R_T} - \frac{1}{R_X} - \frac{1}{R_Y} \right)^{-1} \qquad (7)$$

V_{O3} is not included in the equations, indicating that one of the four voltages is not independent of the others. The exact state/voltage that is not independent is determined by the method used to derive Equations 5, 6, and 7 but is one of the states during which the control signals are opposites (the second or third state in Table 2). In this case, the third state with V_{X_HI} and V_{Y_LO} is the dependent state and produces 1.40 V. Equations 5, 6, and 7 were used to find values for resistors R_X, R_Y, and R_B in Figure 13, given R_T = 402 kΩ, V_{O1} = 1.8 V, V_{O2} = 1.5 V, V_{O4} = 1.1 V, V_{X_HI} = 3.3 V, V_{X_LO} = 0 V, V_{Y_HI} = 3.3 V, V_{Y_LO} = 0 V, and V_{FB} = 0.5 V. Figure 14 shows the transition between the levels when V_{IN} = 3.3 V and R_{LOAD} = 10 Ω, using the circuit in Figure 13.

When injection resistors are used instead of FET switches, the transitions between voltages are much smoother.

Dynamic voltage scaling is a means of conserving power and therefore of extending battery life in portable electronics. There are two basic methods of implementing

Figure 14. Transition between three voltages
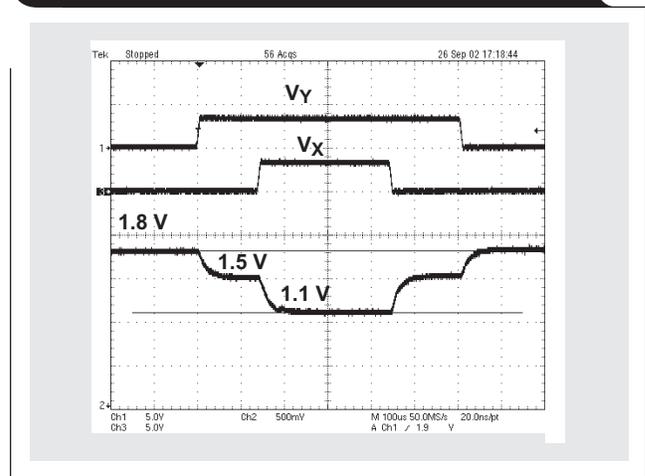
DVS using any adjustable power IC and an external control signal. If the control signal has a poor tolerance or can drive only capacitive loads, then the first method, consisting of FET switches in series with additional feedback resistors, is recommended. If the control signal has an acceptable tolerance and can drive a small resistive load, then the second method, using the control signal to inject current into the feedback network, is a simpler option and offers smoother transitions between voltages.

Related Web sites

analog.ti.com
www.ti.com/sc/device/TPS62200

Understanding piezoelectric transformers in CCFL backlight applications

By Michael Day (Email: m-day@ti.com), *Applications Manager, Portable Power Products,*
and Bang S. Lee (Email: banglee@ti.com), *Application Specialist, Power Management*

Market forces are reducing both the size and energy consumption requirements of portable devices such as PDAs, Internet appliances, and subnotebook computers. Low-profile cold cathode fluorescent lamp (CCFL) backlight solutions are commonly used in these applications. Traditional topologies have used magnetic transformers to generate the high strike and operating voltages required by CCFL lamps. The latest developments in ceramic piezoelectric transformers (PZTs) make them ideal candidates for low-profile back-light applications. PZTs have higher efficiency, smaller size, lower electromagnetic noise, and higher available strike voltage than magnetic transformers. They are also nonflammable and require only easy-to-generate sinusoidal drive voltages. Ceramic PZT operation is fundamentally different from magnetic transformer operation. A successful design requires an understanding of piezoelectric characteristics and how they relate to driving CCFL lamps.

Figure 1. Piezoelectric effect

PZT theory

Magnetic transformers transfer energy from primary to secondary by coupling two circuit windings together through a magnetic flux path. In contrast, PZTs transfer energy from primary to secondary through the use of mechanical force. C.A. Rosen first proposed PZTs in 1956.[1] The basic principle of piezoelectric operation is shown in Figure 1. When an electrical potential is applied to a piezoelectric material, the electrical energy is converted to mechanical force. This is referred to as the "reverse piezoelectric effect." When a mechanical force is applied to a piezoelectric material, the material converts the mechanical force to electrical energy. This conversion is referred to as the "direct piezoelectric effect."

Each manufacturer has a unique, and usually proprietary, "recipe" of materials and structural layering that determines its PZT's operating characteristics. Common materials used to make PZTs include lead zirconate and lead titanate. A PZT may be single-layer or multilayer. Single-layer PZTs are inexpensive due to easier manufacturing processes but have relatively low voltage gains (typically 5 to 10). Multilayered PZT designs are more expensive due to the manufacturing process but have higher voltage gains (20 to 70). Multilayer PZTs are almost always used in CCFL applications because the higher gain eliminates the need for a step-up transformer and allows the CCFL to be driven with conventional off-the-shelf inductors.

Figure 2 shows a typical multilayer PZT with "longitudinal-mode" geometry. The primary has multiple layers of ceramic material with electrodes on the top and bottom. An ac voltage applied to the primary electrodes generates a mechanical force that causes the material to resonate. When the material is compressed in the vertical direction, it is expanded in the horizontal direction, and its length is increased. When it is expanded in the vertical direction, it is compressed in the horizontal direction, and its length decreases. The horizontal, or longitudinal, displacement of the primary is mechanically coupled into the secondary, which causes the secondary to vibrate. The mechanical energy in the secondary is then converted to electrical energy, which is transferred to the circuit through the secondary electrode.

Figure 2. Typical longitudinal-mode PZT for CCFL applications
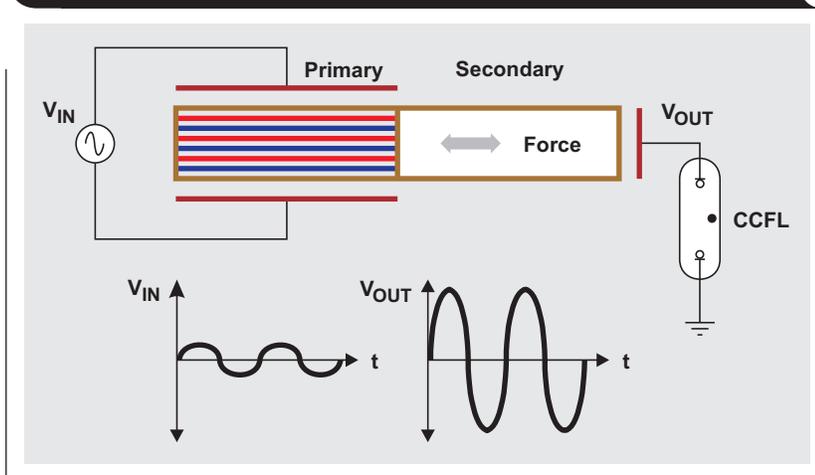
Figure 3 shows the typical construction for a Panasonic PZT (EFTU11R8Mx, EFTU14R0Mxx, and EFTI16R5Mxx series). Notice how the placement of the electrodes corresponds to that shown in Figure 2.

PZT electrical model

To predict PZT performance in a system, it is useful to develop an electrical circuit model. The model shown in Figure 4 is often used to describe the behavior of a longitudinal-mode PZT near the fundamental resonant frequency. Many PZT manufacturers provide component values for the model based on measurements taken at various frequencies and output loads.

The component values depend on the PZT's construction and vary from one PZT part number to another. The input, or primary, capacitance (C_{INPUT}) is formed as a result of the multilayer construction of the primary electrodes and material dielectric constant. This creates a relatively large input capacitance, much like a standard multilayer ceramic capacitor. The output capacitance, C_{OUT}, is much smaller due to the distance between the primary and secondary electrodes. As shown in the following equation, the PZT capacitance is a function of its geometry and material.

$$C_{INPUT} \approx \frac{Length \times Width \times Layers \times \varepsilon}{2 \times Thickness}$$

Figure 3. Typical construction of PZT (Panasonic's (EFTU11R8Mx, EFTU14R0Mxx, EFTI16R5Mxx series)
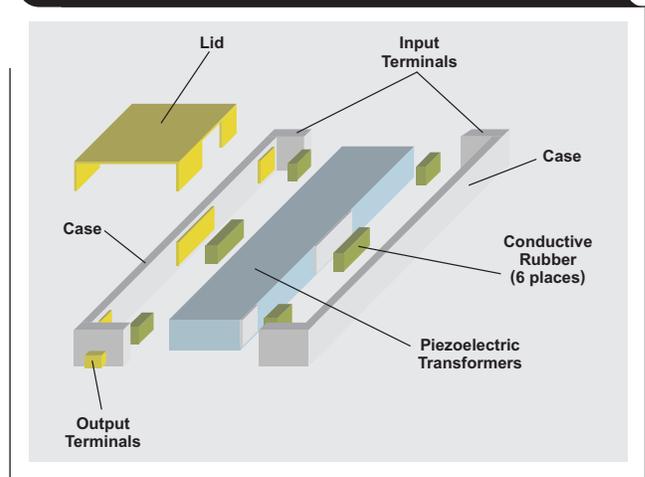
The mechanical resonant frequency, ω_0, of the PZT is also dependent upon geometry and material.

$$\omega_0 \propto \frac{1}{Length} \sqrt{\frac{Y}{\rho}},$$

where Y is the material elasticity and ρ is the material density.

The mechanical piezoelectric gain near a single resonant frequency is modeled by the series R, L, and C circuit as depicted in Figure 4.

$$\omega_0 = \frac{1}{\sqrt{L \times C}}$$

$$Q = \omega_0 \times \frac{L}{R}$$

Component values for a typical 1.8-W PZT (Panasonic part number EFTU11R8MX50) for Figure 4 are $C_{INPUT} = 61.6$ nF; $C_{OUT} = 11.4$ pF; n = 35; and series RLC = 0.66 Ω, 0.94 mH, and 2.79 nF, respectively. The gain and the mechanical resonant frequency of the PZT change with load. These changes directly affect the electrical voltage gain. Figure 5 shows the graph of the electrical voltage gain versus frequency and load for the Panasonic PZT. It also shows that the PZT is capable of providing a large range of voltage gain. The PZT is operated near the 1-MΩ load line to provide the extremely high gain necessary to produce CCFL strike voltages. When loaded, it operates at a much lower gain to provide the lower operating voltages.

Figure 4. Equivalent piezoelectric transformer circuit model
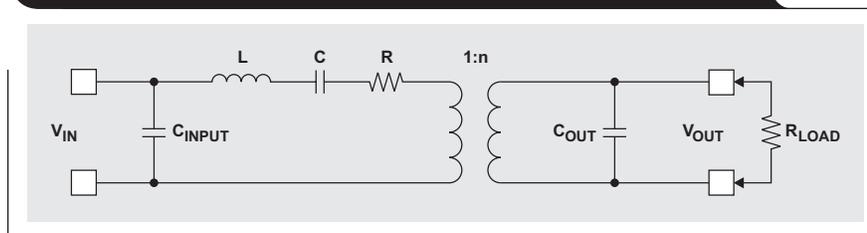
Figure 5. Typical piezoelectric gain characteristics vs. frequency and load
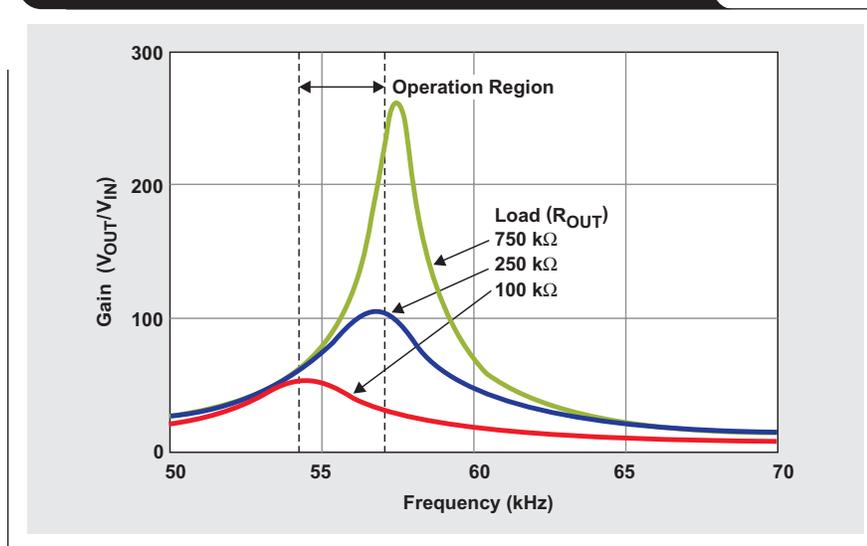
CCFL lamp characteristics

Understanding the electrical operating character-
istics of a CCFL is essential to understanding how
to control its behavior. Before the lamp is ignited,
it has an extremely high resistance and is modeled
as an open circuit. The voltage required to ignite
the lamp is called the strike voltage. The strike
voltage, which is dependent upon lamp length
and diameter, is usually in the range of 500 to
2000 V. Strike voltage can be even higher at cold
operating temperatures. When the lamp strikes,
current begins to flow. The drop in operating
voltage and the increase in current reduce the
dynamic impedance of the CCFL. Figure 6 shows
the nonlinear voltage and current characteristics
of a typical CCFL. Although highly nonlinear, the
lamp impedance can be modeled as a resistor at
any one operating point. Lamp intensity is roughly
proportional to lamp current.

Figure 6. CCFL characteristics
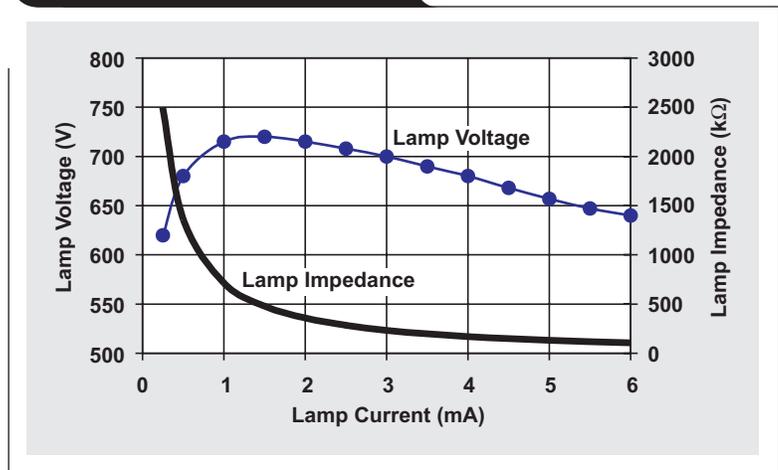
CCFL/PZT interaction

Figure 7 shows the operational interaction between the
CCFL and the PZT. Figure 7 is a combination of Figure 5
(PZT gain versus frequency and load) with Figure 6
(CCFL impedance versus current). Integrating Figures 5
and 6 and examining the result gives insight into the basic

operating principle of the CCFL backlight power-supply
controller. At turn-on, the lamp is an open circuit, so the
PZT operates on the high-gain, high-impedance load line
shown in Figure 7. Since the exact strike voltage and
operating frequency are not known, the controller applies

Figure 7. PZT with CCFL load operating points
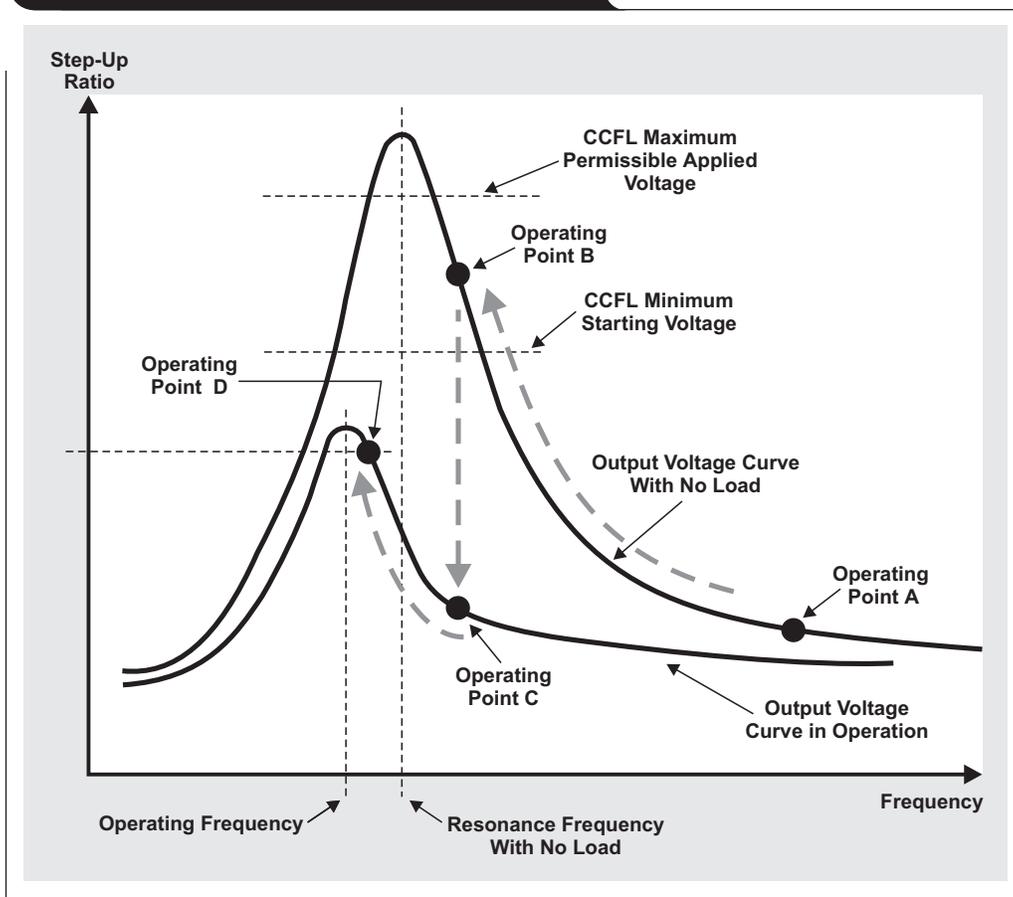
a relatively low voltage to the lamp by operating at the maximum-programmed operational frequency. This is shown as Point A. As the operating frequency is decreased, the PZT gain moves up the no-load line until the CCFL strike voltage is reached. This is shown as operating Point B. At Point B, the CCFL strike voltage is reached and the lamp impedance begins to decrease. The operating frequency continues to decrease as the lamp impedance drops until the correct operating point is reached, somewhere between Points C and D. Varying the operating point between Points C and D controls the lamp intensity. This is accomplished by varying the operating frequency of the converter.

Figure 8 shows a simplified block diagram of a PZT-based backlight converter. The PZT is driven by a resonant power stage whose amplitude is proportional to input voltage. The PZT provides the voltage gain necessary to drive the lamp. A control loop is formed around the error amplifier that compares average lamp current to a reference signal, REF, allowing the intensity of the lamp to be regulated. The resulting control voltage, V_C, drives a voltage-controlled oscillator (VCO) that determines the operating frequency of the resonant power stage. The frequency range of the VCO must include the strike and operating frequencies of the PZT. For example, a frequency range of 51 to 71 kHz is required for proper operation of the lamp characteristics shown in Figure 5. The designer must guarantee that the PZT gain is sufficient to provide the required lamp voltage at minimum input voltage to keep the operating point on the right side of resonance. If the operating point crosses from the right side to the left side of resonance, the supply loses control of the lamp current and the lamp turns off.

Figure 8. Control system for variable-frequency PZT backlight circuit
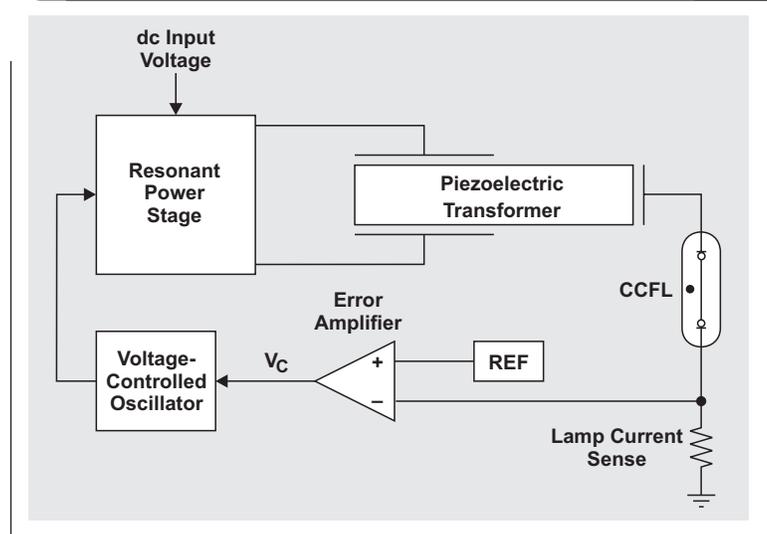
Power topologies

Several topologies exist for the resonant power stage shown in Figure 8. Input voltage range, lamp characteristics, and PZT characteristics determine the correct resonant power stage topology. Some of the more popular choices are the push-pull, half bridge, and full bridge.

Figure 9 shows a basic resonant push-pull topology. The push-pull topology requires two external inductors but has the advantage of providing increased voltage across the PZT primary. This allows a lamp to be operated from a lower input voltage.

Figure 9. Resonant push-pull topology
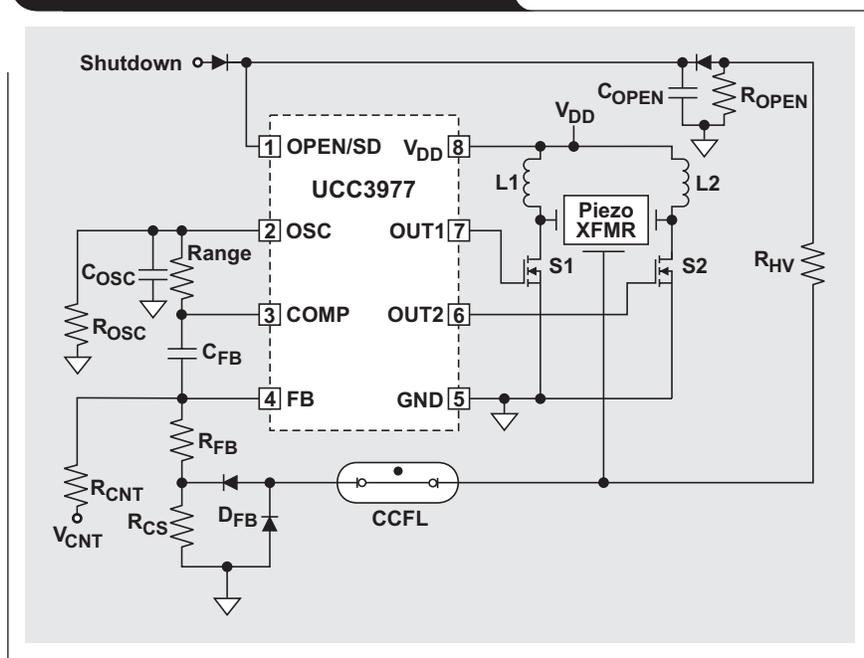
The explanation of circuit operation is fairly simple. For the push-pull circuit, MOSFETs S1 and S2 are driven out of phase with 50% duty cycle at variable frequency (see Figure 10, trace 2). Inductors L1 and L2 resonate with the PZT primary capacitance, forming half sinusoids at the drain of S1 (trace 1) and S2 (trace 4). The resulting voltage across the PZT primary is a near sinusoid (trace M1). Due to the high Q of the ceramic transformer, the lamp voltage, which is approximately 600 V in this particular application, is sinusoidal (trace 3).

To achieve 0-V switching, each drain voltage must return to 0 V before the next switching cycle. This dictates that the LC resonant frequency be greater than the switching frequency. The maximum inductance to meet these conditions can be found from

$$L < \frac{1}{4\pi^2 f^2 C_{INPUT}},$$

where C_{INPUT} is the input capacitance of the transformer primary.

PZT performance

High efficiency can be achieved by selecting the best power topology while matching the lamp, input voltage, and PZT characteristics. Figure 11 shows the performance of a 4-W-rated multilayer PZT operating a 600-V lamp with the push-pull topology at various input-voltage and lamp-current conditions. Electrical efficiency is greater than 85% at lower input voltages, decreasing at higher input voltages as the PZT gain is reduced. This circuit and lamp can operate from 2 Li-Ion cells (5 to 8.2 V). The same PZT and lamp would require 3 Li-Ion cells for a half-bridge topology but would yield similar efficiency.

Dimming by linearly reducing lamp current causes the efficiency to degrade, since the PZT is operated at less than optimal gain (see the 1.5-mA curve in Figure 11). Improved efficiency can be achieved by using burst-mode dimming. This dimming method involves running the lamp at full power but controlling average lamp current by modulating the on/off duty cycle at a frequency higher than the eye can detect (100 Hz, for example).

Figure 10. Push-pull waveforms
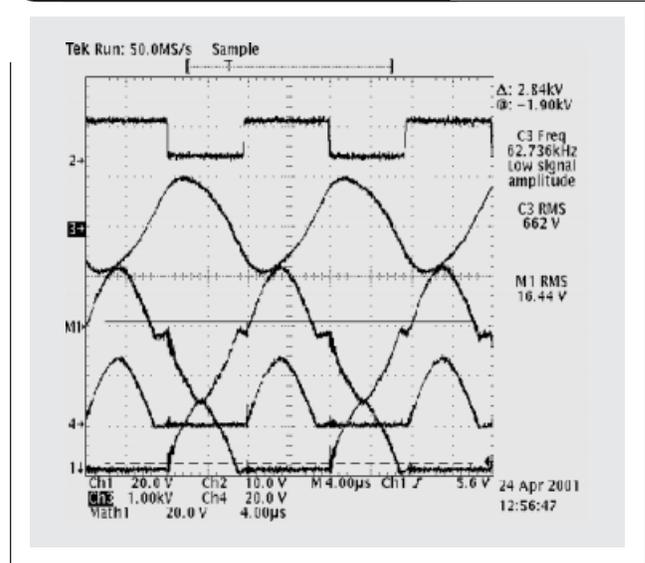
Figure 11. Typical PZT efficiency with input voltage and loading
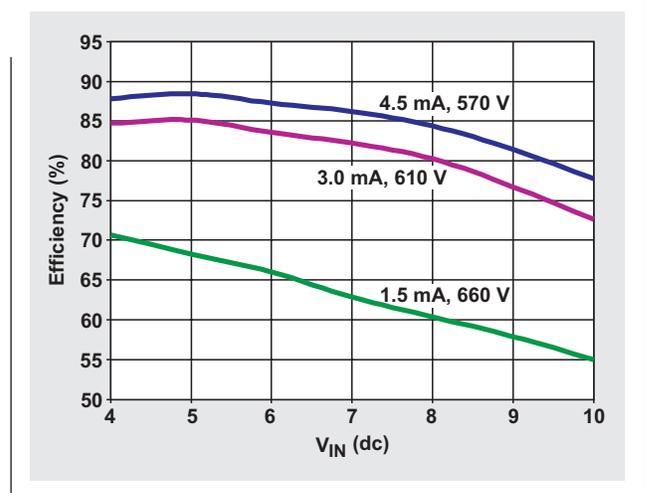
Figure 12 shows plots of PZT operating frequency over the same lamp conditions as Figure 11. As expected, frequency decreases at higher lamp currents as the PZT characteristics shift to a lower operating frequency when loaded (see Figure 5). Frequency increases linearly with input voltage, since the required V_{OUT}/V_{IN} gain to operate the lamp is decreased.

Summary

Piezoelectric transformers offer several advantages for size-constrained, high-performance portable applications. Designing a backlight supply with PZT technology requires a basic understanding of PZT characteristics and performance. A push-pull power topology, along with its various merits for driving a PZT, has been presented. The operation of longitudinal-mode PZTs in a variable-frequency control system has also been reviewed. A successful design will require matching the ceramic transformer to the application to attain high efficiency and stable performance. More information about the control ICs presented in this article can be obtained by contacting the author.

Reference

1. C.A. Rosen, "Ceramic Transformers and Filters," *Proceedings of the Electronic Components Symposium* (1956), p. 205.

Related Web sites

analog.ti.com
www.ti.com/sc/device/UCC3977

Figure 12. PZT operating frequency vs. input voltage and lamp load
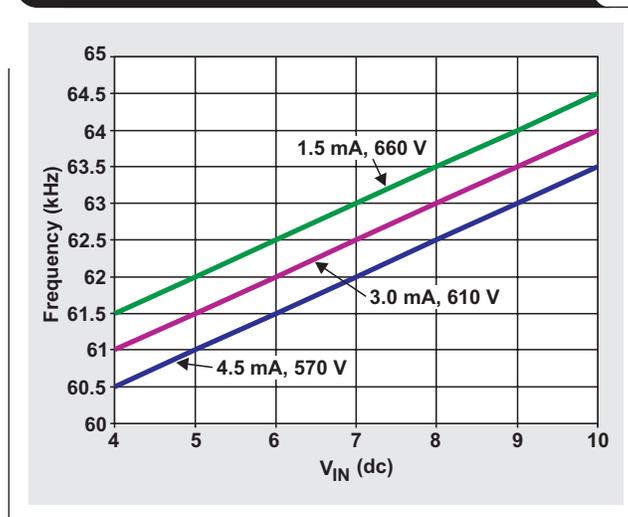
Active output impedance for ADSL line drivers

By Randy Stephens (Email: r-stephens@ti.com)
Systems Specialist, Member Group Technical Staff

Introduction

The exceptional bidirectional data transmission rates over traditional telephone lines are a major factor for the widespread industry growth of ADSL. The ability to transmit data at over 8 MBps over an existing infrastructure of copper telephone lines with limited costs is exciting. There are several key components within the ADSL system, but this article deals solely with the line driver amplifiers.

Because ADSL is considered to be a full-duplex system, able to transmit and receive at the same time, a receiver must be incorporated into the design. The most common way of accomplishing this is to use a hybrid network. The hybrid's function is to cancel out the transmit signal while still being capable of receiving the signals from the customer-premise equipment (CPE) end (also known as the remote-terminal [RT] end). To accomplish this task, series-matching resistors, R_S, are needed and should be equal to one-half the total reflected transmission line impedance to properly match the line impedances (see Figure 1).

$$R_S = \frac{R_{Line}}{2n^2}, \qquad (1)$$

where n is the transformer ratio indicated as 1:n.

The problem with using the series-matching resistor is the associated voltage drop across this resistance. The voltage appearing at the transformer primary side is only one-half the voltage developed at the line driver amplifier output. This is one of the key issues when the power dissipation of an ADSL line driver is considered.

Traditional line driver requirements

ANSI T1.413 specifies that the central office (CO) can nominally transmit at –40 dBm/Hz on a 100-Ω telephone line from approximately 25 kHz to 1.104 MHz. This corresponds to roughly 3.16 V_{RMS} (or +20 dBm) being transmitted on the line. The problem is that ANSI T1.413 also dictates that there shall be a bit-error rate (BER) of 1×10^{-7}. In order to accomplish this feat the ADSL signal must have a peak-to-rms ratio, also known as crest factor (CF), of about 5.6 (15 dB). Taking the crest factor into account, the line voltage must now have a peak voltage of about 17.7 V_{peak} (34.4 V_{PP}). Note that the crest factor can vary

Figure 1. Line driver voltage and current levels to meet ANSI T1.413 requirements
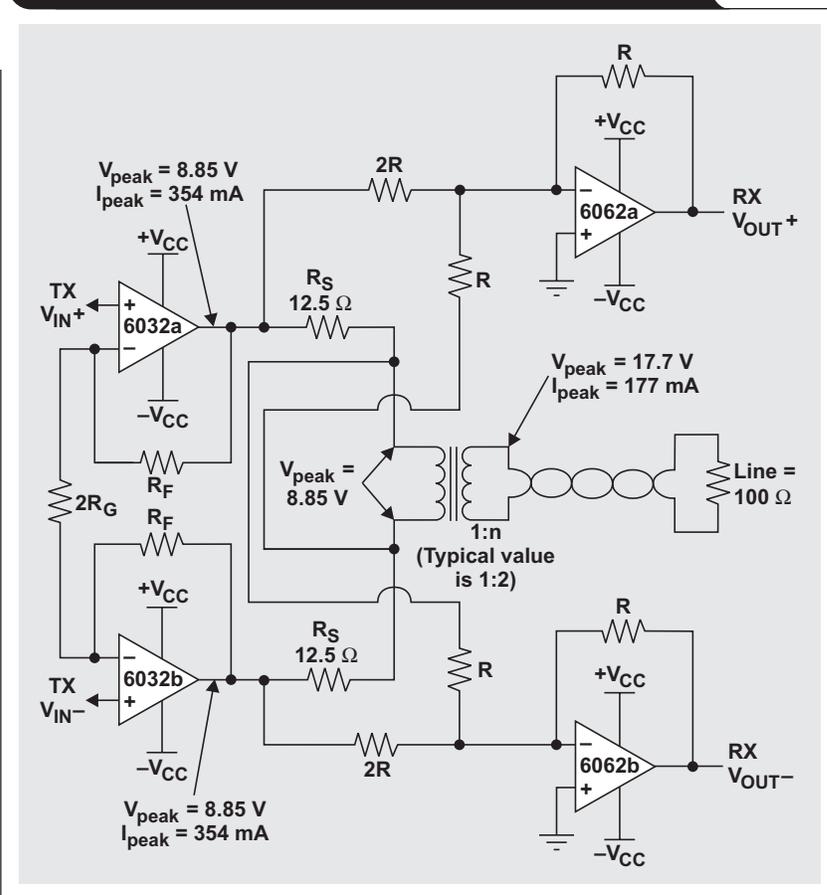
from 5.3 to as high as 7, depending on the manufacturer and the system goals involved.

This large voltage requirement is a key reason for using a transformer and two amplifiers configured differentially to drive the line. Differential circuits have several advantages over single-ended configurations. This includes minimizing common-mode signals and interference, improving power-supply rejection, and the obvious advantage of doubling the voltage swing that appears at the transformer leads. Another advantage of the differential configuration is that even-order harmonics are reduced by as much as 10 to 20 dB, resulting in a very low distortion system.

Because R_S forces the amplifier to swing twice the transformer voltage requirement, the power supplies ($\pm V_{CC}$) must be increased accordingly. This increase in power-supply voltage leads to the primary issue with ADSL line drivers—power dissipation.

Line driver power dissipation

Power dissipation in the line driver amplifier is a dominant factor in CO applications. Let's take an approximation at the power dissipation levels required for the traditional line driver circuit. Let's assume that the amplifier requires at least 2 V of power-supply voltage headroom (i.e., $V_{OUT(max)} = V_{CC} - 2$ V) and there is about a 10% tolerance on the power supply. Since power dissipation of amplifiers is calculated based on the average current flowing into the amplifiers and the dc voltage, the following line driver amplifier power dissipation approximation can be made:

$$P_{Diss} = \left[2(V_{CC} - V_{OUT_{RMS}})(I_{OUT_{RMS}} \times 0.8^*) \right] + P_{Quiescent}. \quad \textbf{(2)}$$

$$P_{Quiescent} \approx 4 \times V_{CC} \times I_{CC} \times 0.7.^{**} \quad \textbf{(3)}$$

To solve for power dissipation, let

$$V_{CC(min)} \approx V_{OUT(max)} + V_{Headroom} + V_{CC_{Tolerance}}$$
$$= 8.85 \text{ V} + 2 \text{ V} + 1.1 = 11.94 \text{ V}$$
(choose standard voltage 12 V_{DC}).

$$V_{OUT_{RMS}} = 8.85 \text{ V}_{peak} \div 5.6 = 1.58 \text{ V}_{RMS}.$$
$$I_{OUT_{RMS}} = 354 \text{ mA}_{peak} \div 5.6 = 63.2 \text{ mA}_{RMS}.$$
Let $I_{CC} = 12 \text{ mA}_{DC}$.
$$\therefore P_{Diss} \approx 1.05 \text{ W} + 0.40 \text{ W} \approx 1.45 \text{ W}.$$

As you can see from the calculation, 1.45 W is a lot of power for a single device to dissipate. To compound the problem, there are as many as 72 ADSL lines on a single PCB. This is an enormous amount of heat to try to dissipate while trying to maintain proper silicon die temperatures.

Minimizing power dissipation

Power reduction is easily accomplished by reducing the series-matching resistors (R_S) to a much smaller value. The voltage drop across these resistors is then minimized. The amplifier output voltage is reduced by the same amount that allows the power-supply voltages to be reduced. Because the voltage difference between the power-supply voltage and the rms output voltage is reduced, power dissipation is also reduced. The quiescent power is reduced as well, due to the dropping power-supply voltages. Using the previous example, we can see the amount of power that will be saved by simply utilizing a smaller resistor. Let new R_S equal 13% of the original R_S value.

$$\text{New } V_{OUT(max)} = 1.13 \times \text{old } V_{OUT(max)} \div 2 = 5 \text{ V}.$$

$$\text{New } V_{CC} = (5 \text{ V} + 2 \text{ V}) \times 1.1 = 7.7 \text{ V}$$
(choose standard voltage 8 V_{DC}).

---

* The ADSL signal is considered to have a Gaussian distribution in the time domain. Because of this, multiplying the amplifier's rms output current by approximately 0.8 yields the average current drawn from the power supply due to the output signal current.

** This multiplication factor accounts for the fact that part of the quiescent current in a Class-AB amplifier gets diverted to the load when there is a signal appearing at the output of the amplifier driving a load. The number chosen is only an approximation and is shown only as a reference. Typical numbers range from 0.4 to 0.9 and are based on numerous circuit parameters internal to the amplifier.

$$\text{New } V_{OUT_{RMS}} = 5 \text{ V} \div 5.6 = 0.893 \text{ V}.$$

$$\text{New } I_{OUT_{RMS}} = \text{old } I_{OUT_{RMS}} = 63.2 \text{ mA}.$$

$$\therefore \text{New } P_{Diss} \approx 0.72 \text{ W} + 0.22 \text{ W} \approx 0.94 \text{ W}.$$

This is a savings of 0.51 W, or 35%, per ADSL channel. When there are several channels on a single PCB, this can add up to substantial heat savings. The die temperature is also reduced, allowing for better performance and longer life of the amplifier.

However, this configuration fails to allow for proper line impedance matching. To get the best of both worlds, utilizing small series resistors and matching the line impedance, we need to use an "old" circuit configuration—the active termination circuit (also known as synthesized impedance).

Active termination

Active termination has been around for several years.[1,2] The idea is to use a small ohmic value resistor for R_S. The circuit then utilizes positive feedback to make the impedance of this resistor appear much larger from the line side.

This accomplishes two things: (1) a very small resistance when the line driver amplifier transmits signals to the line, and (2) proper matching impedance between the line and the amplifier. Most of the original designs, however, were single-ended applications instead of the differential configuration used in ADSL systems.

Taking the general idea a step further, we can utilize the fact that the signals from each amplifier are 180° out of phase from each other in the differential system. We use these signals and connect them into the traditional inverting node on the amplifier (minus input) instead of the non-inverting node (plus input) used in the single-ended application. The advantages of this are: (1) The effective impedance of the noninverting inputs is not dictated by the positive feedback resistance and voltage gain; and (2) the active impedance achieves cross-coupling of the signals. Cross-coupling helps minimize differences between the two amplifier output signals, helping to keep the signals fully differential. Figure 2 shows the basic circuit for differential positive feedback.

Figure 2. Basic active impedance circuit
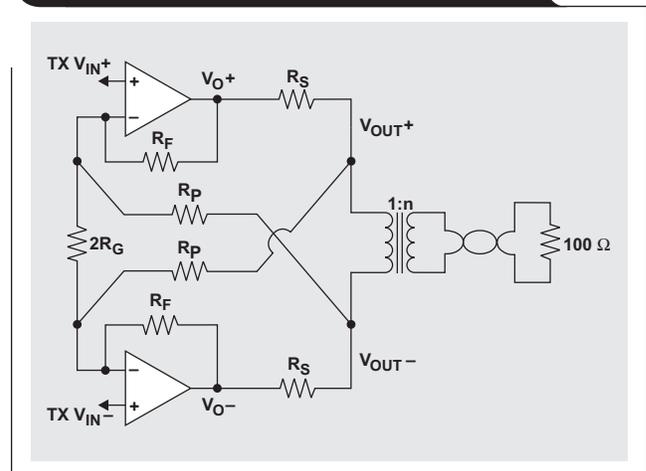
The first question to answer is: How does this circuit configuration increase the effective resistance of R_S when looking from the line? If we assume that the TX inputs are grounded and apply a voltage at $V_{OUT}-$, this creates a voltage at V_O+ equal to $V_{OUT}- \times -RF/RP$. If we also realize that the voltage at $V_{OUT}+$ is equal to $-V_{OUT}-$, then $V_O+ = V_{OUT}+ \times RF/RP$. This makes R_S appear to be a larger impedance, Z, by the following formula:

$$Z(\Omega) = \frac{R_S}{1 - \frac{R_F}{R_P}}. \tag{4}$$

The important thing to consider is that regardless of the forward gain from V_{IN} to V_O, the active impedance value remains constant. The drawback to this arrangement is that the impedance will change at frequencies near the amplifier's bandwidth limit. We must ensure that the amplifier used has a bandwidth high enough not to alter the impedance at the ADSL frequencies from 25 kHz to 1.1 MHz. As a general rule of thumb, the amplifier must have a minimum bandwidth of 10 times the maximum operating frequency, or at least 11 MHz with the amplifier's intended gain.

Active impedance forward gain

Once the return impedance is corrected, we need to turn our attention to the rest of the design parameters. The most fundamental is the forward voltage gain from input to output. For simplicity, we will assume that the amplifier is well within its linear range and ignore bandwidth effects. Equation 5 shows the simplified forward gain from V_{IN} to V_O.

$$A_V = \frac{V_O\pm}{V_{IN}\pm} = \frac{1 + \left(\dfrac{R_F}{R_G\|R_P}\right)}{1 - \left(\dfrac{R_F}{R_P}\right)\left(\dfrac{R_L}{R_L + R_S}\right)} \quad \text{if } R_L \ll R_P, \tag{5}$$

$$\text{where } R_L = \frac{R_{Line}}{2n^2}. \tag{6}$$

In the original circuit (the classic design shown in Figure 1), R_S equaled one-half the total reflected line impedance, which also equaled R_L. We must now choose R_S as a percentage of R_L in the active termination circuit. If we define the variable X as this percentage, where $0 < X \le 1$, then we can start simplifying the preceding equations. Some references use the term "synthesis factor" (SF) to describe the percentage. Synthesis factor is simply $1/X$, but the remainder of this article uses the variable X. If we realize that the term

$$\frac{R_L}{R_L + R_S}$$

is held constant, we can make several simplifications. The first sets of assumptions are

$$R_S = R_L X \text{ and} \tag{7}$$

$$\frac{R_L}{R_L + R_S} = \frac{1}{1 + X}. \tag{8}$$

We will also assume that we want the active impedance, Z, equal to the terminating resistance, R_L. Equation 4 is manipulated to achieve

$$R_P = R_F \left(\frac{1}{1-X}\right) = \frac{R_F}{1-X}. \tag{9}$$

Equation 9 shows that to properly match the active termination impedance, we need only select an arbitrary value of R_F. Substituting Equations 7 through 9 in Equation 5 leads us to the simplified forward voltage gain of

$$A_V = \frac{R_G[(1+X)(2-X)] + R_F(1+X)}{2R_G X}. \tag{10}$$

If we know the forward gain we want in the system, we can rearrange Equation 10 to solve for the gain resistance, R_G:

$$R_G = \frac{R_F(1+X)}{2A_V X - [(1+X)(2-X)]}. \tag{11}$$

Minimum active impedance forward gain design constraint

Because active impedance utilizes positive feedback, it is possible to create negative impedance instead of positive impedance. Negative impedance makes the series resistance appear to decrease rather than to increase as desired; so we must ensure that there is always positive impedance. We come to our first design constraint of the active termination circuit: There must be a minimum forward gain for the system to work properly.

Because we want to match the line properly, we must first arbitrarily choose R_F. Using Equation 9 dictates a specific fixed value for R_P. This leads to R_G solely dictating the forward voltage gain for any given value of X. The minimum forward voltage gain allowed is when R_G is not even in the system, resulting in

$$A_{V(min)} = \frac{2 + X - X^2}{2X} = \frac{(1+X)(2-X)}{2X}. \tag{12}$$

Luckily, for most ADSL systems, the gain of the amplifiers is typically greater than 10 V/V. Meeting the minimum gain requirement is usually not an obstacle as long as the value of X is greater than about 10%. As long as the minimum forward gain is met, the low-power active termination system will work properly.

Line impedance changes

Up until now, we have assumed that the line was a fixed value (usually 100 Ω). But in reality, we know that the line impedance is highly complex. Typically the line impedance can range from as low as 50 Ω up to as high as 300 Ω over the ADSL frequency spectrum. Since the positive feedback

is obtained between R_S and the reflected line impedance (R_L), it stands to reason that the forward voltage gain will be affected.

To quantify the exact change in forward voltage gain, the variable Y is introduced. Let the variable Y equal the percentage change in the reflected line impedance (R_L). This leads to the new forward voltage gain:

$$A_V = \frac{R_G[(2-X)(1+X+Y)] + R_F(1+X+Y)}{R_G X(2+Y)}. \tag{13}$$

Figure 3 illustrates the percentage change in forward gain with varying values of X. The forward gain with a 100-Ω line impedance will be used as the base line for comparison.

It is interesting to note that the change in percentage gain is independent of the transformer ratio, n; feedback resistance, R_F; gain resistance, R_G; and initial amplifier gain, A_V.

The minimum forward gain will also vary with the line impedance. The minimum forward gain becomes

$$A_{V(min)} = \frac{(2-X)(1+X+Y)}{X(2+Y)}. \tag{14}$$

Figure 4 illustrates the minimum forward gain with varying line impedance.

When an active termination system is designed, it does not matter what initial design line impedance is used. As long as the minimum gain criterion is met, the system should not create negative impedances.

Line impedance changes and the amplifier output voltage

In a real system it is quite common for forward voltage gain to change ±20%, which must be accounted for. If not, the input signal can be amplified too high and clipping could easily occur. Excess distortion, data transfer rate, line reach, and even power dissipation could become worse if the line impedance is not handled properly within the active impedance circuit design.

Examining the circuit of Figure 2 and using Equation 7 will help us calculate how the line impedance changes the amplifier's output voltage. We will assume that R_S is designed for a 100-Ω system and is held constant. We will also assume that the power on the line was done with a 100-Ω line impedance and is +20 dBm. This corresponds to a line voltage of 3.162 V_{RMS}. The formula used to find the corresponding amplifier voltages is

$$V_{O_{RMS}} = \frac{V_{Line_{RMS}}(R_{Line} + 2n^2 R_S)}{2nR_{Line}}. \tag{15}$$

The important number is the peak output voltage of the amplifier ($V_{peak} = V_{RMS} \times CF$) because a given supply voltage determines how much voltage swing can occur. Failure to plan for varying line impedances can cause

Figure 3. Forward gain change with varying line impedance
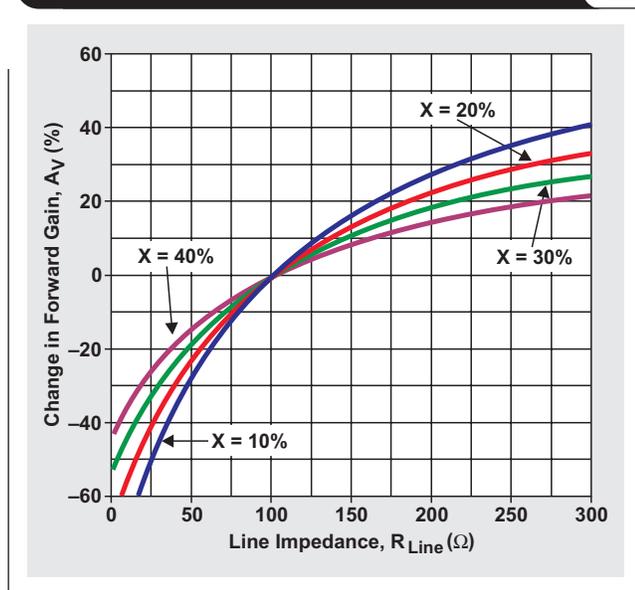
Figure 4. Minimum forward gain change with varying line impedance
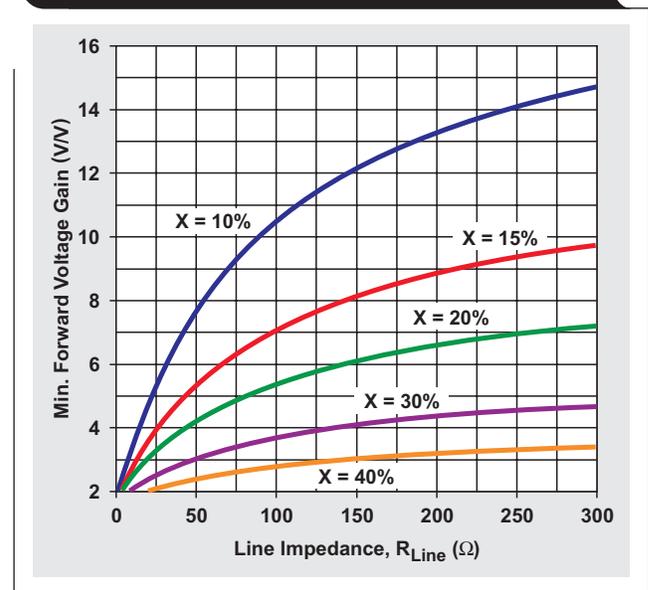
some serious problems. Figure 5 illustrates this issue with X = 20% (SF = 5) and a crest factor of 5.3.

Obviously, as the crest factor increases, the peak output voltage will also increase. Additionally, when R_S increases, the amplifier output voltage will also increase. The obvious question is: Why not use the smallest resistance possible? There are several reasons for this that the remainder of this article explains in detail.

Lab tests

Setup

The first test examined how the resistor values affect the system. Because the THS6032, like most ADSL line drivers, is a current feedback (CFB) amplifier, the feedback resistance (R_F) dictates the bandwidth and the stability of the amplifier. Keeping a high bandwidth increases the amplifier's excess open-loop gain in the ADSL frequency band and reduces distortion. At the same time, however, the amplifier bandwidth may be high enough to interact with the transformer's resonance frequency, which can cause possible instabilities in the overall system. This is especially true when active impedance circuits are used, as R_S can become very small, resulting in very little isolation between the amplifier and the transformer. When you consider Equations 13 to 15 along with the transformer's impedance at resonance, it is apparent that the system can potentially become unstable. Using a simple RC snubber across the transformer can be a simple solution for instability concerns.

To circumvent this potential issue, two new amplifiers from Texas Instruments, the THS6132 and the THS6182, incorporate special internal circuitry. These new amplifiers yield extremely low distortion at the ADSL frequencies yet have a bandwidth of only 10 to 20 MHz—depending on the system design. For all other line drivers, the trade-off of bandwidth and stability needs to be managed. As a side benefit of reducing the feedback resistor, the overall output noise of the line driver system can be significantly reduced.

Figure 6. Amplifier effective output impedance viewed from transformer primary winding

Figure 5. Amplifier peak output voltage with X = 20%

For the THS6032 testing, a feedback resistor value of 1150 Ω was chosen. The rest of the system component values were then easily calculated with the previous equations. The only other variable was that the gain of each amplifier was set to approximately +12 V/V. This allowed testing of the X = 10% system where the appropriate minimum gain requirement was about 10.5. As R_S was increased, the gain also had to be increased to account for the additional voltage drop from the added series resistance.

The active impedance test

Figure 6 shows the impedance looking back into R_S from the transformer primary. It clearly shows the amplifier's closed-loop bandwidth effects. Eventually the amplifier's own output impedance takes over regardless of the termination system used. At this point the impedance is out of the designer's control. Since the ADSL spectrum is well controlled, the system will meet its designated functionality as a low-power line driver.

One area of concern with using active impedance is that lightning surge tests could overwhelm the amplifiers' internal circuitry and cause failures due to a decreased real resistance between the amplifier and the transformer. The larger the resistance, the better the chance that no damage will occur within the amplifier. If the active impedance configuration is utilized, then R_S should be a "respectable" value and not something trivial (for example, 1 Ω). Most systems should strive for a value of 20 to 30% of R_L (SF = 3 to 5). This allows for respectable power savings and reasonable isolation from surges on the line.

Power dissipation and distortion

The line impedance used in the testing was a 100-Ω resistor. Variable line impedance issues are not of concern but should constrain the final system design. As a result, the power dissipation numbers shown should be considered optimal for a particular test setup. When a varying line impedance is thrown into the mix, the power-supply voltages will need to be adjusted accordingly and the power dissipation will increase.

The other factor hampering the power dissipation is that the THS6032 requires 4-V headroom from the power supplies. This is due to the Class-G architecture requiring multiple series transistors in the output stage. If a very low headroom amplifier were used (such as the THS6132 or THS6182), the power-supply voltage could be reduced by at least ±2 V, decreasing power even more. As we are concerned with power savings in general, these results can be used to draw some general conclusions about the use of active termination in an ADSL application.

Keep in mind that when you compare power numbers from amplifier to amplifier, the entire system configuration needs to be divulged. This includes things such as crest factor; accounting for varying line impedances; accounting for power-supply tolerances; and, of course, the synthesis factor. Because of the numerous options available, doing a true apples-to-apples comparison is often very difficult when you just look at manufacturers' data sheets.

As a reference for the active termination testing, a THS6032 was tested with the traditional configuration

shown in Figure 1. To really see the effects of the Class-G circuitry in action, refer to Figure 7, which shows how changing the V_{CC-L} supply voltages alters the power dissipation. For reference, it also shows the power consumed in each set of supplies. In Class-AB mode, power dissipation is about 1.8 W; but in Class-G mode, the best power achieved is approximately 1.35 W with V_{CC-L} at ±6 V. The multitone power ratios (MTPRs) were –70 dBc for Class-AB operation and –68 dBc for Class-G operation.

Figure 8 shows how the crest factor affects power dissipation with a 1:1.2 transformer and X = 20% (R_S = 6.94 Ω). The power-supply voltage was chosen to give an additional ±0.5-V headroom for a design margin. In the lab, we could set the supplies ±1 V lower before clipping started to occur; but this is not considered good practice, as power-supply tolerances and component tolerances could come into play. The power dissipation numbers shown are thus considered to be realistic and within the safe operating area of the system.

When compared to the traditional circuit design, the active termination circuit saved a huge 47% in power dissipation. This was true for both Class-AB operation and Class-G operation. For the active termination data, the use of Class-G operation saved an additional 20 to 25% power dissipation compared to the Class-AB operation. As expected, when the crest factor increased, the power dissipation also increased by as much as 25%. This was mainly due to the increase in power-supply voltage required to handle the larger peak voltages.

Figure 7. Traditional circuit design power dissipation results
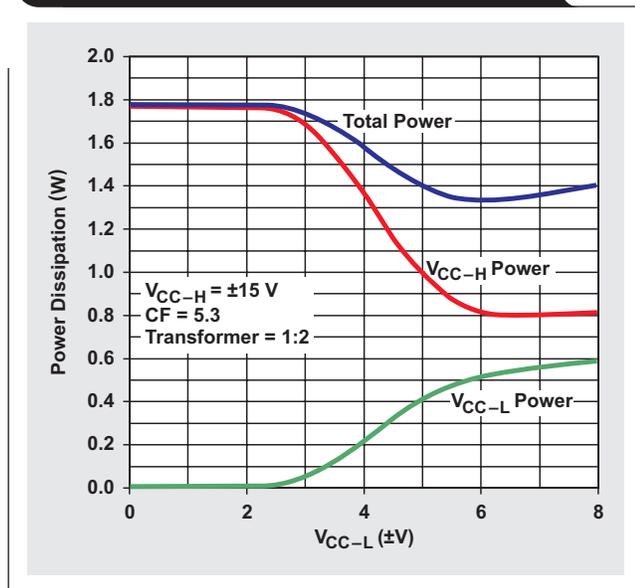
Figure 8. Power dissipation with 1:1.2 transformer and different crest factors
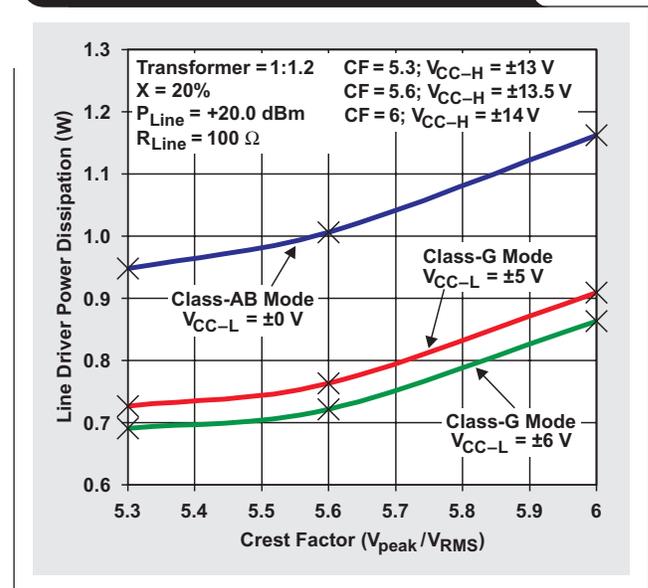
Figure 9 shows how changing R_S affects the power dissipation. A common crest factor of 5.3 was used to illustrate the change in the system.

If the power-supply voltages had been held constant and no clipping had occurred, the power dissipation would have decreased with an increase in R_S; but the testing was done to show the best possible performance with a given set of constraints. The power-supply voltages thus were increased as R_S was increased to compensate for the increase in output voltage required from the amplifier. The power-supply voltages ranged from ±12.5 V (X = 14%) to ±14 V (X = 40%).

The last thing to check was the effect of MTPR distortion on the system.

Figure 10 shows us that as R_S increases, the MTPR distortion decreases. The designer has to choose between lower distortion and lower power dissipation. As stated earlier, a series resistance of 20 to 30% of R_L should give good results for both requirements.

Power dissipation and MTPR with multiple transformer ratios

The purpose of the next series of tests was to find out if there is a general relationship between the transformer ratio and the power dissipation. For each transformer ratio tested, the corresponding resistor values and power-supply voltages were accordingly changed. Figure 11 shows how changing R_S affects power dissipation with varying transformer ratios.

Figure 9. Power dissipation with 1:1.2 transformer and varying R_S
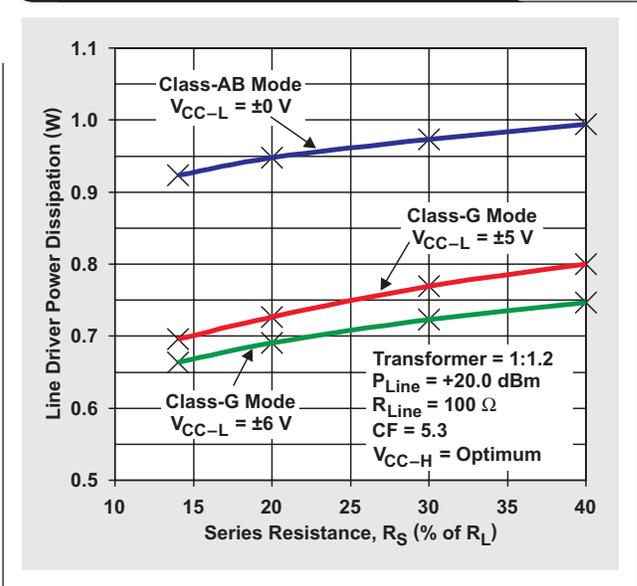
Regardless of the power-supply voltages and the mode of operation, as R_S increases, the power dissipation increases. This is generally dominated by the amplifier's overhead

Figure 10. MTPR with 1:1.2 transformer and varying R_S
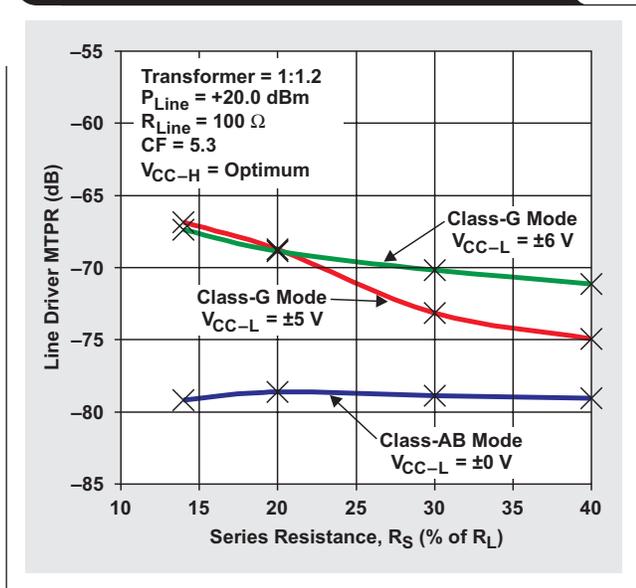
Figure 11. Power dissipation with varying transformer ratios
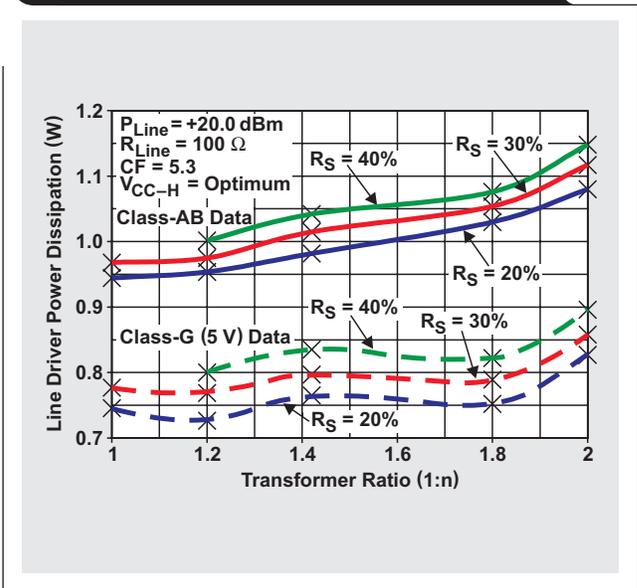
voltage requirements and quiescent current. We now come to the final test—determining the effects of varying transformer ratios on MTPR distortion. Figure 12 shows the effects of R_S on MTPR distortion with a changing transformer ratio and the same setup that was used before.

The data tells us that increasing the physical value of R_S lowers MTPR distortion. This is because distortion in operational amplifiers generally gets better with an increase in load resistance. In the case of the ADSL configuration, increasing R_S also helps isolate the complex loading that the transformer places on the amplifier. Comparing the 1:2 transformer data with the traditional circuit design shows that MTPR performance degrades by 4 to 5 dB as the transformer ratio increases.

Conclusion

Reduced power dissipation is the main goal for using active termination in ADSL systems. Using a 1:1.2 transformer saved 47% of power regardless of the mode in which the THS6032 was used. This translates to a savings of up to 0.85 W with Class-AB operation and 0.63 W with optimal Class-G operation. In light of the distortion and power savings, choosing a value for X of 0.2 to 0.3 (SF = 3 to 5) shows about the best overall performance.

Using TI's newest amplifiers, THS6132 (Class-G) or THS6182 (Class-AB), can save substantially even more power. Initial testing with the THS6132 in Class-G operation shows a total power consumption of as low as 0.53 W, which is a power dissipation of roughly 0.43 W over the THS6032. However, keep in mind the design constraints of the active termination system. The line impedance variations, the minimum power-supply voltages, and the system crest factor all contribute to the power consumption of the line driver.

With any electrical circuit, there are trade-offs to using one configuration over another. The active impedance circuit is no exception. The trade-off to achieving lower line driver power dissipation is that the receiver circuitry will require more voltage gain to overcome the voltage reduction appearing across R_S. This can play a significant role in the noise performance of the system. One way to help alleviate this problem is to use a smaller transformer ratio; but the power-supply voltages will have to be increased, which can increase power dissipation. The added benefits of an increased series resistance can help in many other areas of the system, including distortion and

Figure 12. MTPR distortion with varying transformer ratios
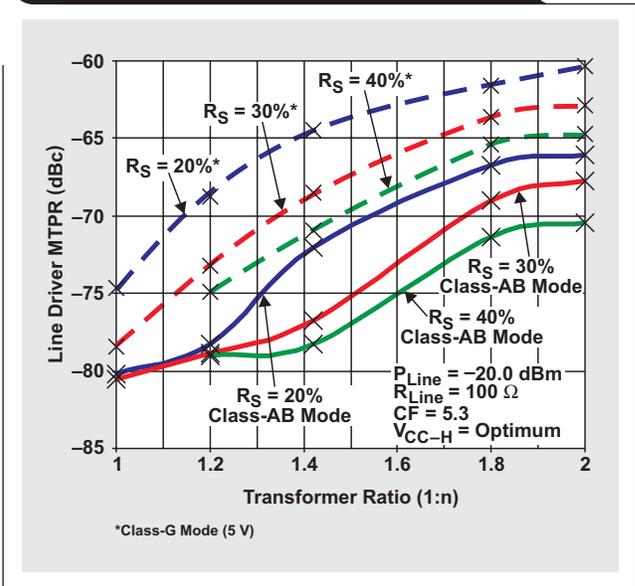
surge isolation. Ultimately, the goal of saving power can still be met while satisfying all requirements of the ADSL line driver system.

Additional information will be available in an application note to be released by January 2003, at www-s.ti.com/sc/techlit/sloa100

References

1. Jerry Steele, "Ideas For Design - Positive Feedback Terminates Cables," *Electronic Design* (March 6, 1995), pp. 91-92.
2. Donald Whitney Jr., "Design Ideas - Circuit Adapts Differential Input to Drive Coax," *Electronic Design News* (May 8, 1997), pp. 132-34.

Related Web sites

analog.ti.com
www-s.ti.com/sc/techlit/sloa100 (available January 2003)
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with THS6032, THS6132 or THS6182

Index of Articles

33

TI Worldwide Technical Support

Internet

**TI Semiconductor Product Information Center
Home Page**
support.ti.com

TI Semiconductor KnowledgeBase Home Page
support.ti.com/sc/knowledgebase

Product Information Centers

Americas

Phone	+1(972) 644-5580
Fax	+1(972) 927-6377
Internet/Email	support.ti.com/sc/pic/americas.htm

Europe, Middle East, and Africa

Phone

Belgium (English)	+32 (0) 27 45 55 32
Finland (English)	+358 (0) 9 25173948
France	+33 (0) 1 30 70 11 64
Germany	+49 (0) 8161 80 33 11
Israel (English)	1800 949 0107
Italy	800 79 11 37
Netherlands (English)	+31 (0) 546 87 95 45
Spain	+34 902 35 40 28
Sweden (English)	+46 (0) 8587 555 22
United Kingdom	+44 (0) 1604 66 33 99
Fax	+(49) (0) 8161 80 2045
Email	epic@ti.com
Internet	support.ti.com/sc/pic/euro.htm

Japan

Fax	International	+81-3-3344-5317
	Domestic	0120-81-0036
Internet/Email	International	support.ti.com/sc/pic/japan.htm
	Domestic	www.tij.co.jp/pic

Asia

Phone		
International		+886-2-23786800
Domestic		Toll-Free Number
	Australia	1-800-999-084
	China	108-00-886-0015
	Hong Kong	800-96-5941
	Indonesia	001-803-8861-1006
	Korea	080-551-2804
	Malaysia	1-800-80-3973
	New Zealand	0800-446-934
	Philippines	1-800-765-7404
	Singapore	800-886-1028
	Taiwan	0800-006800
	Thailand	001-800-886-0010
Fax		886-2-2378-6808
Email		tiasia@ti.com
Internet		support.ti.com/sc/pic/asia.htm

Important Notice: The products and services of Texas Instruments Incorporated and its subsidiaries described herein are sold subject to TI's standard terms and conditions of sale. Customers are advised to obtain the most current and complete information about TI products and services before placing orders. TI assumes no liability for applications assistance, customer's applications or product designs, software performance, or infringement of patents. The publication of information regarding any other company's products or services does not constitute TI's approval, warranty or endorsement thereof.

A070802

FilterPro and SWIFT are trademarks of Texas Instruments. Celeron is a trademark of Intel Corporation.

SLYT042

35