Texas Instruments

HIGH VOLTAGE SEMINAR

MAMADOU DIALLO

HIGH POWER GATE DRIVERS

TROUBLESHOOTING GATE DRIVE CIRCUITS IN AUTOMOTIVE AND INDUSTRIAL APPLICATIONS

Acknowledgement

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What will I get out of this session?

Purpose:

- **Gate driver Fundamentals**
- **Common issues, solutions and design practices on:**
  1. Bias/bootstrap supply
  2. Open functional pins or connect with Hi-Z
  3. Parasitics
  4. dv/dt noise
  5. Variance

Part numbers mentioned:

- UCC27282
- UCC27710
- UCC27284-Q1
- UCC27201
- UCC27524

Relevant applications:

- Motor drive
- Switch mode power supplies
- Solar inverters

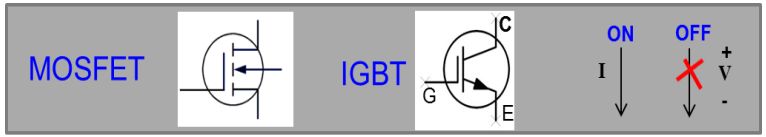
Where are gate drivers used?

Fundamental Component in Power Electronics

Input (V_{IN}, I_{IN}, P_{IN}) → **Switch-Mode Power Converter** → Output (V_{OUT} I_{OUT}, P_{OUT})

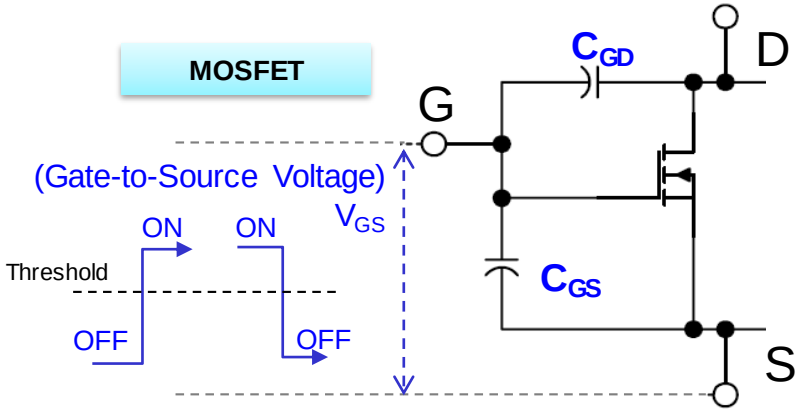
AC-DC (or) DC-DC (or) DC-AC

Power Switches control flow of current in power electronic circuits by operating in 2 states (ON/OFF)



GATE (G) terminal controls ON/OFF status of switch

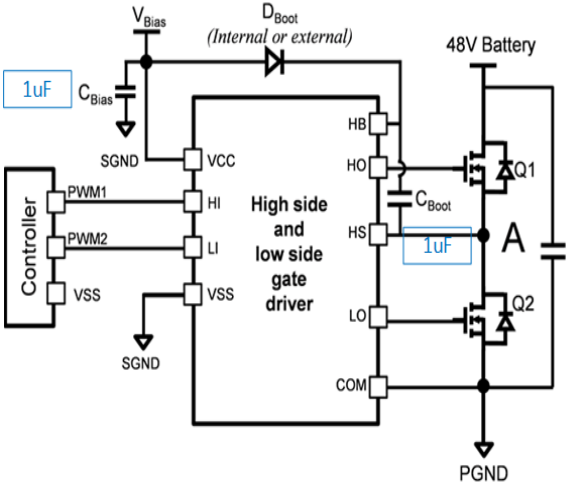
Si → GaN and SiC



To turn ON: Apply a positive voltage, VGS > Threshold level

To turn OFF: VGS < Threshold level

#1 What is wrong with VCC?



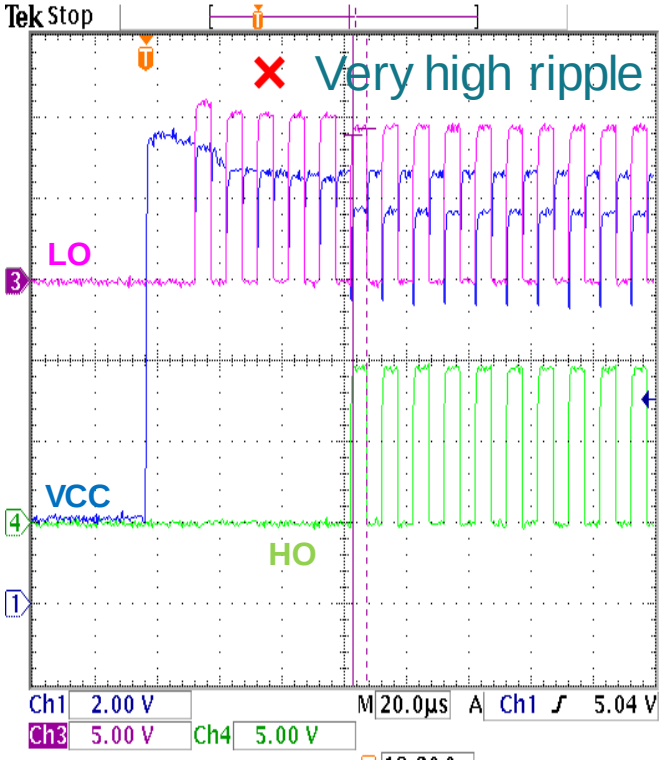
Causes

- Low capacitance on V_{CC}
- Capacitor placement/layout
- Biased capacitance (C vs. V)
- Temperature (C vs. temp)
- Capacitance aging

Consequences

- ✕ Driver malfunction
- ✕ UVLO tripping
- ✕ EMI noise

Bias supply



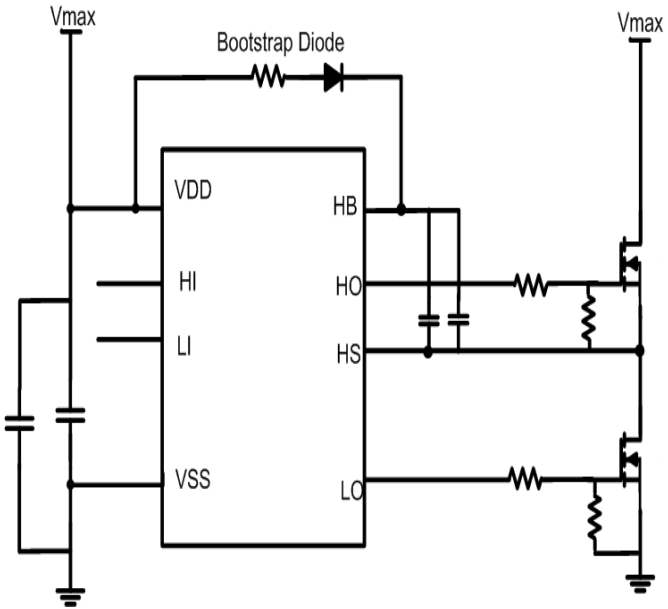
#1 VCC bias capacitor considerations

- Increase VCC bias capacitor
- Rule of Thumb: $C_{VCC} \geq 10 \times C_{boot}$
- Place the VCC bias capacitor very close to the VCC pin of the driver

Sizing VCC bypass capacitor

- ❑ $\Delta V_{HB} = V_{CC} - V_{DF} - V_{HBL}$
- ❑ $C_{BOOT} = Q_{Total} / \Delta V_{HB}$
- ❑ $C_{Bias} >> C_{Boot}$
- ❑ High freq. filter capacitor

What is wrong with HO waveform?



- Causes:
  - Low capacitance
  - Low R_{gs}
  - Low F_{sw}
  - Large D
- Consequences
  - ✕ Hot MOSFET
  - ✕ Output ripple

✕ HO drooping / Bootstrap leakage

#2 bootstrap capacitor considerations

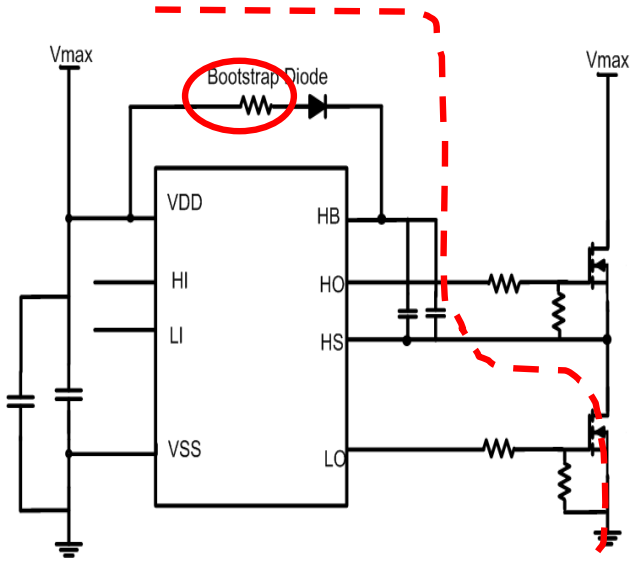
- Increase Cboot
- Increase Rgs
- Place the boot capacitor very close to the HB-HS pins of the driver

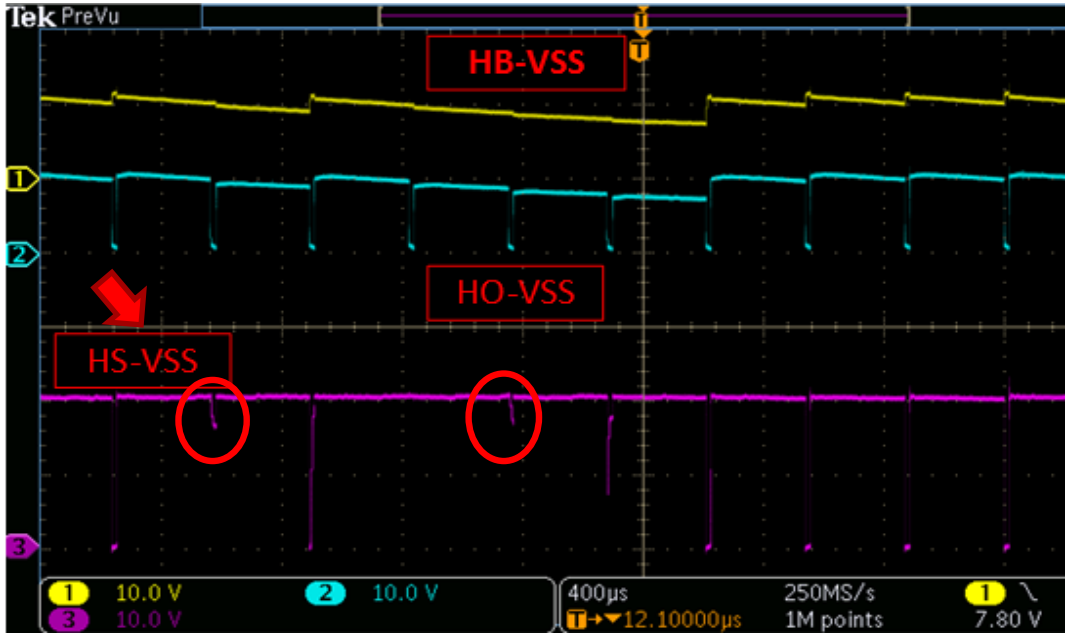
Sizing bootstrap capacitor

- $C_{Boot} = Q_{Total} / \Delta V_{HB}$
- $Q_{Total} = Q_G + (I_{HBS} \times D_{Max}/F_{SW}) + (I_{HB}/F_{sw})$

#2 What is wrong with switch node waveform?

Bias supply





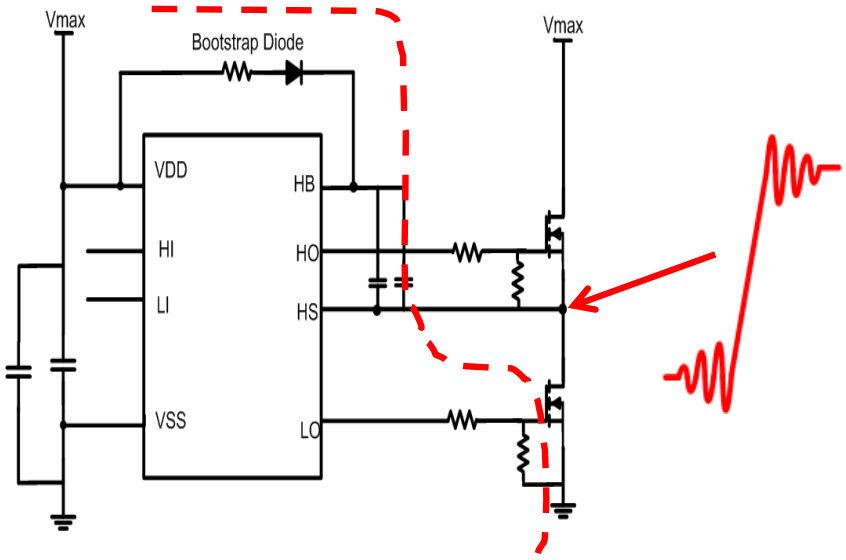
Design guidelines

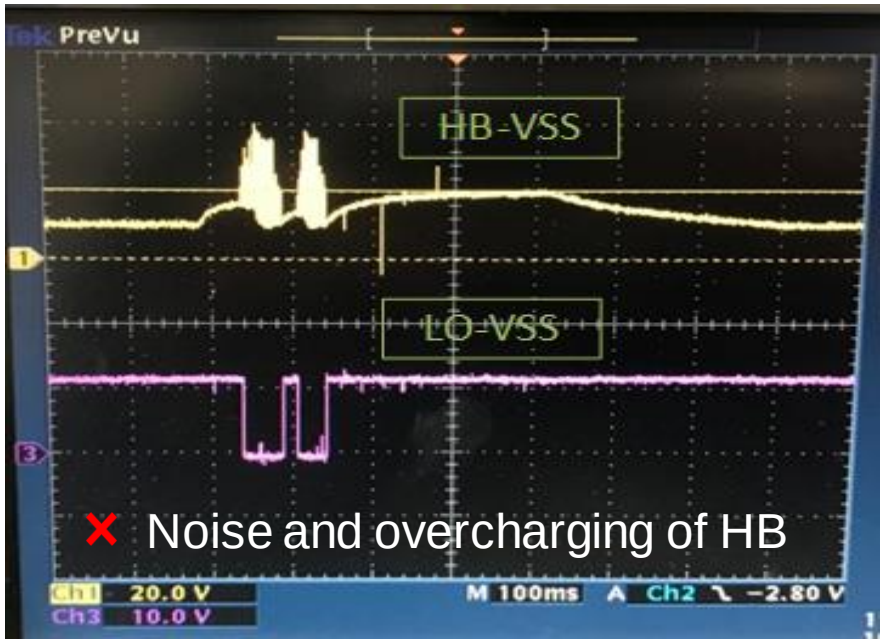
- **Reduce R_{Boot}**
- **Minimum top switch ON time**

✗ HS waveform – inconsistent HS signal

✗ Very short LO duty cycle – partially charged C_{Boot}

#3 Is this waveform normal?



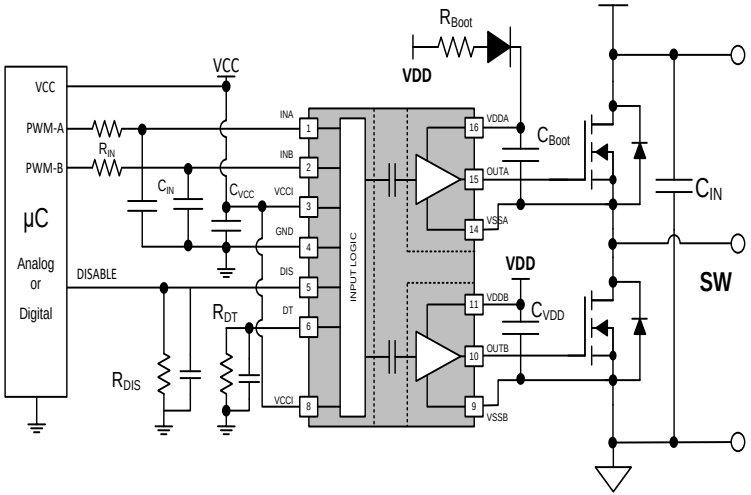


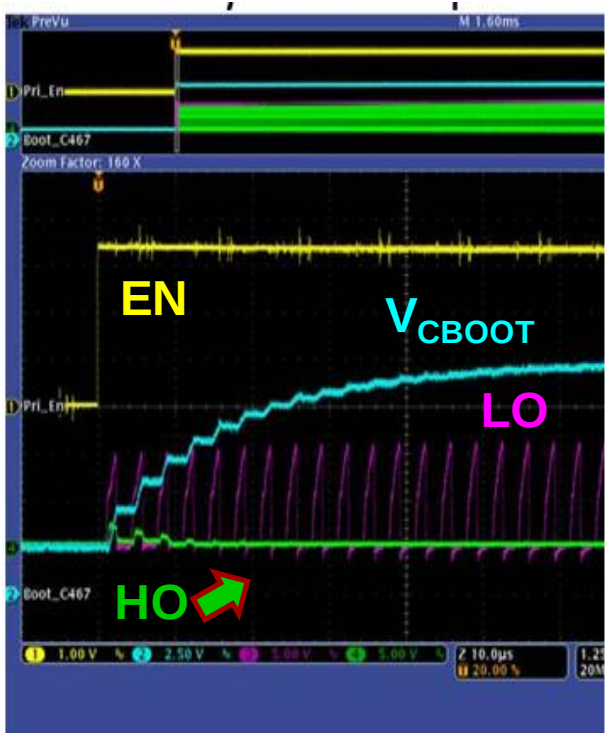
Design guidelines

- **Increase boot resistor**
- **Increase boot capacitor**

- ✗ HS neg. ringing → overcharging the boot cap
- ✗ Fast HS slew rate → noise and oscillation on HB

#4 Why is there NO gate driver output?





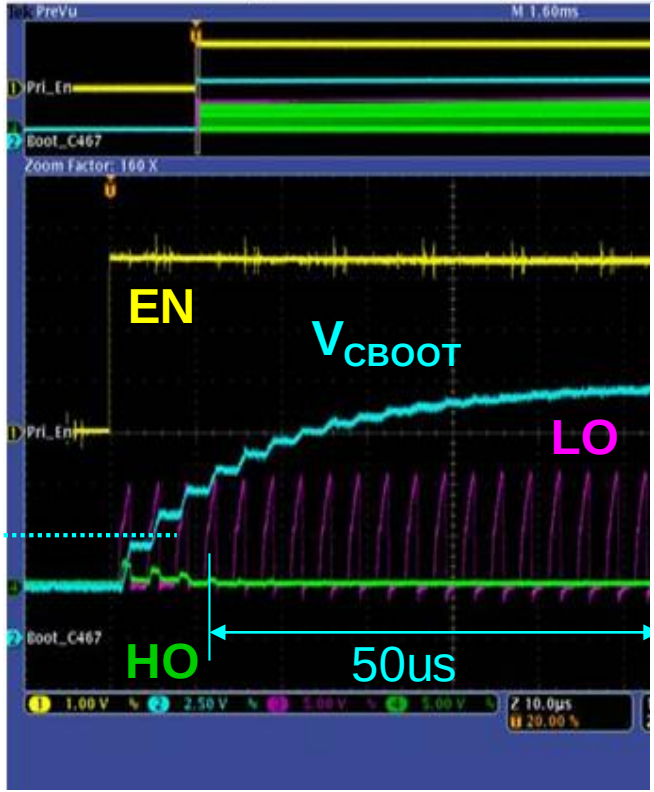
- High side boot supply is ready
- Driver IC is enabled
- PWM input HI&LI are ready
- The low side LO is good

#4 Why is there NO gate driver output?

- High side boot supply is ready
- Driver IC is enabled
- PWM input HI&LI are ready
- The low side LO is good

✖ There is NO high side output

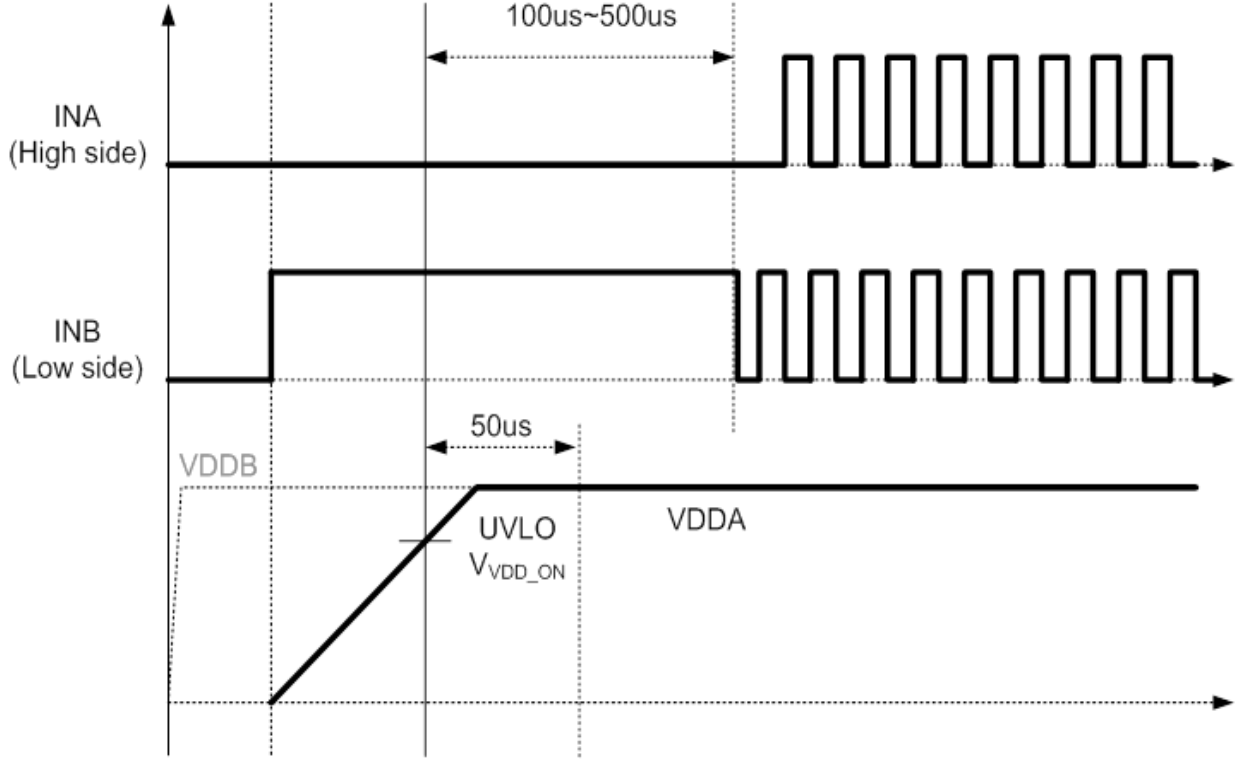
❑ **<u>UVLO delay</u>:** 5µs to 100µs depends on the driver



Bias supply

Design guidelines

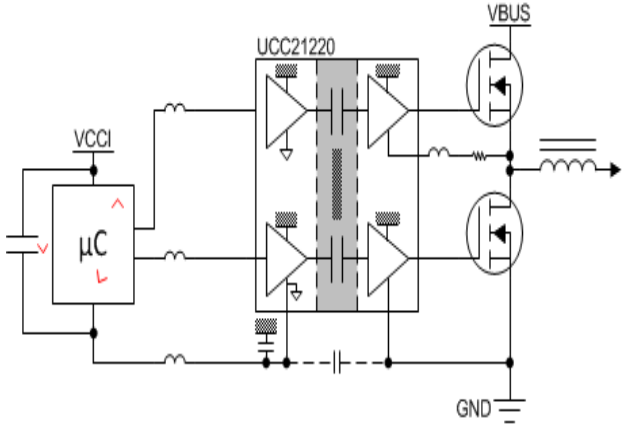
- Turn-on low side to pre-charge boot capacitor
- Synchronize HI and LI

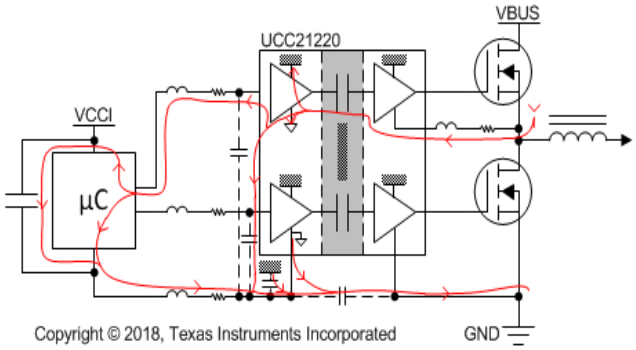


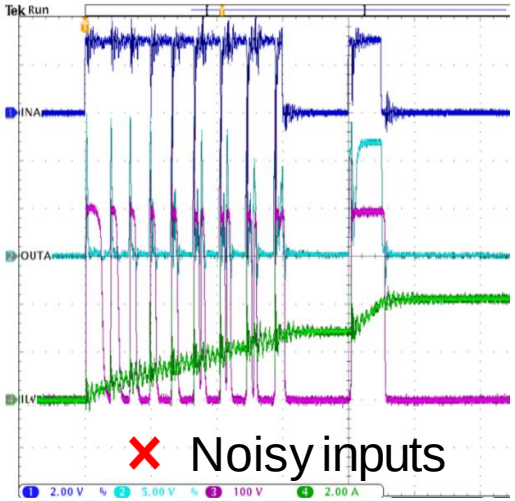
Synchronization LI and HI after bias supplies are both ready

#5 What is wrong with the waveform?

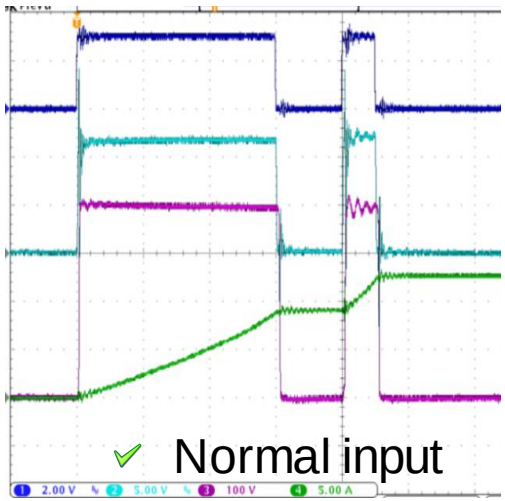
Pin w/ Hi-Z







✗ Noisy inputs



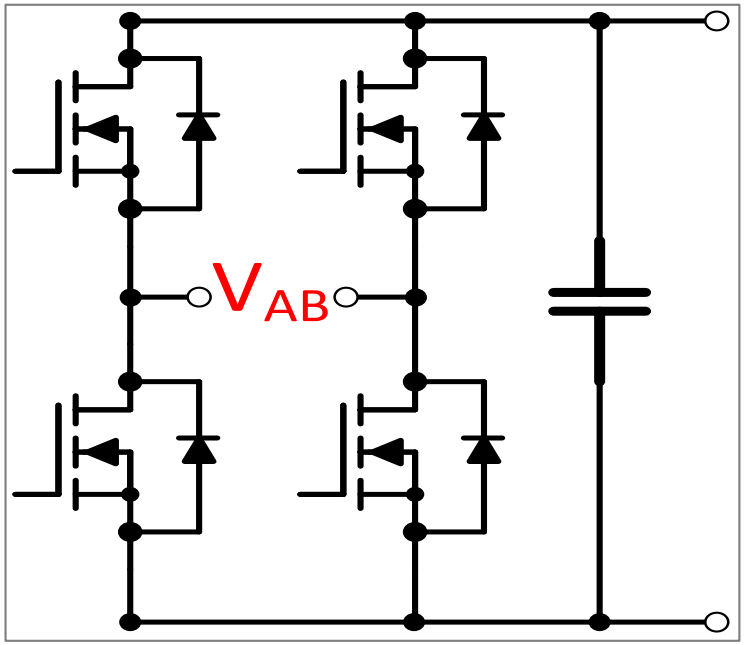
✓ Normal input

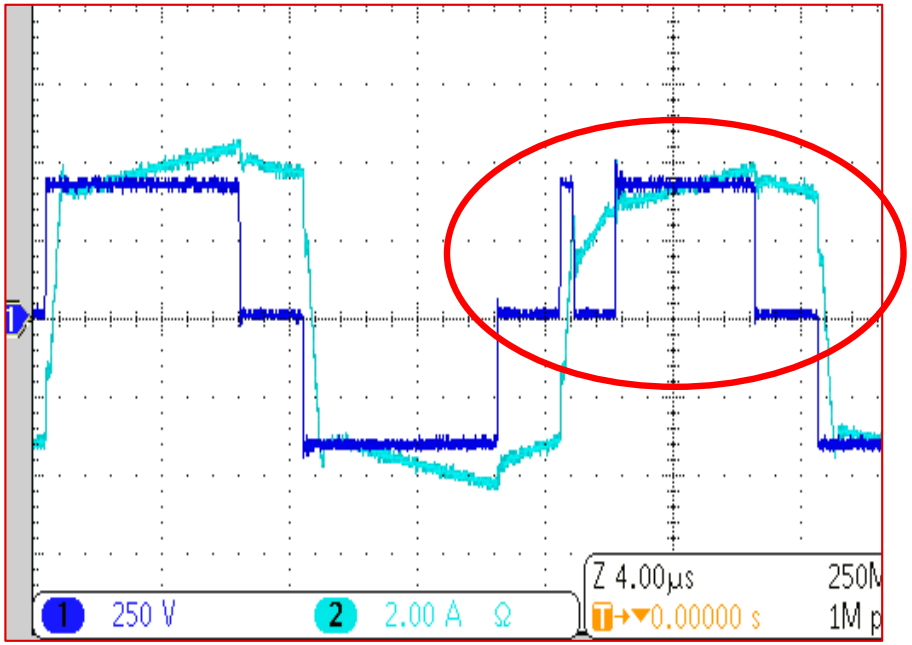
Design guidelines:

- Input filter to improve overall system performance
- Decrease loop inductance in PCB layout

#6 What causes glitches in PSFB at full load?

Pin w/ Hi-Z

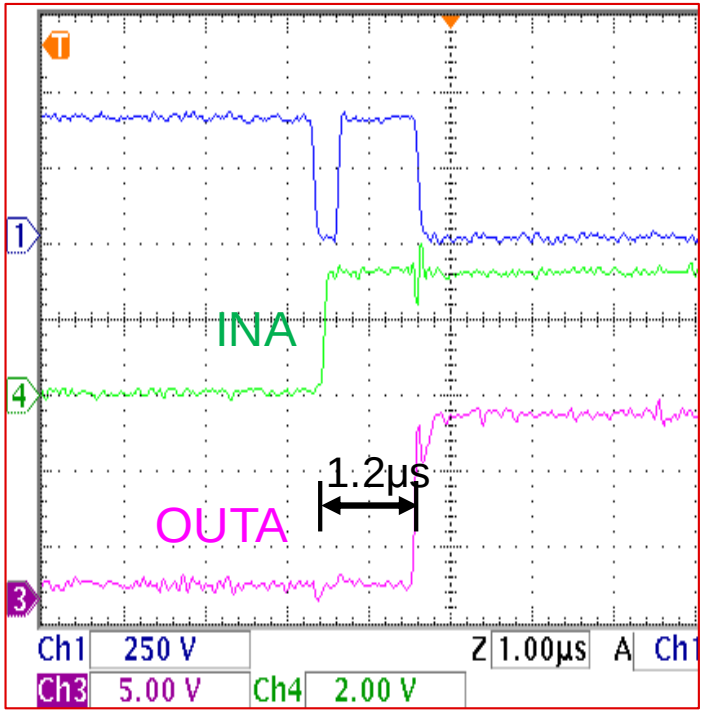


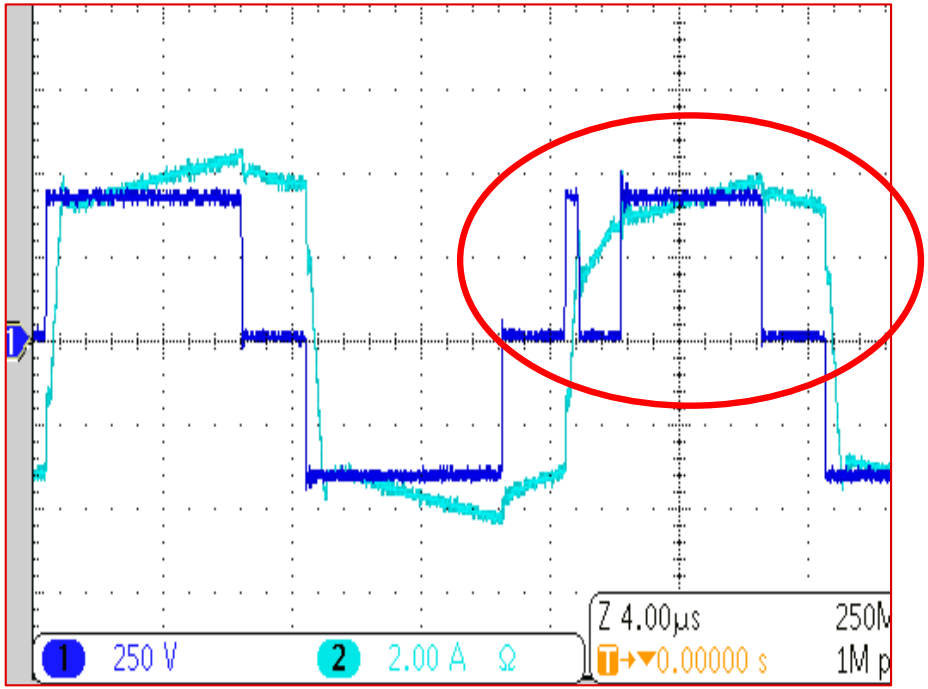


✖ Voltage waveform “VAB” has intermittent failure and glitches

#6 What causes glitches in PSFB at full load?

Pin w/ Hi-Z

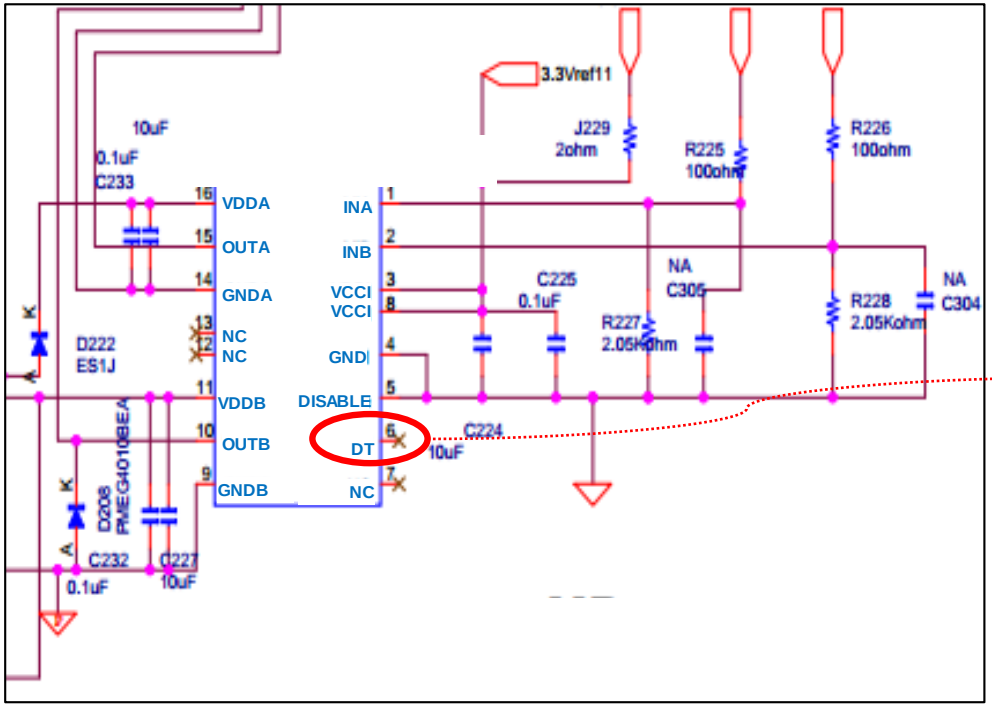




✖ Output A is being delayed by 1.2µs (which should be <50ns)

Root cause

Pin w/ Hi-Z



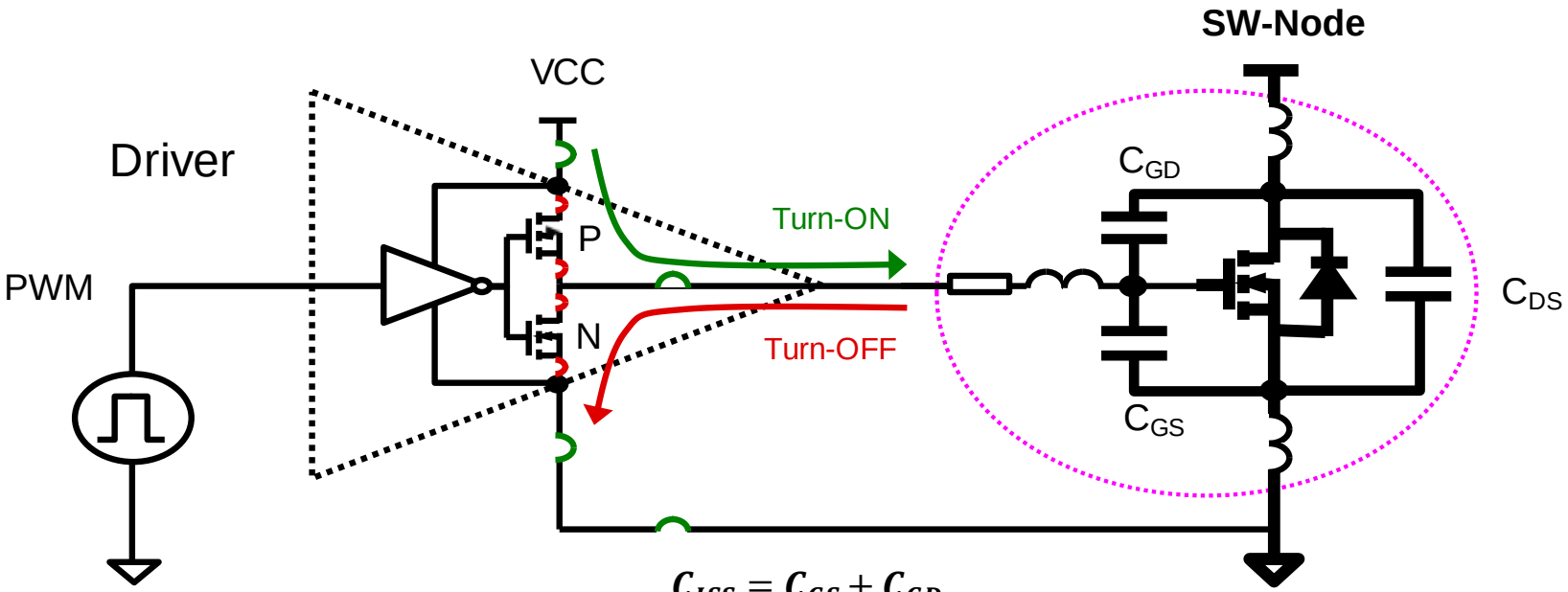
Design guidelines

- DT pin is left open and noise is coupled into the driver
- For dead time setting, bypass with ≥2.2nF close to DT pin

  $DT(\text{in ns}) = 10 \times RDT(\text{in k}\Omega)$
- For overlapping or no DT, tie DT pin to VCCI

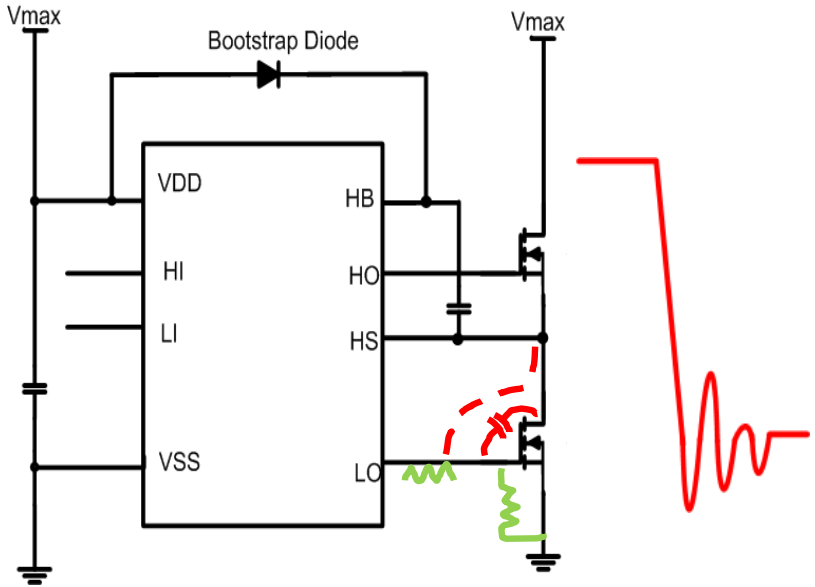
❑ **Do NOT leave functional pins open**

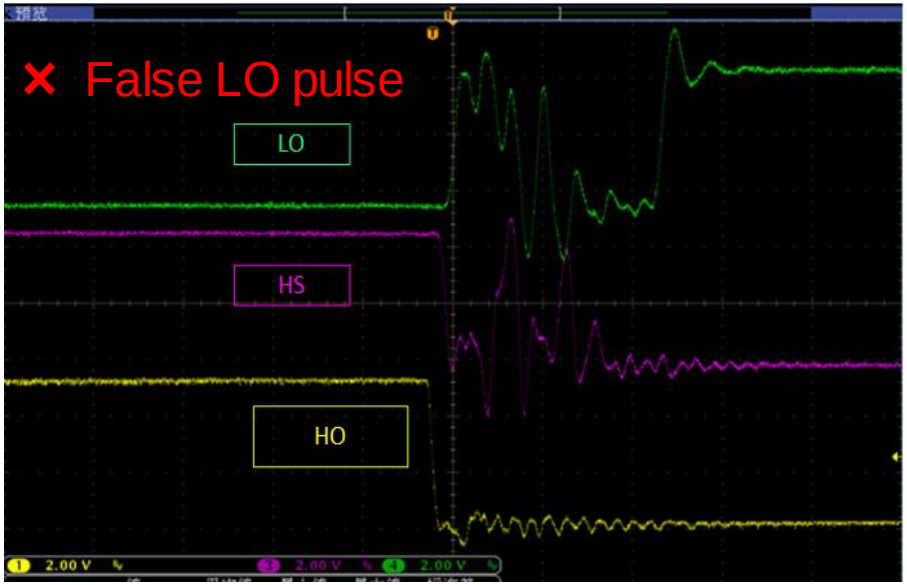
Parasitics in gate driver sub-system



$$C_{ISS} = C_{GS} + C_{GD}$$
$$C_{RSS} = C_{GD}$$
$$C_{OSS} = C_{GD} + C_{DS}$$

#7 What Is wrong when HO turns off?

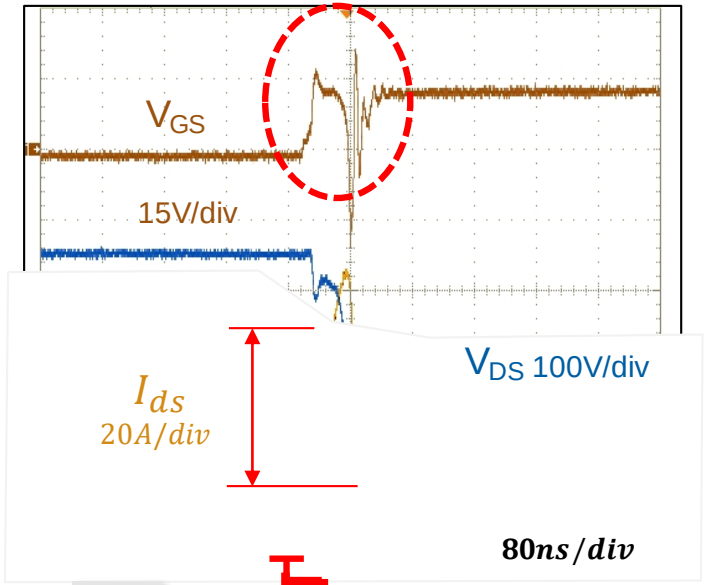


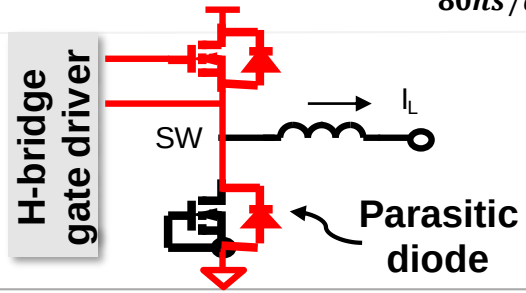


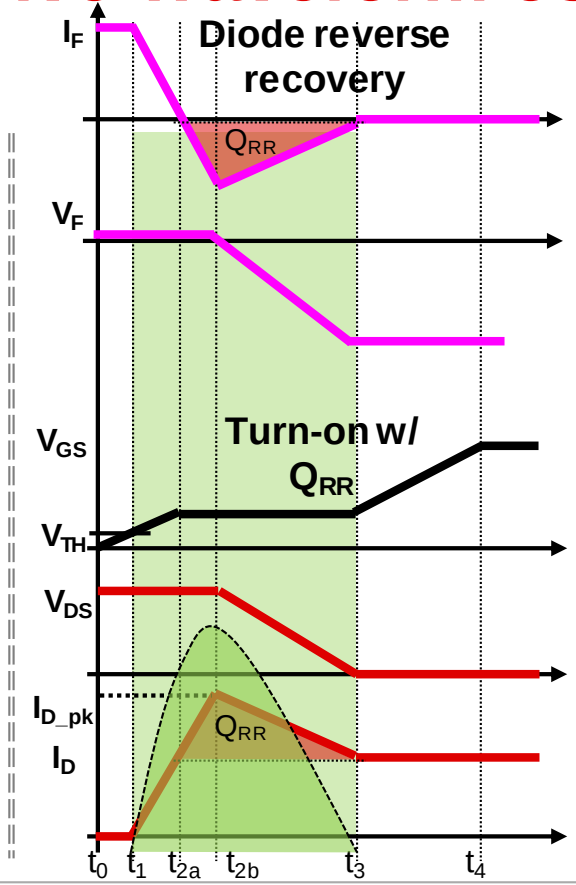
- **High voltage and IGBT applications**
- **Series gate and gate to source resistor**
- **Driver with Miller clamp**

- ✕ High dV/dt and dI/dt causes D-G capacitor to charge and develop voltage
- ✕ Voltage may be higher than $V_{gs(th)}$

#8 Why is the gate drive waveform oscillating?







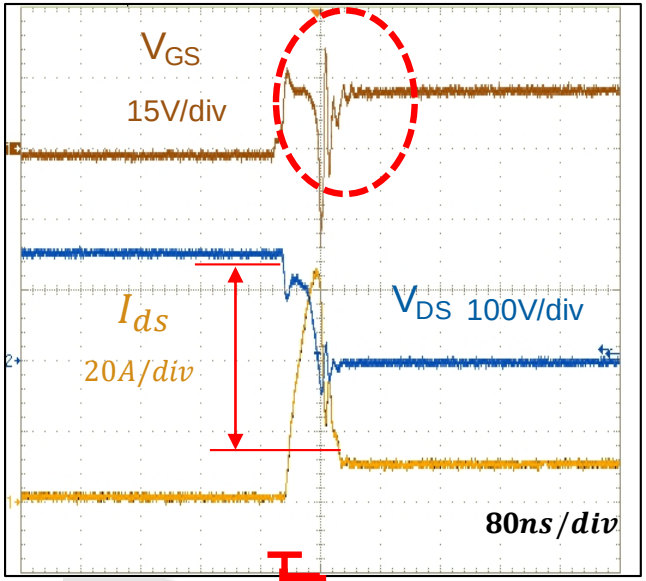
Parasitics

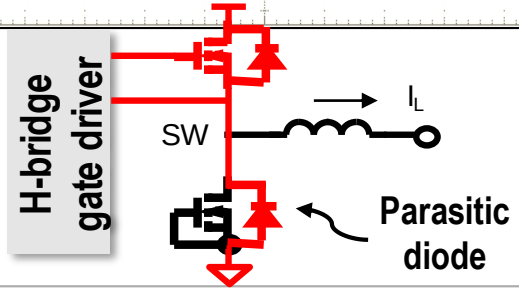
- ✖ Increase turn-on loss
- ✖ Higher di/dt, EMI
- ✖ Device overshoot
- ✖ Gate drive oscillation (over/under shoot)

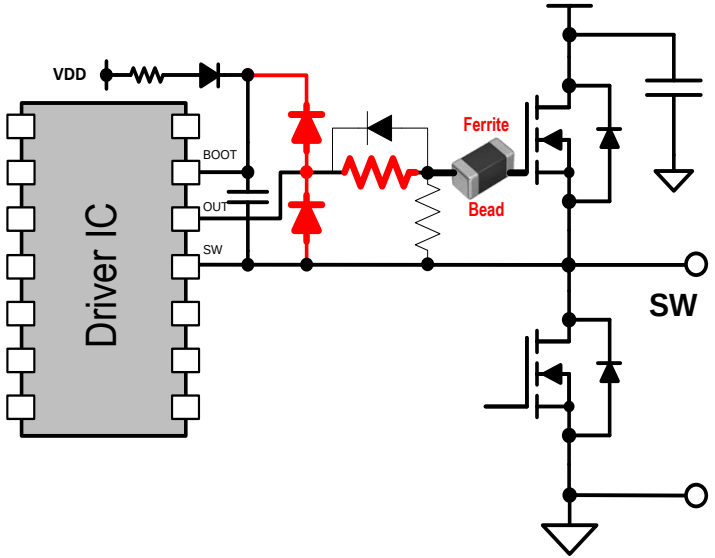
#8 Why is the gate drive waveform oscillating?

Parasitics

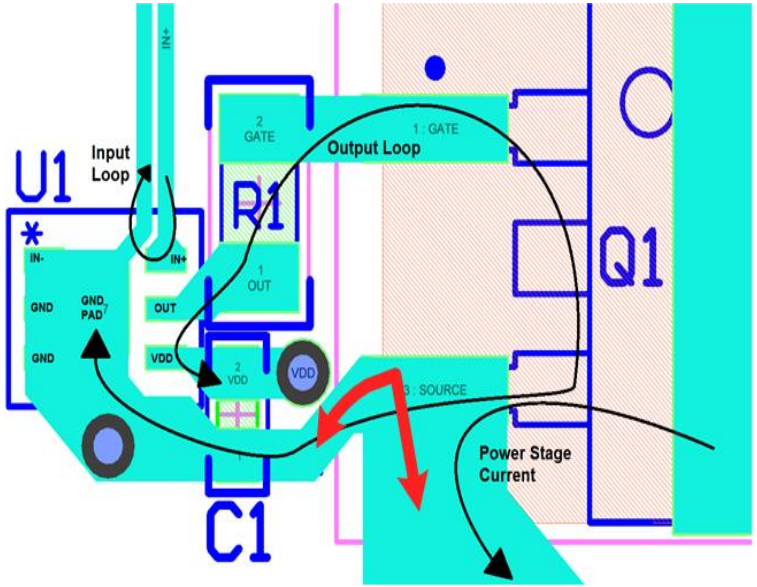
- Slow down body diode reverse recovery
- FET with robust and low Q_{RR} body diode
- Soft switching - ZVS

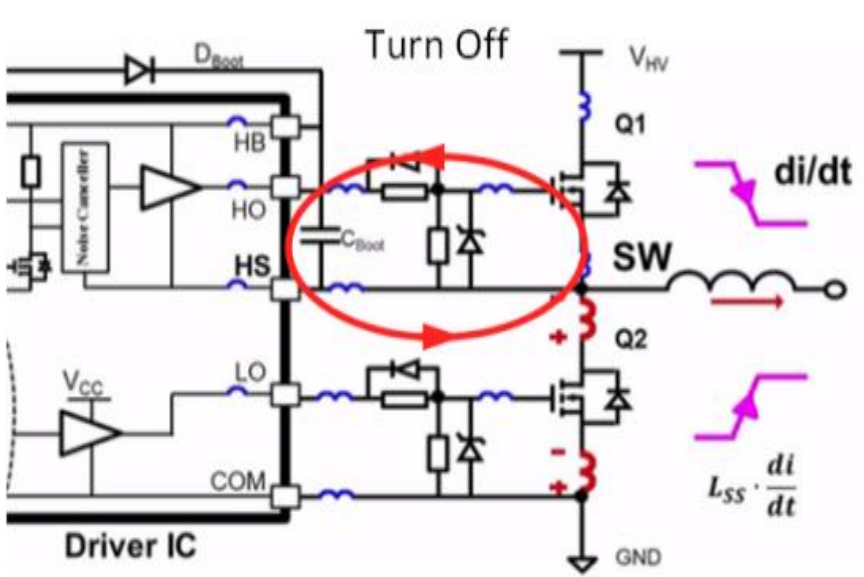






Minimize high current gate drive loops

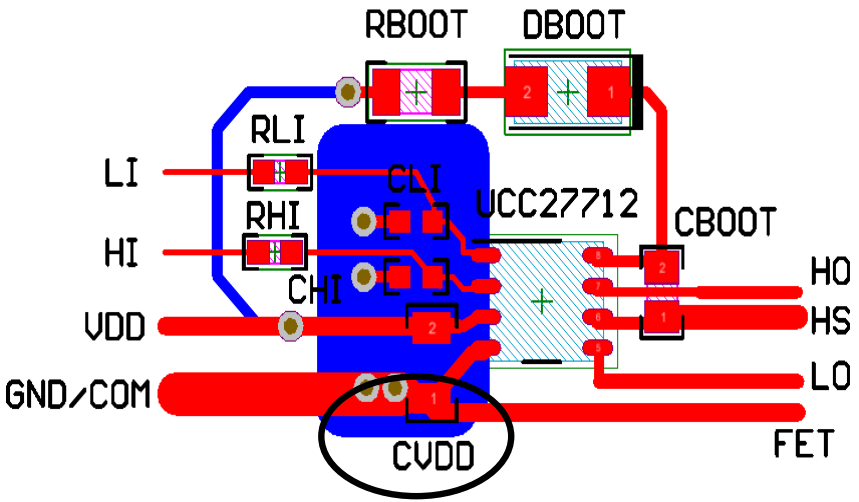




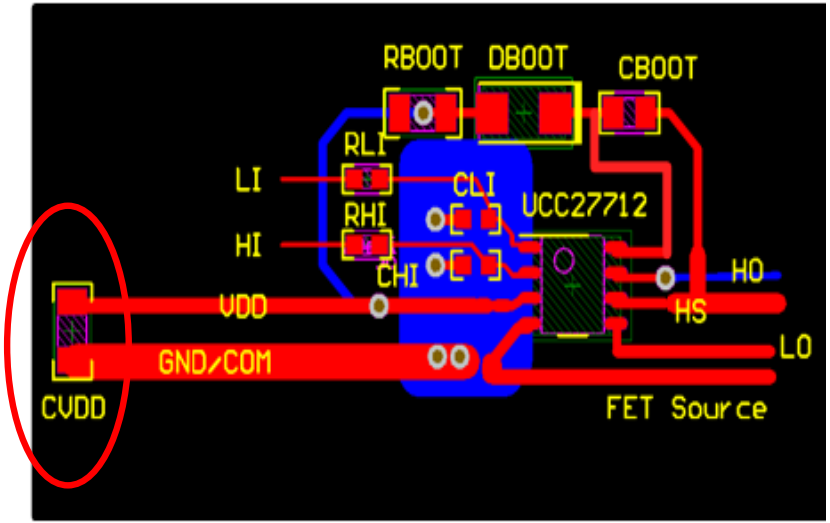
- Gate driver outputs carry high currents and therefore minimize the output loop
- If totem pole buffer is used, then place it as close to the power MOSFET as possible

Examples

GOOD



BAD



- Bypass capacitor needs to be as close to gate driver IC as possible
- V_{CC}, V_{DD}, input filter, DT, EN, DIS
- Value and package of the capacitor do matter

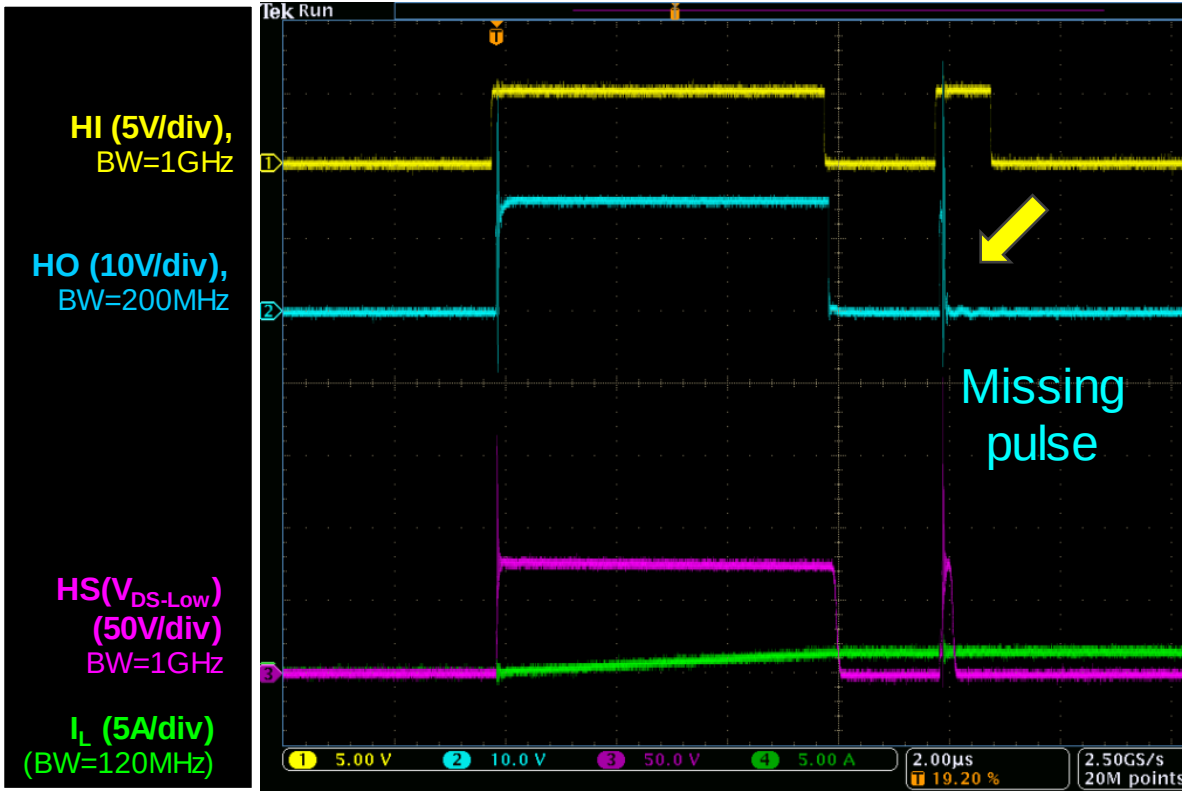
#9 What is wrong with my HO output?

dv/dt

- Case 1: output is shorter than input

✖ **HO 80ns glitches at HI=high**

- Double pulse on HI
- LI pulled down w/ 4.7kΩ



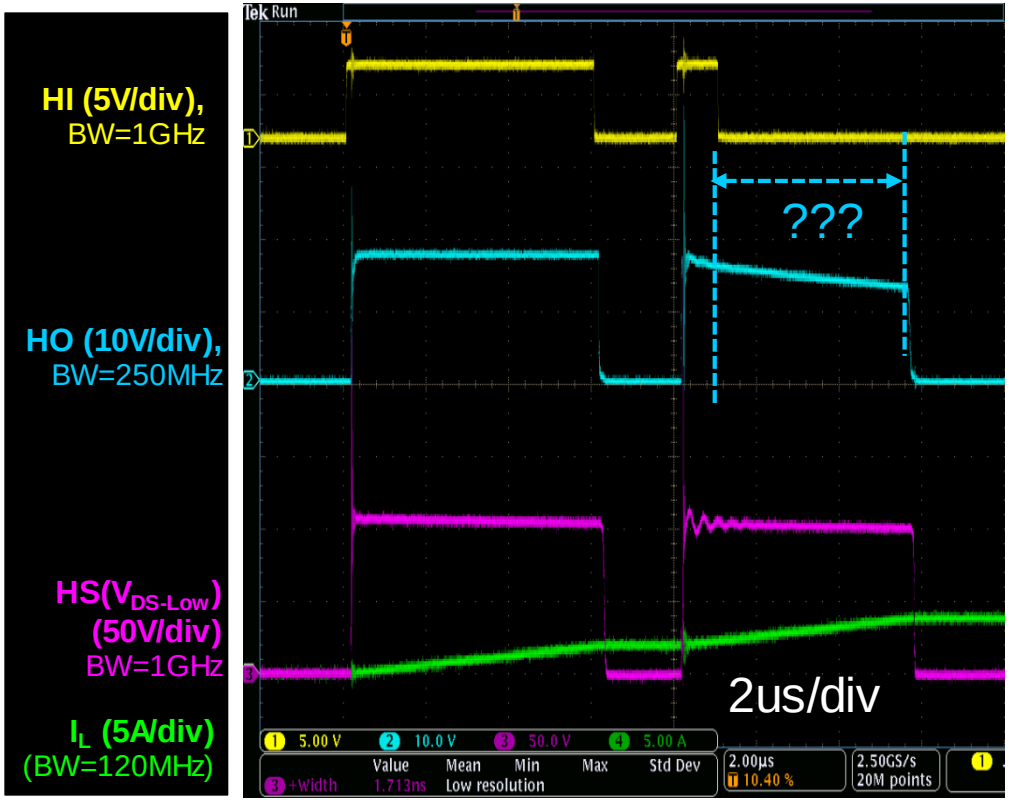
#9 What is wrong with my HO output?

dv/dt

- Case 2: output is longer than input

✖ **HO stretched for 4µs more**

- Double pulse on HI
- LI pulled down w/ 4.7kΩ

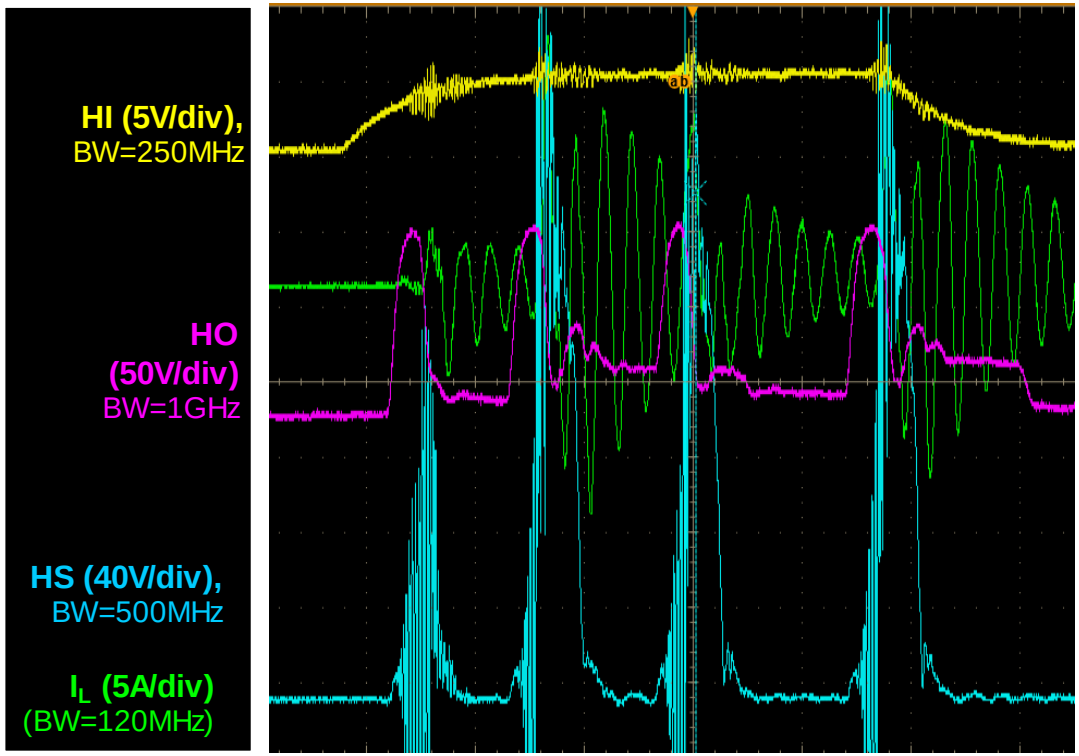


#9 What is wrong with my output?

- Case 3: output on and off intermittent while HI is ON

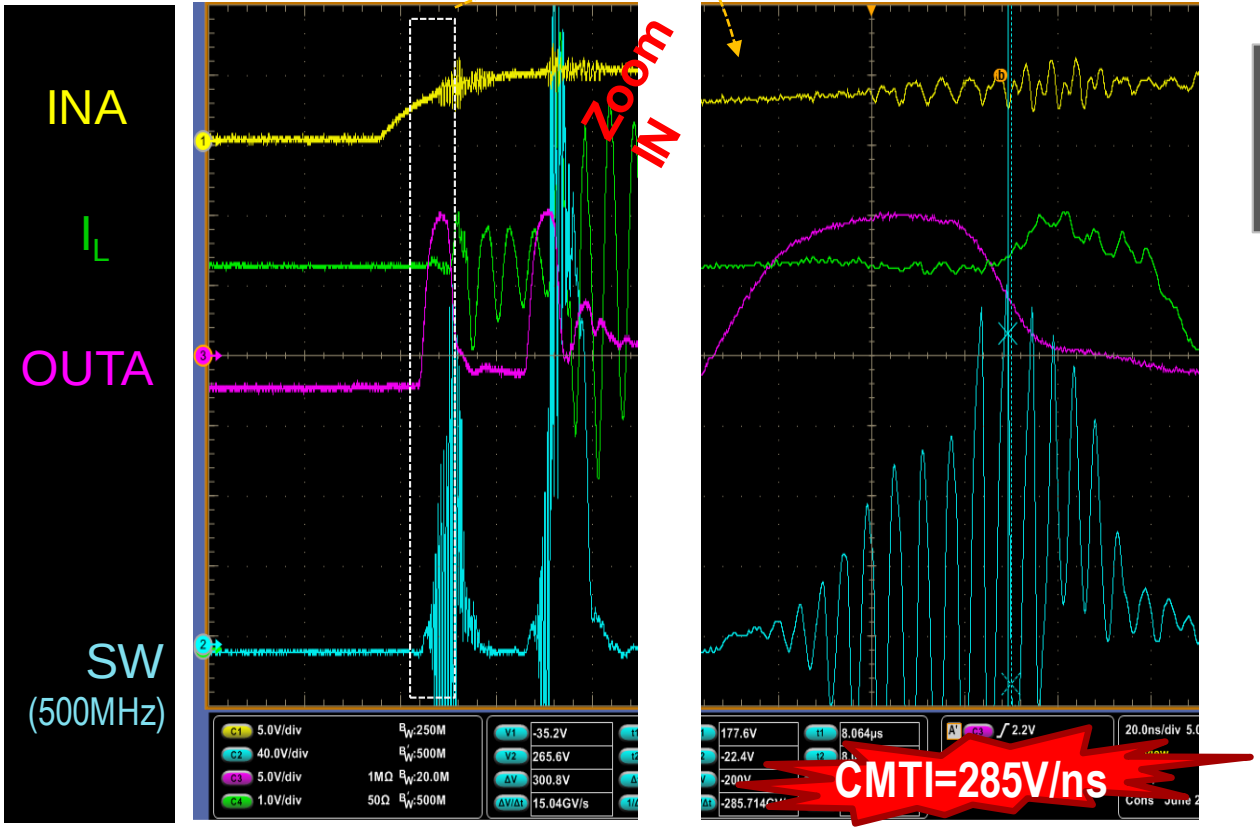
✖ **HO turns off intermittent**

- Double pulse on HI
- LI pulled down w/ 4.7kΩ

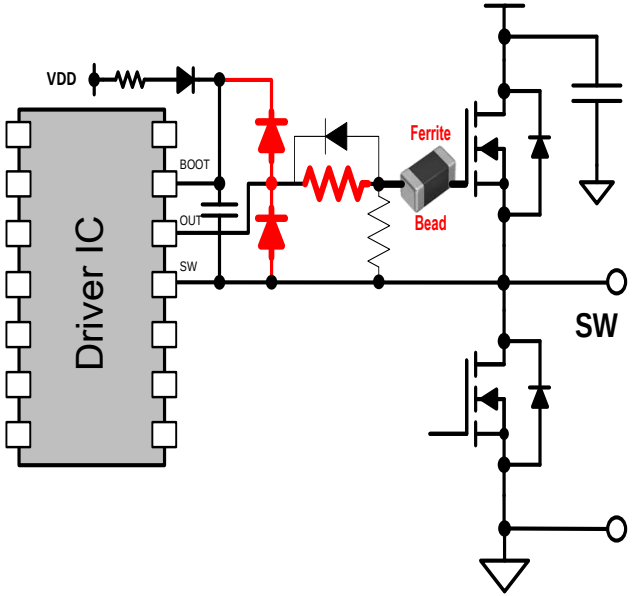


The switch node CMTI is >200V/ns

dv/dt

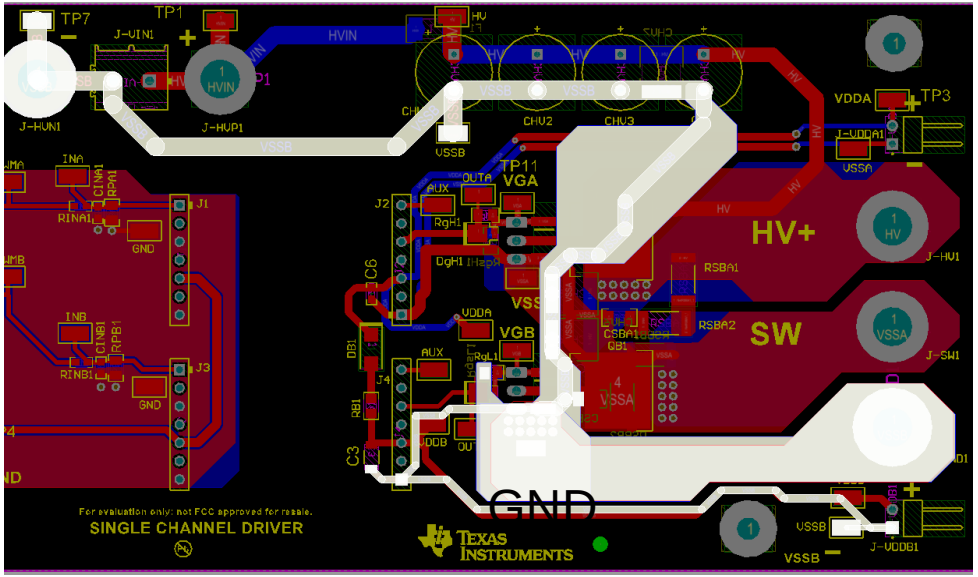


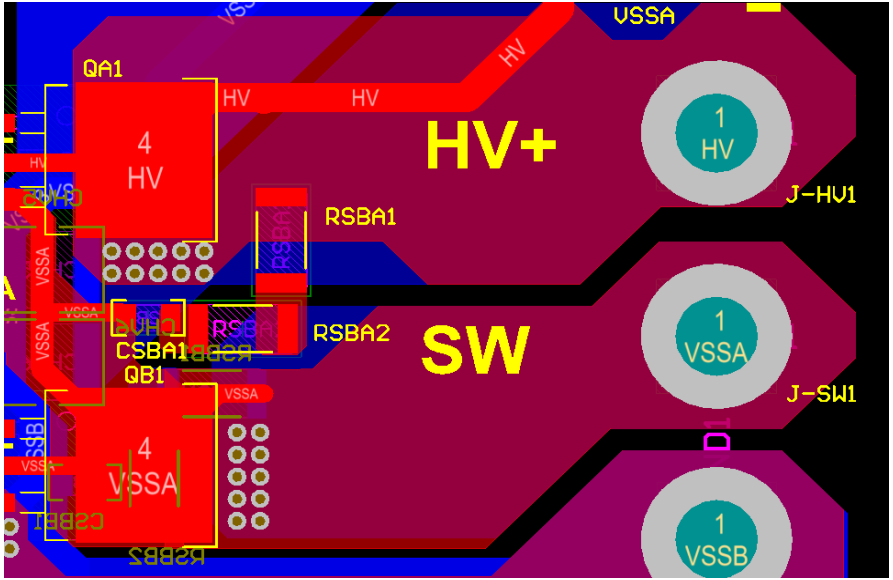
- Slow down reverse recovery
- FET w/ low Q_{RR} B-diode
- Soft switching - ZVS



Layout: ground plane and switch node (SW)

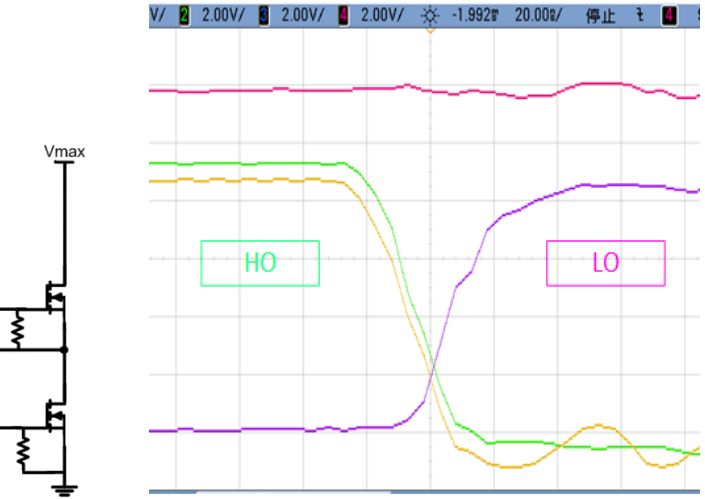
dv/dt



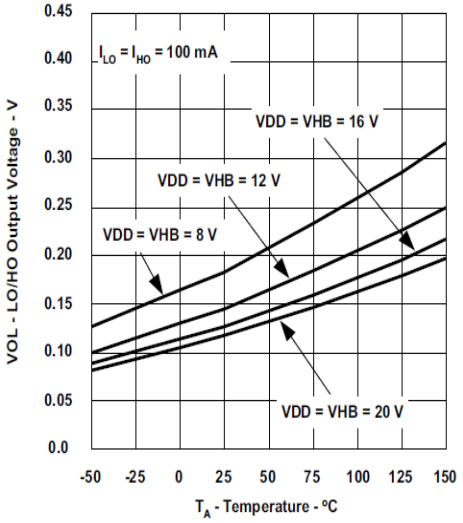


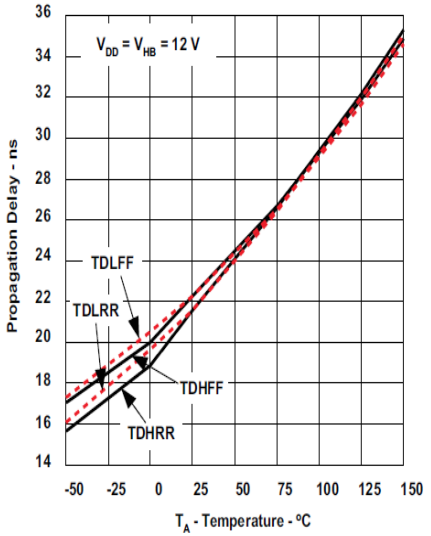
- Minimize or avoid overlapping switch node plane and ground plane
- Could create issues when switching frequencies are high
- As HS slew rates are high, overlap of ground plane and switch node plane might inject noise in other circuits on the board

#10 Would this waveform create any system problems?



Variance





- ✕ HO/LO might cross conduct
  - ✕ Shoot-through current
  - ✕ Excessive power dissipation
  - ✕ False overcurrent tripping

- Account for propagation delay and delay matching variation across temperature/voltage
- Account for drive strength variation across temperature/bias voltage

Summary

- Various issues encountered while designing switch-mode power supplies were discussed from the gate driver IC point of view and their resolutions were clearly identified
- Proper bypassing of the gate driver IC (as with many other ICs) is extremely critical to its performance
- When gate driver IC is used in half-bridge configuration, switch node slew rate plays an important role in the performance of the gate driver IC
- PCB layout plays important role in satisfactory performance of the gate driver IC and thus the whole system

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