Technical Reference Manual

TPS6521402 Technical Reference Manual

ABSTRACT

This Technical Reference Manual (TRM) can be used as a reference for the default register bits after the NVM download. The end user is responsible for validating the NVM settings for proper system use including any safety impact. This TRM does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the device data sheet at ti.com.

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Trademarks

1 Introduction

The TPS6521402 PMIC is a cost and space optimized solution that has flexible mapping to support the power requirements from different processors and SoCs. The PMIC includes 3 Buck regulators and 2 Low Drop-out Regulators (LDOs) with I2C, GPIOs, and configurable multi-function pins. The device also contains One-Time Programmable (OTP) Non-Volatile Memory (NVM) that is loaded to the device registers when entering the INITIALIZE state. This document describes the default configuration programmed on the TPS6521402.

Note

The NVM configuration described in this document is ideal for the application described below but can also be used to power other processors or SoCs with equivalent power requirements.

- Processor: AM62L
- CORE voltage: 0.75V
- Memory: LPDDR4 or DDR4
- Input Supply (VSYS, PVIN_Bx): 3.3V or 5V

2 PDN and Sequence Diagrams

This section details how the TPS6521402 power resources and digital signals are connected to the processor and other peripheral components.

2.1 TPS6521402 Power Sequence and Example Block Diagram

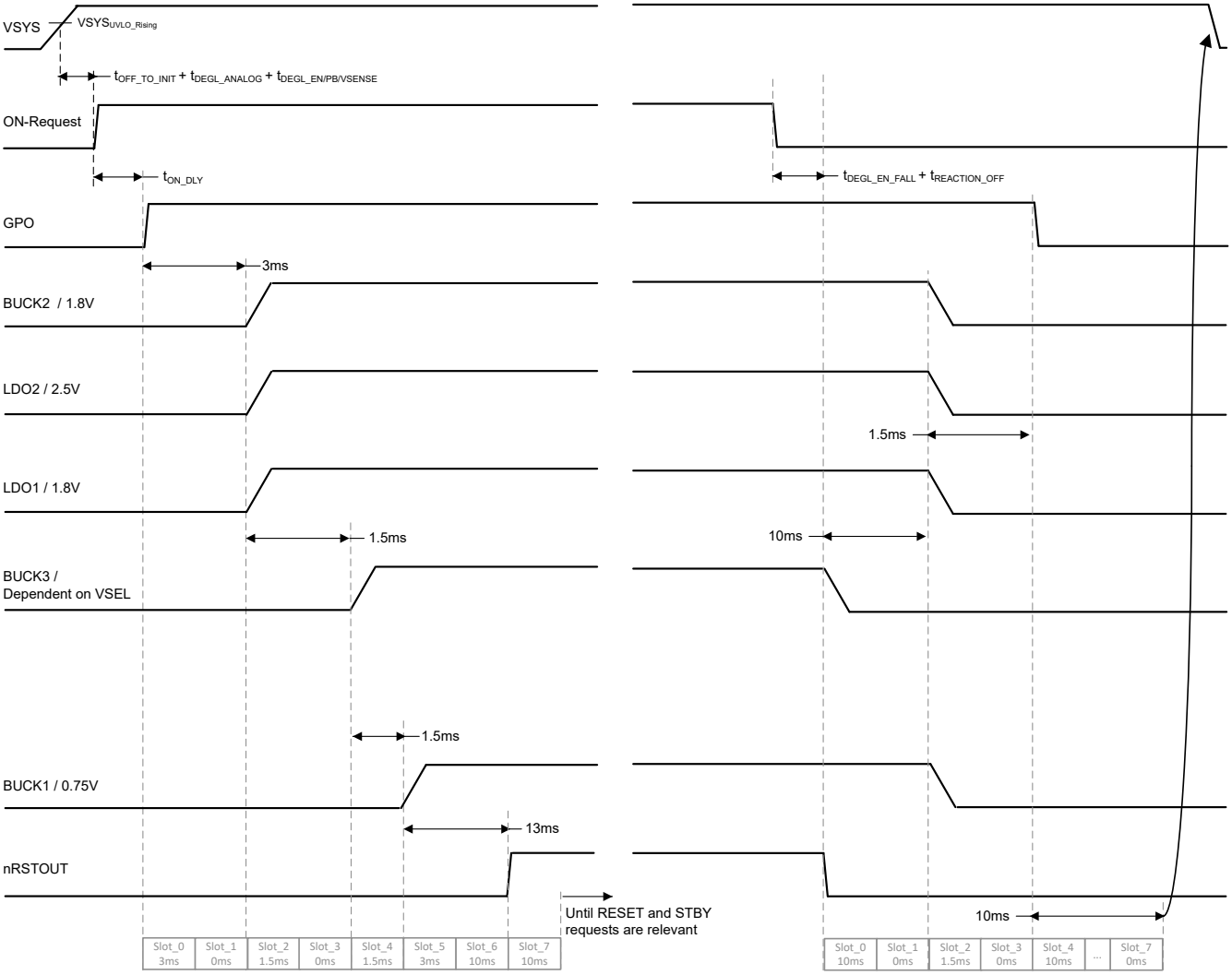

Figure 2-1. TPS6521402 Power Sequence

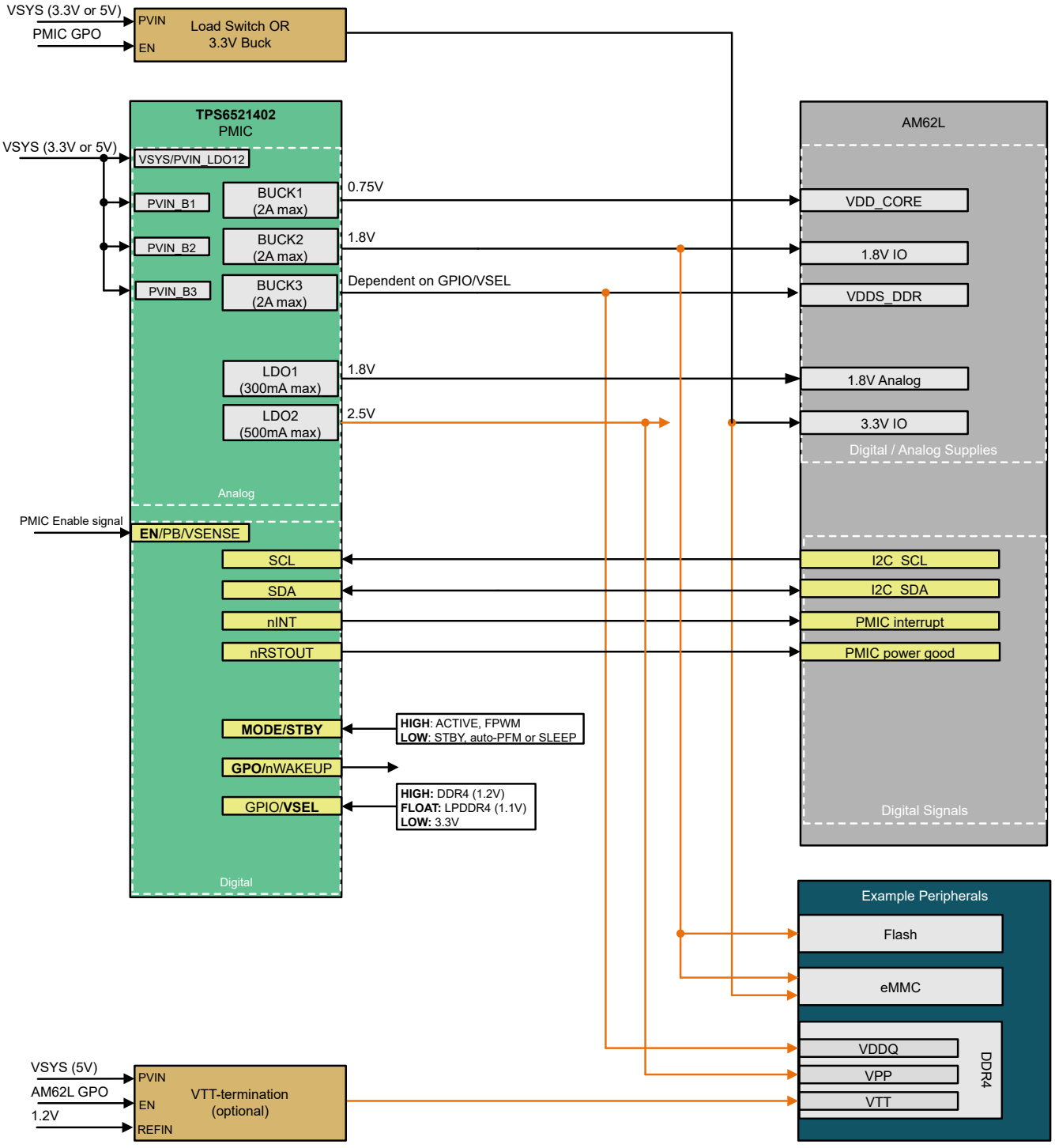

Figure 2-2. TPS6521402 Example Block Diagram

3 NVM Device Settings

The following sections describe the default configuration on the NVM-backed registers. During the power-down-sequence, non-NVM-backed bits are reset, with the exception of unmasked interrupt bits and DISCHARGE_EN bits.

3.1 Device ID

This section lists all the register settings that identify the supported temperature and the NVM ID with the corresponding revision that represents a list of default register settings.

Table 3-1. Device ID

Register Address	Field Name	Value	Description
0x00	NVM_REVISION (Bits: 7-5)	0x4	Identification code for the NVM revision
0x00	TI_DEVICE_ID (Bits: 4-0)	0x04	Device specific ID code.
0x01	TI_NVM_ID (Bits: 7-0)	0x02	Identification code for the NVM ID
0x26	I2C_ADDRESS (Bits: 6-0)	0x30	I2C address

3.2 Enable Settings

This section describes the PMIC rails that are enabled in Active and Standby state. Any rail that is disabled by default has the option to be enabled through I2C once the device is in Active state and I2C communication is available. The transition between Active and Standby state can be triggered by hardware (when MODE/STBY pin is configured as STBY) or by software (register field: STBY_I2C_CTRL).

Table 3-2. ACTIVE state

PMIC Rail	Register Address	Field Name	Value	Description
BUCK1	0x02	BUCK1_EN	0x1	Enabled
BUCK2	0x02	BUCK2_EN	0x1	Enabled
BUCK3	0x02	BUCK3_EN	0x1	Enabled
LDO1	0x02	LDO1_EN	0x1	Enabled
LDO2	0x02	LDO2_EN	0x1	Enabled
GPO	0x1E	GPO_EN	0x1	GPO enabled. The output state is Hi-Z.
GPIO	0x1E	GPIO_EN	0x0	GPIO not enabled. The output state is low.

Table 3-3. STANDBY (STBY) state

PMIC Rail	Register Address	Field Name	Value	Description
BUCK1	0x21	BUCK1_STBY_EN	0x0	Not enabled in STBY Mode
BUCK2	0x21	BUCK2_STBY_EN	0x1	Enabled in STBY Mode
BUCK3	0x21	BUCK3_STBY_EN	0x1	Enabled in STBY Mode
LDO1	0x21	LDO1_STBY_EN	0x0	Not enabled in STBY Mode
LDO2	0x21	LDO2_STBY_EN	0x1	Enabled in STBY Mode
GPO	0x22	GPO_STBY_EN	0x1	Enabled in STBY Mode
GPIO	0x22	GPIO_STBY_EN	0x0	Not enabled in STBY Mode
nRSTOUT	0x22	nRSTOUT_STBY_CONFIG	0x0	nRSTOUT asserted in STBY Mode

3.3 Regulator Voltage Settings

This section describes how each of the PMIC power resources are configured.

Table 3-4. Buck Regulator Settings

PMIC Rail	Register Address	Field Name	Value	Description
BUCK1	0x0A	BUCK1_VSET (Output Voltage)	0x6	0.750V
	0x0A	BUCK1_UV_THR_SEL (UV threshold)	0x0	-5% UV detection
	0x0A	BUCK1_BW_SEL (Bandwidth)	0x0	low bandwidth
	0x1D	BUCK1_DVS_STBY	0x0	No DVS transition in STBY
	0x1D	BUCK1_VSET_STBY	0x00	0ms
BUCK2	0x09	BUCK2_VSET (Output Voltage)	0x24	1.800V
	0x09	BUCK2_UV_THR_SEL (UV threshold)	0x0	-5% UV detection
	0x09	BUCK2_BW_SEL (Bandwidth)	0x0	low bandwidth
	0x1C	BUCK2_DVS_STBY	0x0	No DVS transition in STBY
	0x1C	BUCK2_VSET_STBY	0x00	0ms
BUCK3	0x08	BUCK3_VSET (Output Voltage)	0x33	3.300V
	0x08	BUCK3_UV_THR_SEL (UV threshold)	0x0	-5% UV detection
	0x08	BUCK3_BW_SEL (Bandwidth)	0x0	low bandwidth
	0x19	BUCK3_DVS_STBY	0x0	No DVS transition in STBY
	0x19	BUCK3_VSET_STBY	0x00	0ms

Table 3-5. LDO Regulator Settings

PMIC Rail	Register Address	Field Name	Value	Description
LDO1	0x05	LDO1_VSET	0x1A	1.800V
	0x05	LDO1_LSW_CONFIG	0x0	LDO Mode
	0x1E	LDO1_UV_THR	0x0	-5% UV detection
	0x04	LDO1_DVS_STBY	0x0	No DVS transition in STBY
	0x04	LDO1_VSET_STBY	0x1A	1.800V
LDO2	0x06	LDO2_VSET	0x28	2.500V
	0x06	LDO2_LSW_CONFIG	0x0	LDO Mode
	0x1E	LDO2_UV_THR	0x0	-5% UV detection
	0x07	LDO2_DVS_STBY	0x0	No DVS transition in STBY
	0x07	LDO2_VSET_STBY	0x28	2.500V

Note

- If a LDO is configured in LSW-mode, UV-detection is not supported.
- If LDO is configured as load-switch (LSW_mode), the desired voltage does not need to be configured in the LDOx_VOUT register.
- In LSW-mode, the LDO acts as a switch, where VOUT is VIN minus the drop over the FET-resistance.

3.4 Sequence Settings

This section breaks down the power sequence settings for the device including the power-up/power-down slot assignment and duration. There may be slots in which no rail or GPIO is assigned to ramp. These "empty" slots can be used to add additional time and increase a slot duration.

3.4.1 Power-Up Sequence

Table 3-6. Power-Up Sequence - Slot Assignment

PMIC Rail	Register Address	Field Name	Value	Description
BUCK1	0x11	BUCK1_SEQUENCE_ON_SLOT	0x5	slot 5
BUCK2	0x10	BUCK2_SEQUENCE_ON_SLOT	0x2	slot 2
BUCK3	0x0F	BUCK3_SEQUENCE_ON_SLOT	0x4	slot 4
LDO1	0x0C	LDO1_SEQUENCE_ON_SLOT	0x2	slot 2
LDO2	0x0D	LDO2_SEQUENCE_ON_SLOT	0x2	slot 2
GPO	0x15	GPO_SEQUENCE_ON_SLOT	0x0	slot 0
GPIO	0x13	GPIO_SEQUENCE_ON_SLOT	0x0	slot 0
nRSTOUT	0x12	nRST_SEQUENCE_ON_SLOT	0x7	slot 7

Note

PMIC rails are turned ON during the power-up sequence if the corresponding EN bit on section "Enable Setting" is set to 0x01.

Table 3-7. Power-Up Sequence - Slot Duration

	Register Address	Field Name	Value	Description
SLOT0	0x16	POWER_UP_SLOT_0_DURATION	0x2	3ms
SLOT1	0x16	POWER_UP_SLOT_1_DURATION	0x0	0ms
SLOT2	0x16	POWER_UP_SLOT_2_DURATION	0x1	1.5ms
SLOT3	0x16	POWER_UP_SLOT_3_DURATION	0x0	0ms
SLOT4	0x17	POWER_UP_SLOT_4_DURATION	0x1	1.5ms
SLOT5	0x17	POWER_UP_SLOT_5_DURATION	0x2	3ms
SLOT6	0x17	POWER_UP_SLOT_6_DURATION	0x3	10ms
SLOT7	0x17	POWER_UP_SLOT_7_DURATION	0x3	10ms

3.4.2 Power-Down Sequence

Table 3-8. Power-Down Sequence - Slot Assignment

	Register Address	Field Name	Value	Description
BUCK1	0x11	BUCK1_SEQUENCE_OFF_SLOT	0x2	slot 2
BUCK2	0x10	BUCK2_SEQUENCE_OFF_SLOT	0x2	slot 2
BUCK3	0x0F	BUCK3_SEQUENCE_OFF_SLOT	0x0	slot 0
LDO1	0x0C	LDO1_SEQUENCE_OFF_SLOT	0x2	slot 2
LDO2	0x0D	LDO2_SEQUENCE_OFF_SLOT	0x2	slot 2
GPO	0x15	GPO_SEQUENCE_OFF_SLOT	0x4	slot 4
GPIO	0x13	GPIO_SEQUENCE_OFF_SLOT	0x0	slot 0
nRSTOUT	0x12	nRST_SEQUENCE_OFF_SLOT	0x0	slot 0

Table 3-9. Power-Down Sequence - Slot Duration

	Register Address	Field Name	Value	Description
SLOT0	0x1A	POWER_DOWN_SLOT_0_DURATION	0x3	10ms
SLOT1	0x1A	POWER_DOWN_SLOT_1_DURATION	0x0	0ms
SLOT2	0x1A	POWER_DOWN_SLOT_2_DURATION	0x1	1.5ms
SLOT3	0x1A	POWER_DOWN_SLOT_3_DURATION	0x0	0ms

Table 3-9. Power-Down Sequence - Slot Duration (continued)

	Register Address	Field Name	Value	Description
SLOT4	0x1B	POWER_DOWN_SLOT_4_DURATION	0x3	10ms
SLOT5	0x1B	POWER_DOWN_SLOT_5_DURATION	0x0	0ms
SLOT6	0x1B	POWER_DOWN_SLOT_6_DURATION	0x0	0ms
SLOT7	0x1B	POWER_DOWN_SLOT_7_DURATION	0x0	0ms

3.5 EN / PB / VSENSE Settings

The EN/PB/VSENSE pin is used to enable or disable the PMIC. This pin can be configured in one of three ways: EN, PB or VSENSE. The table below shows the default configuration for this pin. Please note, if the FSD (First supply detection) feature is enabled, the device goes from "No Power" to "Active" state, executing the power-up sequence as soon as the voltage on VSYS is above the POR threshold. In this scenario, the EN/PB/VSENSE pin is ignored ONLY during the first power-up.

Table 3-10. EN / PB / VSENSE Settings

	Register Address	Field Name	Value	Description
Pin Config	0x20	EN_PB_VSENSE_CONFIG	0x1	Device Enable Configuration
ON Deglitch	0x20	EN_PB_VSENSE_DEGL	0x0	short (typ: 120us for EN/VSENSE and 200ms for PB)
First Supply Detection	0x20	PU_ON_FSD	0x0	First Supply Detection (FSD) Not enabled.

Note

The deglitch configured on register field "EN_PB_VSENSE_DEGL" is for the ON request. The deglitch for the OFF request is not configurable. The parameters that are not configurable can be found in the Specifications section of the device data sheet.

3.6 Multi-Function Pin Settings

The TPS6521402 has three multi-function pins: GPIO/VSEL, MODE/STBY, and GPO/nWAKEUP. This section describes how each of the multi-function pins are configured.

Table 3-11. Multi-Function Pin Settings

Pin Name	Setting	Register Address	Field Name	Value	Description
GPIO / VSEL	Function selection	0x1F	GPIO_VSEL_CONFIG	0x1	Configured as VSEL
	I/O selection	0x1F	GPIO_CONFIG	0x0	Configured as an input (only applicable if GPIO_VSEL_CONFIG=0x0)
	Pin polarity	0x13	GPIO_SEQUENCE_POLARITY	0x0	LOW - off / HIGH - on (only applicable if GPIO_VSEL_CONFIG=0x0 and GPIO_CONFIG=0x1)
	Rail selection	0x1F	VSEL_RAIL	0x1	BUCK3 (only applicable if GPIO_VSEL_CONFIG=0x1)
MODE / STBY	Function selection	0x20	MODE_STBY_CONFIG	0x2	MODE and STBY
	Pin polarity	0x1F	MODE_STBY_POLARITY	0x0	[if configured as MODE] LOW - auto-PFM / HIGH - forced PWM. [if configured as a STBY] LOW - STBY state / HIGH - ACTIVE state.
GPO / nWAKEUP	Function selection	0x20	GPO_nWAKEUP_CONFIG	0x0	GPO

- Operation of the buck converters in auto-PFM and forced-PWM can be changed by I2C (register field: MODE_I2C_CTRL).

Table 3-12. Default register setting for MODE_I2C_CTRL

Register Address	Field Name	Value	Description
0x1F	MODE_I2C_CTRL	0x0	0x0 = Auto PFM 0x1 = Forced PWM

3.7 Over-Current Deglitch

This section describes the default settings for the over current deglitch. When any of these registers are set (value = 1b), it enables the long-deglitch option for the corresponding rail.

Table 3-13. Over Current Deglitch

Register Address	Field Name	Value	Description
0x23	EN_LONG_DEGL_FOR_OC_BUCK1	0x0	Deglitch duration for OverCurrent on BUCK1 is ~20us
0x23	EN_LONG_DEGL_FOR_OC_BUCK2	0x0	Deglitch duration for OverCurrent on BUCK2 is ~20us
0x23	EN_LONG_DEGL_FOR_OC_BUCK3	0x0	Deglitch duration for OverCurrent on BUCK3 is ~20us

3.8 Mask Settings

This section describes the settings that are masked by default and the effect they have on the device state as well as the nINT pin.

Table 3-14. Mask Settings

	Register Address	Field Name	Value	Description
Mask effects on device state and nINT pin	0x25	MASK_EFFECT	0x03	no state change, nINT reaction, bit set for Faults
UV Mask	0x24	BUCK1_UV_MASK	0x0	un-masked (Faults reported)
	0x24	BUCK2_UV_MASK	0x0	un-masked (Faults reported)
	0x24	BUCK3_UV_MASK	0x0	un-masked (Faults reported)
	0x24	LDO1_UV_MASK	0x0	un-masked (Faults reported)
	0x24	LDO2_UV_MASK	0x0	un-masked (Faults reported)
Power-up retries/ attempts	0x20	MASK_RETRY_COUNT_ON_ FIRST_PU	0x0	RETRY_COUNT is not masked on first power-up.
	0x24	MASK_RETRY_COUNT	0x0	Device retries up to 2 times
Die Temperature	0x25	SENSOR_0_WARM_MASK	0x0	un-masked (Faults reported)
	0x25	SENSOR_1_WARM_MASK	0x0	un-masked (Faults reported)
	0x25	SENSOR_2_WARM_MASK	0x0	un-masked (Faults reported)
Masking bit to control whether nINT pin is sensitive to PushButton (PB)	0x25	MASK_INT_FOR_PB	0x1	masked (nINT pin not sensitive to any PB events)
Masking bit to control whether nINT pin is sensitive to RV (Residual Voltage)	0x25	MASK_INT_FOR_RV	0x0	un-masked (nINT pin pulled low for any RV events during transition to ACTIVE state or during enabling of rails)

3.9 Discharge Check

Each rail is discharged prior to its enable in the power sequence or by I2C. This discharge check can be skipped by setting bit BYPASS_RV_FOR_RAIL_ENABLE.

Active discharge is enabled by default and is not NVM based. If desired, this setting can be disabled after each VSYS-power-cycle. In case active discharge on a rail is disabled, it does not gate the disable of the subsequent rail, but the sequence is purely timing based. In case of residual voltage, the RV-bit is set regardless. During RESET or OFF-request, the discharge configuration is not reset, as long as VSYS is present.

Table 3-15. Discharge Check

Register Address	Field Name	Value	Description
0x1E	BYPASS_RV_FOR_RAIL_ENABLE	0x0	Discharged checks enforced

3.10 Low Power Mode

TPS6521402 includes two different low power modes enterable by STBY-request.

Table 3-16. Low Power Mode

Register Address	Field Name	Value	Description
0x22	STBY_SLEEP_CONFIG	0x0	STBY Mode

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

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