User's Guide
SLVU374–May 2010

TPS54060EVM-590 100-mA, Split Rail SWIFT™ Regulator Evaluation Module

This user's guide contains information for the TPS54060EVM-590 evaluation module (HPA590). Included are the performance specifications, the schematic, and the bill of materials for the TPS54060EVM-590.

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1 Introduction

This user's guide contains background information for the TPS54060 as well as support documentation for the TPS54060EVM-590 evaluation module (HPA590). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54060EVM-590.

1.1 Background

The TPS54060 DC/DC converter is designed to provide up to a 0.5-A output from an input voltage source of 3.5V to 60V. Rated input voltage and output current range for the TPS54060EVM-590 (HPA590) evaluation module are given in Table 1. This evaluation module is designed to demonstrate transformer-coupled split rail operation with dual outputs providing ±18V at up to ±100mA. The -18V output is used as the ground reference for the TPS54060 in this application, which allows the sum of the positive and negative outputs to be divided and sent to the VSNS pin for regulation. The switching frequency is externally set to 300kHz with a resistor at the RT/CLK pin, and the compensation components are also external to the integrated circuit (IC). The high-side MOSFET is incorporated inside the TPS54060 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS54060 to achieve high efficiency and helps keep the junction temperature low at high output currents. Additionally, the TPS54060 provides adjustable slow start and undervoltage lockout inputs.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54060EVM-590	VIN = 18 V to 30V	0 A to ±100 mA

1.2 Performance Specification Summary

A summary of the TPS54060EVM-590 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 34 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54060EVM-590 is designed and tested for V_{IN} = 12 V to 48 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54060EVM-590 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			18	24	30	V
Output voltage set point				+18, –18		V
Output current range	V_{IN} = 18 V to 30V		0		±0.1	A
Line regulation	I_O = 0.1 A, V_{IN} = 18 V to 30V			±0.24%		
Load regulation	V_{IN} = 24 V, I_O = 0.001 A to 0.1 A			±0.22%		
Load transient response	I_O = 0.05 A to 0.3 A	Voltage change		–500		mV
		Recovery time		7		ms
	I_O = 0.3 A to 0.05 A	Voltage change		500		mV
		Recovery time		7		ms
Loop bandwidth	V_{IN} = 24 V, I_O = ±0.1 A			800		Hz
Phase margin	V_{IN} = 24 V, I_O = ±0.1 A			85		°
Input ripple voltage	I_O = ±0.1 A			50		mVpp
Output ripple voltage	I_O = ±0.1 A			20		mVpp
Output rise time				40		ms
Operating frequency				300		kHz
Maximum efficiency	TPS54060EVM-590, V_{IN} = 24 V, I_O = ±0.1 A			92%		

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54060EVM-590 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS54060EVM-590 is provided with input/output connectors and test points as shown in Table 3. A power supply capable of supplying 0.5 A must be connected to J1 through a pair of 20 AWG wires. The loads must be connected to J2 and J3 through 20 AWG wires. The maximum load current capability must be 0.1 A each. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP7 and TP9 are used to monitor the output voltages with TP8 and TP10 as the ground references.

Table 3. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range)
J2	V_{OUT1}, +18 V at 100 mA maximum
J3	V_{OUT2}, –18 V at –100 mA maximum
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	V_{IN} test point at V_{IN} pin
TP4	PH test point
TP5	Test point between voltage divider and output, used for loop response measurements
TP6	Test point at +18 V pin of output inductor
TP7	Output voltage test point at +18 V connector
TP8	GND test point at +18 V connector
TP9	Output voltage test point at –18 V connector
TP10	GND test point at –18 V connector

2.2 Efficiency

Figure 1 shows the efficiency for the TPS54060EVM-590 at an ambient temperature of 25°C.

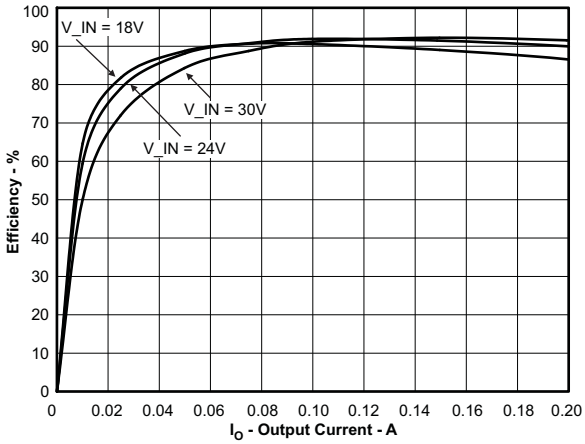

Figure 1. TPS54060EVM-590 Efficiency

2.3 Output Voltage Load Regulation

The load regulation for the TPS54060EVM-590 is shown in Figure 2.

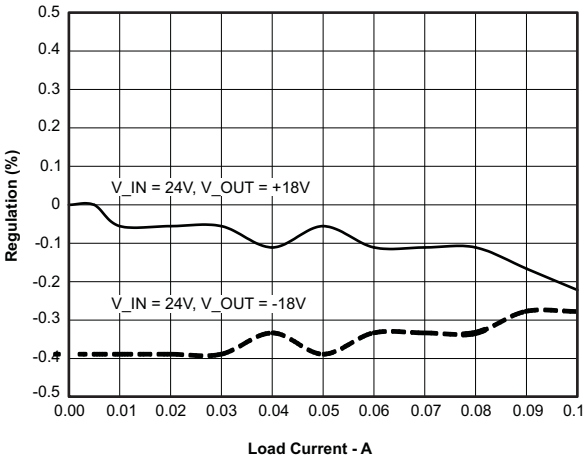

Figure 2. TPS54060EVM-590 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

The line regulation for the TPS54060EVM-590 is shown in Figure 3.

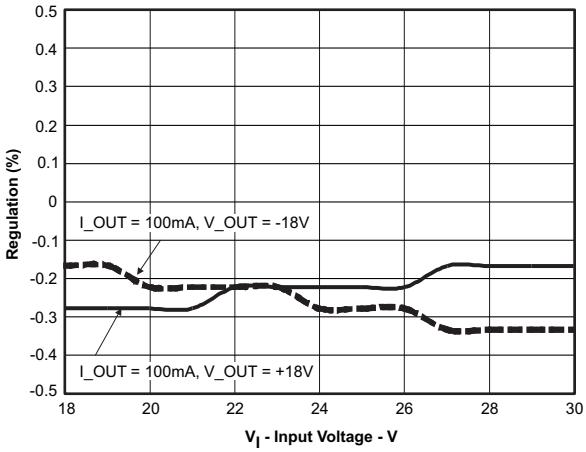

Figure 3. TPS54060EVM-590 Line Regulation

2.5 Load Transients

The TPS54060EVM-590 response to load transients is shown in Figure 4. The current step is from 50% to 100% of maximum rated load at 24-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

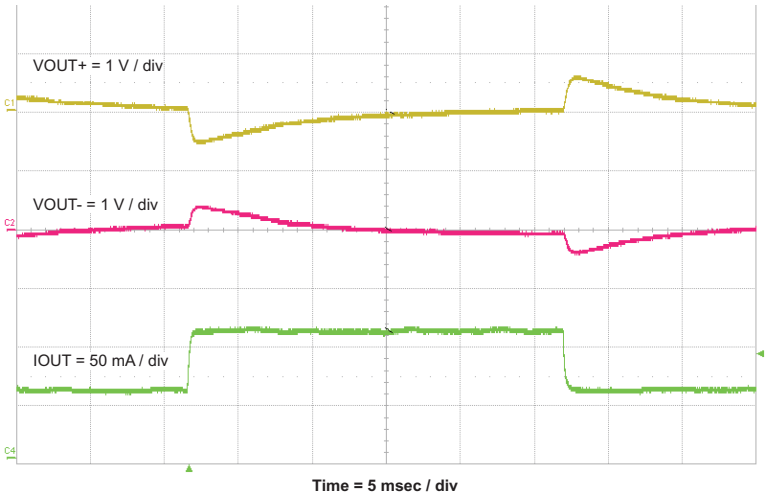

Figure 4. TPS54060EVM-590 Transient Response

2.6 Loop Characteristics

The TPS54060EVM-590 loop-response characteristics are shown in Figure 5 . Gain and phase plots are shown for V_{IN} voltage of 24 V. Load current for the measurement is ±100 mA.

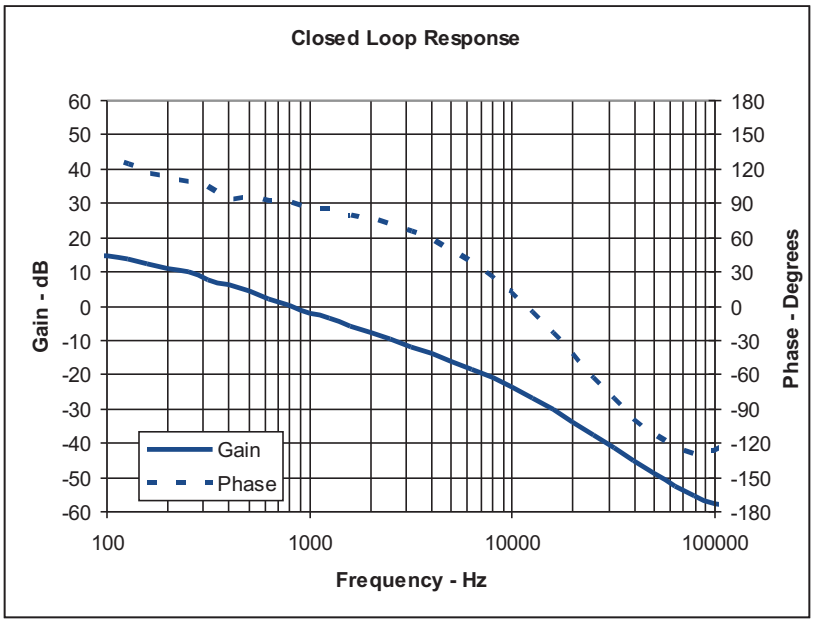

Figure 5. TPS54060EVM-590 Loop Response

2.7 Output Voltage Ripple

The TPS54060EVM-590 output voltage ripple is shown in Figure 6 . The output current is the rated full load of ±100 mA and V_{IN} = 24 V. The ripple voltage is measured directly across the output capacitors.

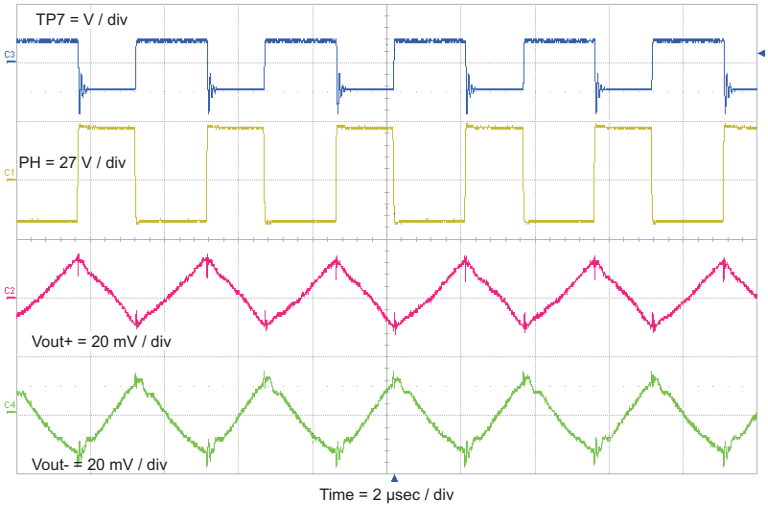

Figure 6. TPS54060EVM-590 Output Ripple

2.8 Input Voltage Ripple

The TPS54060EVM-590 input voltage ripple is shown in Figure 7 . The output current is the rated full load of ±100 mA and V_{IN} = 24 V. The ripple voltage is measured directly across the input capacitors.

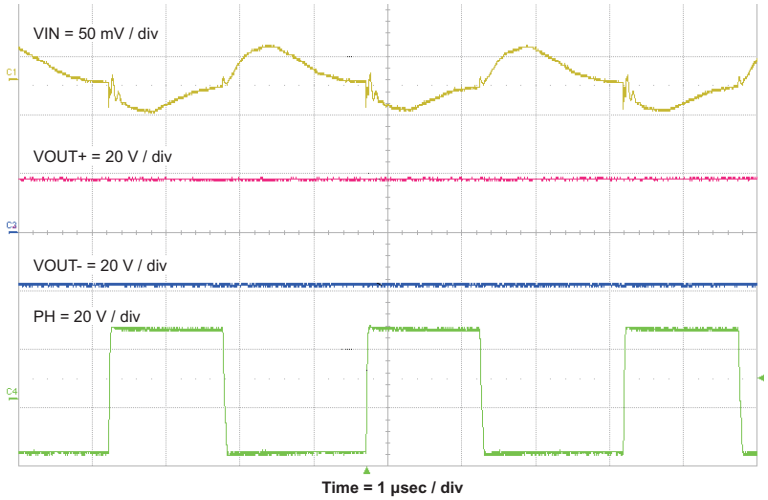

Figure 7. TPS54060EVM-590 Input Ripple

2.9 Powering Up

The start-up waveforms are shown in Figure 8. The input voltage for these plots is 24 V with a ±100 mA load.

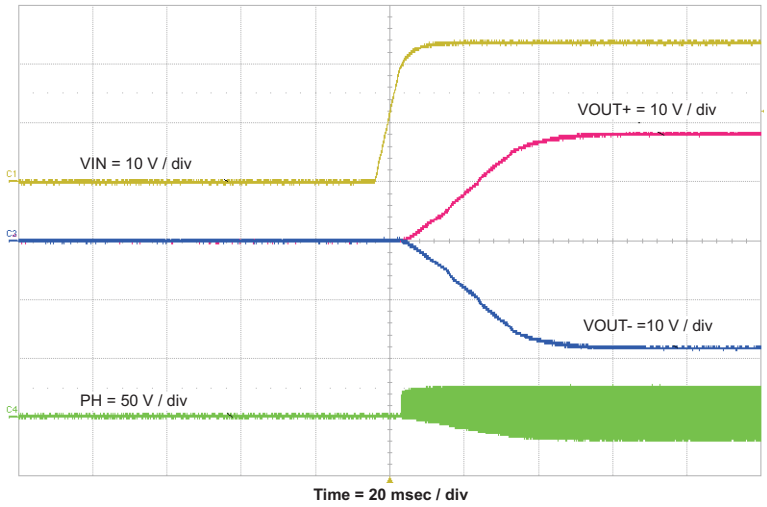

Figure 8. TPS54060EVM-590 Start-Up Relative to V_{IN}

3 Board Layout

This section provides a description of the TPS54060EVM-590, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54060EVM-590 is shown in Figure 9 through Figure 11. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for V_{IN}, +18 v, –18 v, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54060 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including six vias directly under the TPS54060 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C2 and C3) and bootstrap capacitor (C5) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace past the output capacitor (C10 and C11). For the TPS54060, an additional input bulk capacitor may be required (C1), depending on the EVM connection to the input supply.

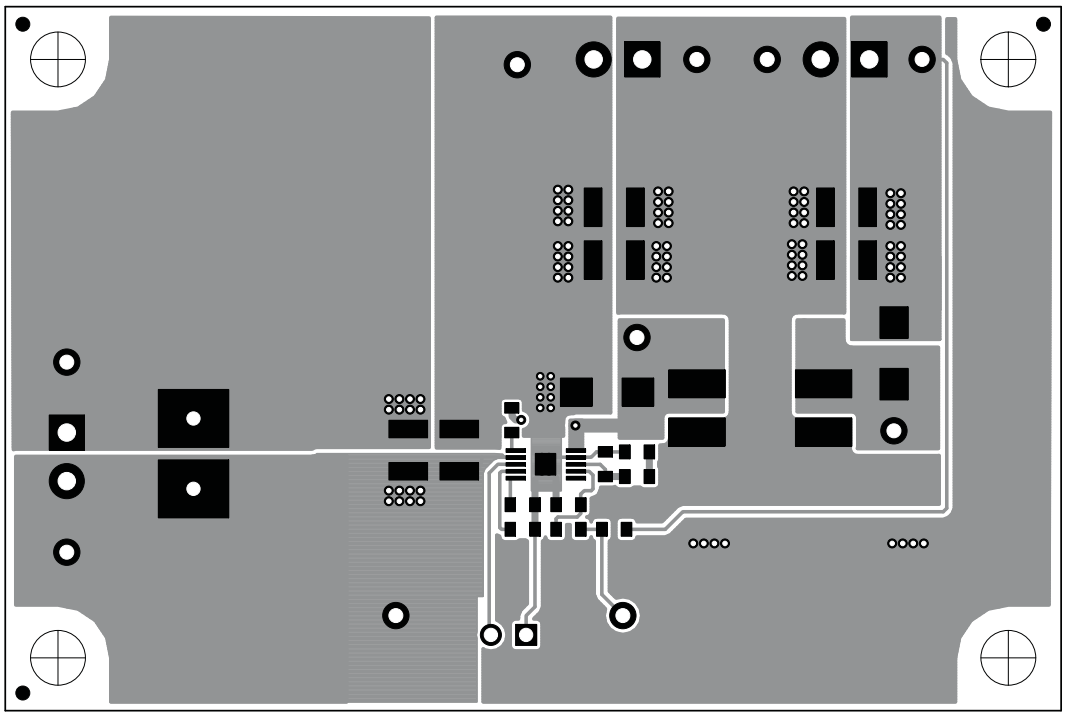

Figure 9. TPS54060EVM-590 Top-Side Layout

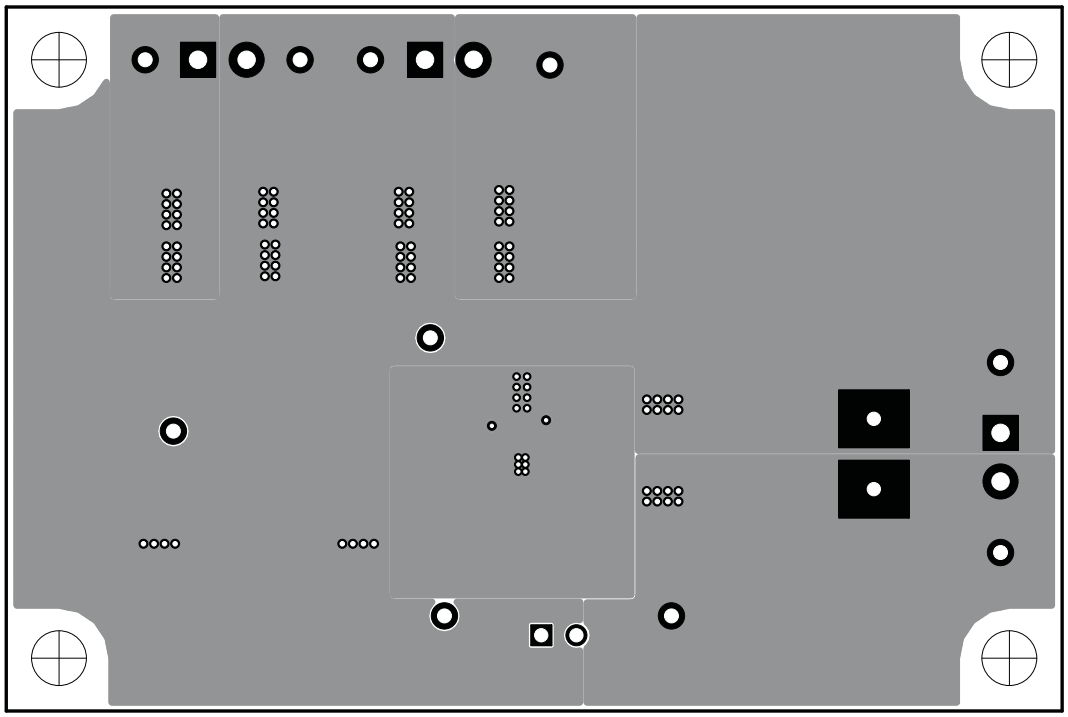

Figure 10. TPS54060EVM-590 Bottom-Side Layout

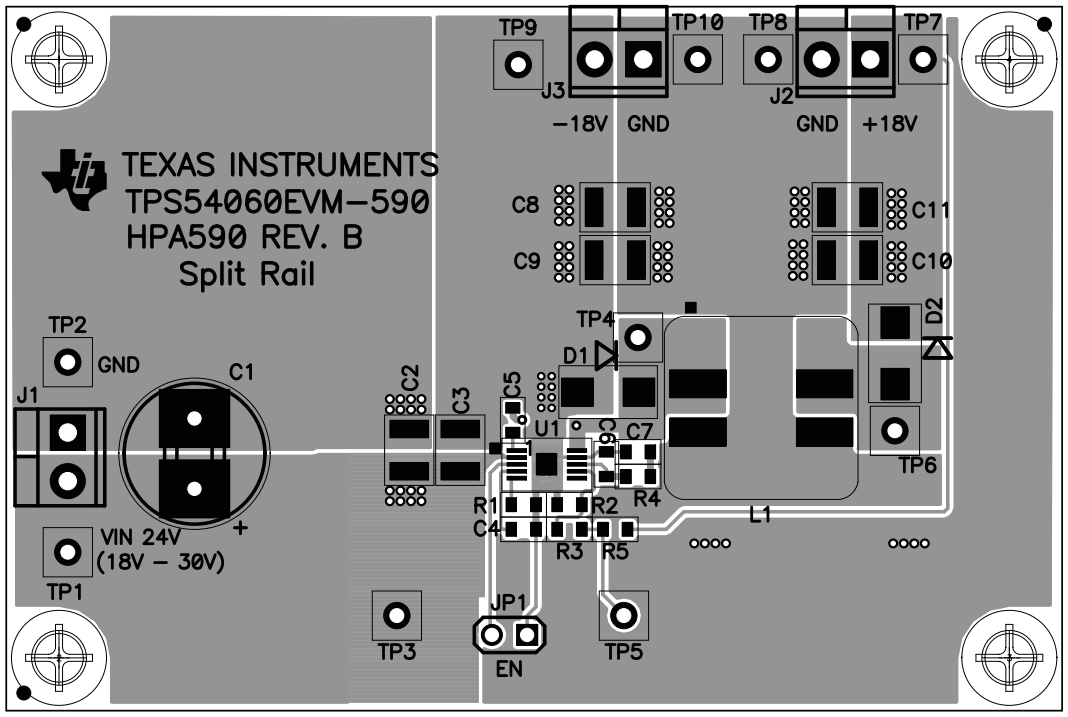

Figure 11. TPS54060EVM-590 Top-Side Assembly

4 Schematic and Bill of Materials

This section presents the TPS54060EVM-590 schematic and bill of materials.

4.1 Schematic

Figure 12 is the schematic for the TPS54060EVM-590.

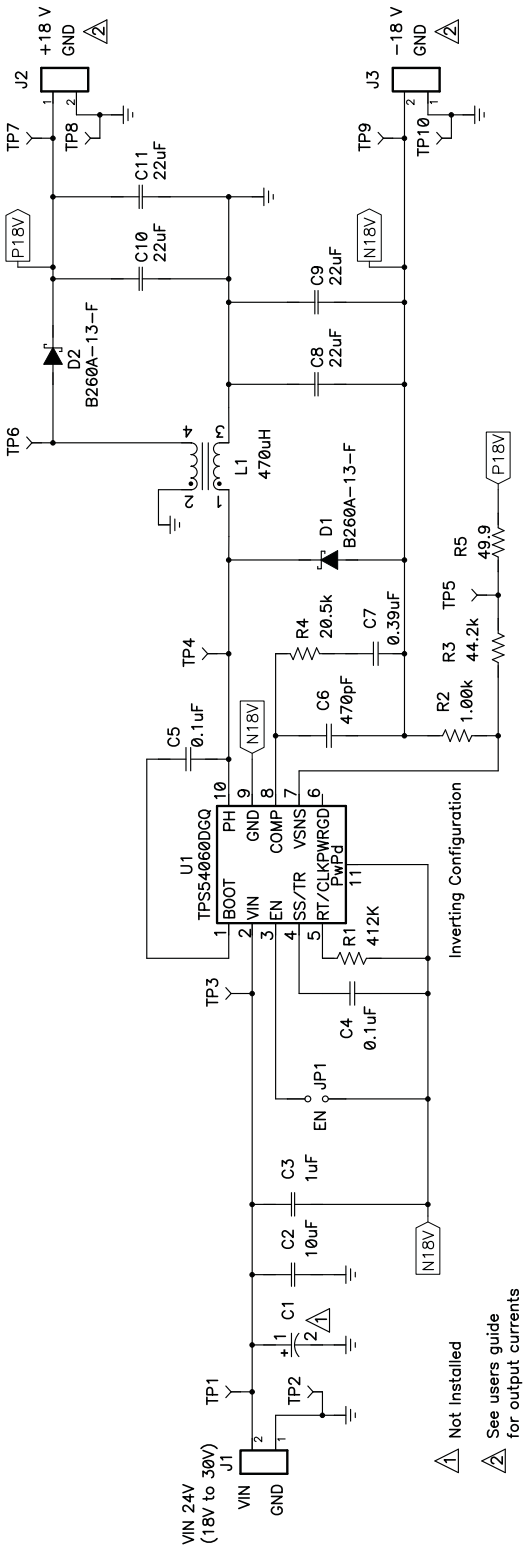

Figure 12. TPS54060EVM-590 Schematic

4.2 Bill of Materials

Table 4 presents the bill of materials for the TPS54060EVM-590.

Table 4. TPS54060EVM-590 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1	Open	Capacitor, multi pattern SM 1210 to E case + F THole	Multi sizes	Engineering Only	Std
1	C2	10µF	Capacitor, Ceramic, 50V, X5R, 20%	1210	Std	Std
1	C3	1µF	Capacitor, Ceramic, 100V, X7R, 20%	1210	Std	Std
2	C4, C5	0.1µF	Capacitor, Ceramic, Low Inductance, 25V, X7R, 10%	0603	Std	Std
1	C6	470pF	Capacitor, Ceramic, Low Inductance, 50V, X7R, 10%	0603	Std	Std
1	C7	0.39µF	Capacitor, Ceramic, 10V, X5R, 10%	0603	Std	Std
4	C8, C9, C10, C11	22µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	Std	Std
2	D1, D2	B260A-13-F	Diode, Schottky Barrier Rectifier, 2A, 60V	SMA	B260A-13-F	Diodes, Inc.
3	J1, J2, J3	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25""	ED555/2DS	OST
1	JP1	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	470µH	Inductor, SMT, 1A, 1.59milliohm, ±10%	0.484 x 0.484 inch	MSD1260-47KL	Coilcraft
1	R1	412kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	1.00kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	44.2kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	20.5kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	49.9Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
7	TP1, TP3, TP4, TP5, TP6, TP7, TP9	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
3	TP2, TP8, TP10	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	TPS54060DGQ	IC, 0.5A, 60V Step-Down		TPS54060DGQ	TI
1	–		Shunt, 100-mil, Black	0.100	929950-00	3M
1	–		PCB, 2.0" x 3.0" x 0.062"		HPA590	Any

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 10.8 V to 19.8 V and the output voltage range of 1.3 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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