Functional Safety Information

TPS3813-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TPS3813-Q1 (Sot23 (6) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

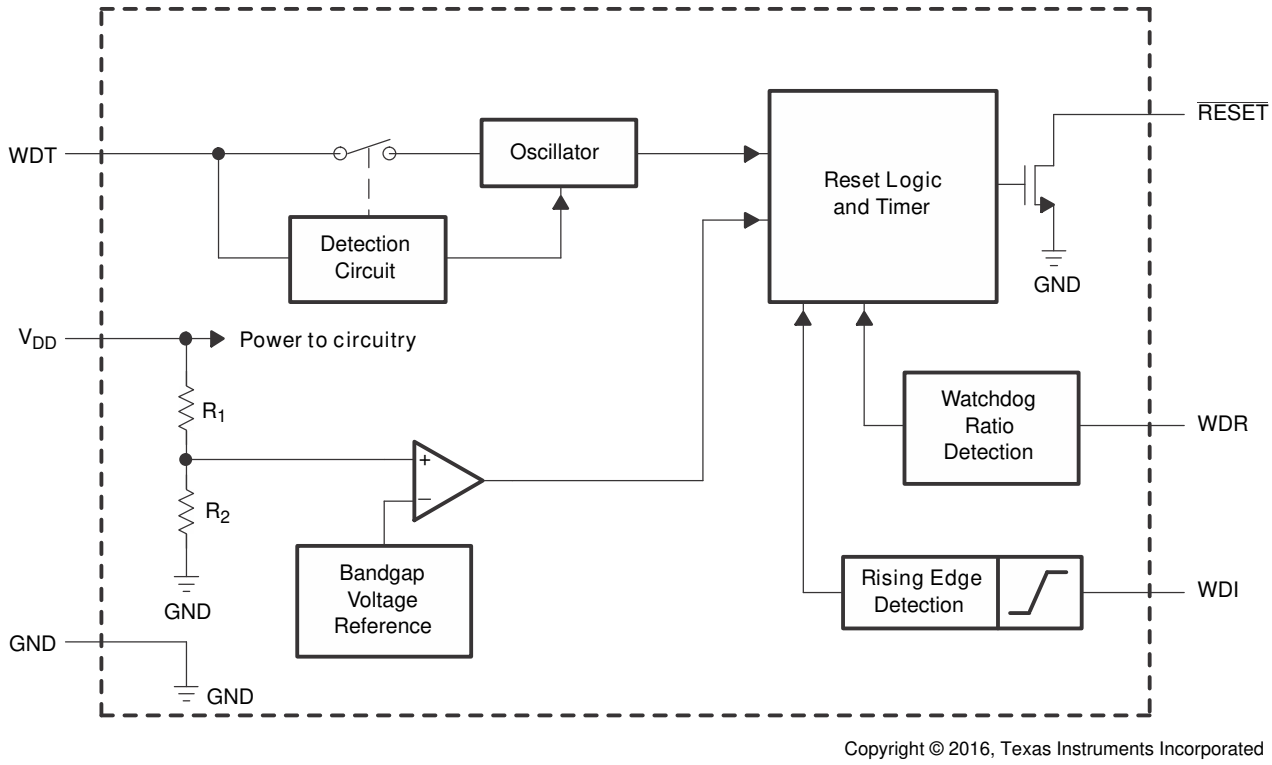

Figure 1-1. Functional Block Diagram

TPS3813-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS3813-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 35mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, Analog, Mixed	25 FIT	55 C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS3813-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
$\overline{\text{RESET}}$ false trip	1
RESET stays asserted	5
$\overline{\text{RESET}}$ trips outside specification (voltage or time)	60
Threshold does not meet specification (temperature)	30
Iq specifications do not meet specification	4

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS3813-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDD (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS3813-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS3813-Q1 data sheet.

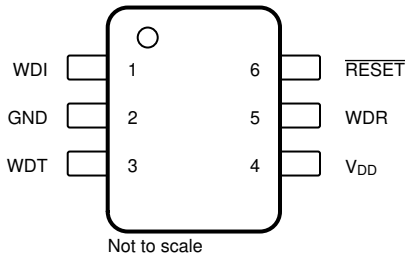

Figure 4-1. Top View Sot23 (6) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
WDI	1	A constant watchdog timeout fault is detected on the $\overline{\text{RESET}}$ pin.	B
GND	2	Normal operation.	D
WDT (When WDT = VDD)	3	VDD shorts to GND. The device has no power for normal operation.	B
WDT (When WDT = GND)	3	Behavior is as expected. Refer to the *Window-Watchdog Configuration Setting* table in the data sheet.	D
WDT (When WDT = External Capacitor)	3	The expected timing is observed until a voltage fault occurs. After the fault, the timing changes accordingly, since WDT = GND.	C
VDD	4	The device is not damaged, but the condition of the device is undefined. The $\overline{\text{RESET}}$ pin tends to be low.	B
WDR (When WDR = VDD)	5	VDD shorts to GND. The device has no power for normal operation.	B
WDR (When WDR = GND)	5	Normal operation mode. Behavior is as expected. Refer to the *Window-Watchdog Configuration Setting* table in the data sheet.	D
$\overline{\text{RESET}}$	6	The $\overline{\text{RESET}}$ pin is constantly low; some additional current can flow through the pullup resistor.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
WDI	1	A constant watchdog timeout fault is detected on the $\overline{\text{RESET}}$ pin.	B
GND	2	The device is not operational.	B
WDT	3	No damage to the device, but the device enters an undefined timing operation. Observe that the window frame (twindow) shortens when WDT is left open.	B
VDD	4	The device is not powered.	B
WDR	5	No damage to the device, but TI recommends that this pin is not left open.	B
$\overline{\text{RESET}}$	6	High impedance output, $\overline{\text{RESET}}$ functionality.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Relevant Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
WDI	1	GND	A constant watchdog timeout fault is detected on the $\overline{\text{RESET}}$ pin.	B
GND	2	WDT	The failure effect class depends on the WDT connection. Refer to the *Short Circuit to Ground* table.	Dependent
WDT	3	VDD	The failure effect class depends on the WDT connection. Refer to the *Short Circuit to VDD* table.	Dependent
VDD	4	WDR	The failure effect class depends on the WDR connection. Refer to the *Short Circuit to VDD* table.	Dependent
WDR	5	$\overline{\text{RESET}}$	No damage to the device, but the device is in an undefined operating condition. The failure effect class depends on the WDR connection; the $\overline{\text{RESET}}$ pin is either tied to GND or VDD. Refer to table 4.2 and 4.5 of this section.	Dependent
$\overline{\text{RESET}}$	6	WDI	No damage to the device, but the device is in an undefined operating condition. With the WDI signal applied: $\overline{\text{RESET}}$ forcefully follows the WDI input, and no reset assertion occurs due to VDD voltage faults.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
WDI	1	A constant watchdog timeout fault is detected on the $\overline{\text{RESET}}$ pin.	B
GND	2	VDD shorts to GND. The device has no power for normal operation.	B
WDT (When WDT = VDD)	3	Behavior is as expected. Refer to the *Window-Watchdog Configuration Setting* table in the data sheet.	D
WDT (When WDT = GND)	3	VDD shorts to GND. The device has no power for normal operation.	B
WDT (When WDT = External Capacitor)	3	The expected timing is observed until a voltage fault occurs. After the fault, the timing changes accordingly; since WDT = VDD.	B
VDD	4	Normal operation.	D
WDR (When WDR = VDD)	5	Normal operation mode. Behavior is as expected. Refer to the *Window-Watchdog Configuration Setting* table in the data sheet.	D
WDR (When WDR = GND)	5	VDD shorts to GND. The device has no power for normal operation.	B
$\overline{\text{RESET}}$	6	A large current can flow into the device, potentially causing damage.	A

5 Revision History

Changes from Revision * (November 2020) to Revision A (June 2025)	Page
• Updated the package name	2
• Updated *Power Dissipation* and *Reference FIT Rate*	3
• Updated the *Die Failure Modes and Distribution* table	4
• Added package image	5
• Updated each pin-FMA table	5

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