

# TPS65987x, TPS65988x Power and Data Role Swaps

#### ABSTRACT

Power and data role swaps allow individual devices to change their roles under certain conditions. This ability allows a power source to become a sink, a data DFP (Downward Facing Port) to become a data UFP (Upward Facing Port), or both. The roles are negotiated using USB Power Delivery (PD) messaging according to the USB PD specification. This application report explains the standard implementation of data and power role swaps as well as assigning data and power preferences to individual USB Type-C ports. This application report is to be used with Texas Instruments' TPS65987x and TPS65988x families of USB Type-C and USB PD controllers and associated software tools.

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#### 1 Introduction

The Power Delivery specification allows two connected dual-role ports to optionally switch their data role, their power role, or both roles using the power-role swap and data-role swap mechanisms.

Texas Instruments' TPS65987 and TPS65988 families of USB Type-C and USB PD controllers can be configured to automatically initiate data or power role swaps to a desired state, or the same role swaps may be initiated by an external microcontroller through host interface commands. The control configuration (0x29) register is used to specify automatically initiated role swaps. You can specify a preferred data role by using the *Initiate Swap to DFP* command instead of the *Initiate Swap to UFP* command, and can configure the device to either allow or disallow swaps through the *Process Swap to DFP* and *Process Swap to UFP* bits. The power roles have similar settings.

Using an external microcontroller to modify data and power roles using host interface commands provides an additional level of functionality. Whereas the control configuration register provides a simple preference towards one setting or the other setting, an external microcontroller can use information gathered from the TPS65987 and TPS65988 host interface status registers to make more advanced power and data role decisions. For instance, a microcontroller could use the externally powered bit of the connection partner as stored in the Rx Source Capabilities (0x30) register to make a more informed decision when setting power role orientation.

## 2 Role Swap Configuration in Host Interface Registers

The TPS65987 and TPS65988 registers include the following:

- Configuration registers:
  - 0x28, Port Configuration register, Type-C supported options fields
  - 0x29, Port control register, all fields
- Status registers:
  - 0x1A, Status register, Port Role and Data Role fields
  - 0x3F Power status register, Source or Sink field
  - 0x2D, Boot Status register, *Dead Battery* field
- Run-Time Host-Interface Commands:
  - SWSr, swap to source (power)
  - SWSk, swap to sink (power)
  - SWDF, swap to DFP (data)
  - SWUF, swap to UFP (data)

The Port Control register (0x29) is the primary register used to control role swap behavior. This register allows you to configure the initiation of role swaps, which causes the TPS65987 and TPS65988 PD controller to automatically initiate the given role swap, and it allows you to configure the processing of role swaps, which controls whether the TPS65987 and TPS65988 USB PD controller accepts or does not accept various role swap requests initiated by the port partner.

The Port Configuration register (0x28) can used to set what initial role the device can take when Type-C connection is made. The Port Configuration field can chose between DFP only, UFP only, or DRP. The Type-C Supported Options field selects if the DRP port has additional options as Try.Src (Try Source) or Try.Snk (Try Sink), simple no options, or it can declare it is a powered accessory. The default templates that are used in this document do not have Type-C Supported options set as "No Options", but you can modify this to Try.Src for the preferred Source project.

The Status register (0x1a) reports the current data and power role of the system. The Boot Status register (0x2d) is also important as it reports whether or not the system is currently in Dead Battery Mode, and a system that is in Dead Battery Mode does not support power role swaps. Power status register (0x3F) can be used to look at power role easily.

Finally, four host interface commands can be used to manually initiate a data or power role swap using an external controller. As discussed in this application report, certain system conditions must still be met in order for a role swap to occur. If these conditions are not met, the host interface swap command is rejected.



#### 3 Data and Power Role Swap Examples

The TPS6598x Configuration Tool contains multiple dual-role port configurations, all of which use one of two data and power role swap settings. Refer to the *TPS6598x Application-Customization Tool User Guide* to select the appropriate template that best represents your project configuration.

When a new project is started from the Configuration Tool, it asks for following questions to select correct template -

- 1. Which device are you using? For example, the TPS65987DDH.
- 2. Which template type do you want to start with?
  - Standard
  - Advanced
- 3. What is the port type of the design? The choices are the following:
  - Upstream Facing Port(UFP) only
  - Downstream Facing Port (DFP) only
  - Dual Role Port (DRP), prefers data host
  - Dual Role Port (DRP), prefers power source
- 4. Which Super Speed data controller or mux is used?

Choices on the third question determine the behavior of the Date Role and Power Role swaps. For example, if you select "DRP, prefers power source", these generated project variants initiate a power role swap if necessary to become a power source, but the do not initiate data role swap, but instead accept any data role swap. If you select "DRP, prefers power source", these variants initiate a power role swap if they start as sink, and they do not initiate data role swap, but accept data role swap.

In the second question, if you have selected the "Standard" template configuration, the Port Control (0x29) register view relating to Power and Data role swap has a simplified view each of strategy having four options. Tools generate appropriate bit settings required for the options selected, whereas in the case of the "Advanced" template configuration, the register view shows individual bits as defined in the Host Interface TRM document. Figure 1 shows Port Control Data Role strategy settings in standard template and Figure 2 shows Port Control Power Role strategy settings in standard template.

Application Customization Tool		- 🗆 X
Project Binary Device Settings Debug Document	ts Help	
General Settings Common Settings		
Configuration Mode		S65987DDH_Standard_v5_13.tpl S65987DDH (Standard), Version 5.13
Customer Use Global System Configuration Port Configuration	Port Control (0x29)	
Port Control	Field	Value
Transmit Source Capabilities	Type-C Current	3 A (strongest pullup)
Transmit Sink Capabilities PD3 Configuration Register	Power Swap Strategy	No Preference, Supports All Swaps
Transmit Identity Data Object	Data Swap Strategy	No Preference, Rejects All Swaps No Preference, Supports All Swaps
Display Port Capabilities	Externally Powered	Prefers Power Source
Intel VID Config Register	Sink Control Bit	Prefers Power Sink
Tx Manufacturer Info SOP	Charger Advertise Enable	Charger Advertise Disabled
Tx Source Capabilities Extended Data Block Raw View	Charger Detect Enable	BC1.2 Detection

Figure 1. Port Control Data Role strategy Settings in a Standard Template



Help					
Port Control (0x29)					
Field	Value				
Type-C Current	3 A (strongest pullup)				
Power Swap Strategy	No Preference, Supports All Swaps	-			
Data Swap Strategy	No Preference, Rejects All Swaps				
Externally Powered	Prefers Power Source				
Sink Control Bit	Prefers Power Sink				
Charger Advertise Enable	Charger Advertise Disabled	•			
	TP: TP: Port Control (0x29) Field Type-C current Power Swap Strategy Data Swap Strategy Data Swap Strategy Externally Powered Sink Control Bit	TPS65987DDH_Standard_v5_13.tp TPS65987DDH (Standard), Version           Port Control (0x29)         Field         Value           Type-C current         3 A (strongest pulup)         Power Swap Strategy         No Preference, Supports Al Swaps           Data Swap Strategy         No Preference, Rejects Al Swaps         Statemally Powered         Prefers Power Source           Sink Control Bit         Prefers Power Source         Source         Source			

Figure 2. Port Control Power Role Strategy Settings in a Standard Template

Between Standard and Advanced, the only difference is the register view. This document limits discussion to Advanced template view of Port control register, as it is better suited to illustrate detailed functionality of power and data role swaps.

Note that the names of templates discussed below start with the last portion of the file name that points to the version of the Configuration tool being used, which gets updated whenever a newer version of configuration tool is used. For example, template *TPS65987DDH\_Advanced\_v5\_13.tpl* is for the TPS65987DDH device and was done based on configuration tool version 5.13.

eneral Settings Common Settings			
cheral Settings Contribut Settings			
Configuration Mode		PS65987DDH_Advanced_v5_ PS65987DDH (Advanced), Ve	
Customer Use	Port Control (0x29)		
Interrupt Mask for I2C1			
Interrupt Mask for I2C2 Global System Configuration	Field	Value	
Port Configuration	Type-C Current	3 A (strongest pullup)	
Port Control	PD Mode	Normal PD Behavior	
Transmit Source Capabilities Transmit Sink Capabilities	Process Swap To Sink		
Autonegotiate Sink	Initiate Swap To Sink		
Alternate Mode Entry Queue	Process Swap To Source	2	
PD3 Configuration Register Event Delay	Initiate Swap To Source		
Transmit Identity Data Object	Process VCONN Swap	2	
User Alternate Mode Config	Process Swap to UFP		
Display Port Capabilities Intel VID Config Register	Initiate Swap to UFP	6	
MIPI VID Configuration	Process Swap to DFP	M	
I/O Config Retimer Debua Register	Initiate Swap to DFP	2	
App Config Binary Data Indices	Automatic ID Request	2	
I2C Master Configuration	Force USB Generation 1	6	
App configuration Register Sleep Control Register	Externally Powered	6	
Tx Manufacturer Info SOP	Automatic Sink Cap	Z	
Tx Source Capabilities Extended Data Block	Sink Control Bit	6	
Tx Battery Capabilities Tx Manufacturer Info SOP Prime	15 kOhm Resistor Present	6	
Raw View	Data Contact Detection Enable		
	Charger Advertise Enable	Charger Advertise Disabled	
	USB Disable		
	Charger Detect Enable	BC1.2 Detection	

Figure 3. Port Control Register (0x29) Advanced Settings Tab for "Preferred Host"

Figure 3 shows the Control Configuration register (0x29) settings for the *TPS65987DDH\_Advanced\_v5\_13.tpl* project set as "preferred Host". For this project, Process Swap to Sink, and Process Swap to Source are both enabled, but Initiate Swap to Sink and Initiate Swap to Source are both disabled. This indicates that the system accepts either power role swap request from a connected device but does not (automatically) initiate a power swap request of either type. This is an agnostic configuration since it supports both power roles without driving a preference towards one or the other.

By contrast, the data role swap settings are as follows: *Initiate Swap to DFP* and *Process Swap to DFP* are both enabled, but *Initiate Swap to UFP* and *Process Swap to UFP* are both disabled. This combination indicates that the device always attempts to become the data DFP (host) in the connection.

**NOTE:** The *Swap to DFP* setting indicates that the device being configured swaps to become the DFP for both the *Initiate* and *Process* settings. This setting is a preferred data configuration because it drives the system towards a configuration in which the device is data DFP if possible.

When setting the initiate and process bits in the Control Configuration register, avoiding a configuration that could potentially lead to an infinite sequence of data or power role swaps is important. First, system should never be configured to initiate swaps in both directions (such as selecting *Initiate Swap to UFP* and *Initiate Swap to DFP* in the same configuration). First, this would be a meaningless configuration because it provides no preference to data or power role and therefore is swapping seemingly for the sake of swapping, but second, if the port partner accepts swaps in both directions, this configuration would lead to an infinite series of swaps.

Likewise, any configuration that initiates a data or power role swap should not process swaps in the reverse direction. Two systems that are both configured to *Initiate Swap to DFP* and *Process Swap to UFP* toggle infinitely back and forth as each system continually initiates swaps to attempt to become DFP. In any event, a system that prefers to be configured as DFP would have no reason to accept swaps to UFP since this would require relinquishing the preferred role.

Comparing the settings of Figure 3 to those of the "preferred Source" project as shown in Figure 4, it is seen that the latter project is configured to drive towards a power source role by selecting *Process Swap to Source* and *Initiate Swap to Source*, and deselecting *Process Swap to Sink* and *Initiate Swap to Sink*. The data role is left agnostic by enabling the *Process* settings in both directions but disabling the *Initiate* settings.

eneral Settings Common Settings			
Configuration Mode		PS65987DDH_Advanced_v5_ PS65987DDH (Advanced), Ve	
Customer Use Interrupt Mask for I2C1	Port Control (0x29)		
Interrupt Mask for I2C2 Global System Configuration	Field	Value	
Port Configuration	Type-C Current	3 A (strongest pullup)	
Port Control Transmit Source Capabilities	PD Mode	Normal PD Behavior	
Transmit Source Capabilities	Process Swap To Sink		
Autonegotiate Sink	Initiate Swap To Sink	6	
Alternate Mode Entry Queue PD3 Configuration Register	Process Swap To Source	V	
Event Delay	Initiate Swap To Source	V	
Transmit Identity Data Object	Process VCONN Swap	<b>V</b>	
User Alternate Mode Config Display Port Capabilities	Process Swap to UFP	V	
Intel VID Config Register	Initiate Swap to UFP		
MIPI VID Configuration	Process Swap to DFP	<u> </u>	
VO Config Retimer Debug Register	Initiate Swap to DFP	6	
App Config Binary Data Indices	Automatic ID Request	V	
2C Master Configuration	Force USB Generation 1	6	
App configuration Register	Externally Powered	<u> </u>	
Sleep Control Register Tx Manufacturer Info SOP	Automatic Sink Cap	<u> </u>	
Tx Source Capabilities Extended Data Block	Sink Control Bit		
Tx Battery Capabilities Tx Manufacturer Info SOP Prime	15 kOhm Resistor Present	<u> </u>	
TX Manufacturer into SOP Prime Raw View	Data Contact Detection Enable		
	Charger Advertise Enable	Charger Advertise Disabled	
	USB Disable		
	Charger Detect Enable	BC1.2 Detection	

Figure 4. Port Control Advanced Settings Tab for "preferred Source"

The following PD message trace was taken with a Teledyne LeCroy PD analyzer between two TPS65987 EVMs, one setup as the "preferred Source" and the other setup as "preferred Host". If the project which is set as "preferred Source" has the try.SRC feature enabled in port config register(0x28), the trace always follows this structure so long as either both boards are powered before connection or the board containing the source settings is powered with the host board in Dead Battery Mode. This trace was taken with both boards powered. This example also uses a non-e-marked cable, which leads to the cable resets and VConn Swap, which is discussed.



Ca 4 Packets SC CBL PD Meg Meg Type Cable Plug Meg ID Obj Cht VDM Header C	md Cmd Type Obj Pos Vendor ID Duration Time Time Stamp
Vendor Defined DFP or UFP 0 1 Discove	er Identity Initiator 0 PD SID 638.442 us 7.201 ms 1 . 584 508 000
Packet         Left         SRC         PD Msg         Msg Type         DR         PR         Msg ID         Obj Cnt         Fixed         Max Cur           42         "Left"         SRC         PD Msg         Msg Type         DFP         SRC         0         3.00 A	Voltage         Dual Role         Max Cur         Voltage         Dual Role         Max Cur         Voltage         Dual Role           5.00 V         0         3.00 A         12.00 V         0         Max Cur         Voltage         Dual Role
A SNK PD M60	r Cut/Pow Opr Cut/Pow Cap Mismatch Obj Pos Duration Time Tin 75.00W 3.00A / 75.00W 0 3 632.016 us 1.337 ms 1 . 5
Packet         Left         SRC ➡         PD Msg         Msg Type         DR         PR         Msg ID         Obj Cnt         Duration           46         "Left"         SRC ➡         PD Msg         Accept         DFP         SRC         1         0         501.683 us	Time         Time Stamp           32.019 ms         1 . 594 990 000
0 Packet Left SRC 2 PD Msg Type DR PR Msg ID Obj Cnt Duration	Time         Time Stamp           1.466 ms         1.627 009 000
Packet         Right         # snk         PD Meg         DE Type         DR         PR Meg         D Obj Cnt         Duration           0         51         "Right"         # snk         PD Meg         DR Swap         UFP SNK         1         0         493.255 us	Time         Time Stamp           1.206 ms         1.628 475 000
0 Packet Left SRC → PD Msg Msg Type DR PR Msg ID Obj Cnt Duration 53 Teft SRC → Accest DFP SRC 3 0 501.633 us	Time Time Stamp 1.389 ms 1 , 629 651 000
Packet CBL PD Meg Meg Type Cable Plug Meg ID Obj Cht Duration Idle Soft Reset DPF or UFP 0 0 493.256 us 1.135 f	Time Stamp
Packet         Display         CBL         PD Msg         Type         Cable Flug         Msg ID Obj Cntt         Duration         Idle           56         Soft Reset         DFP or UFP         0         0         493.256 us         1.132 r	Time Stamp
Packet         CBL         PD Msg Type         Cable Plug         Msg Type         Msg T	Time Stamp
Packet C** CBL PD Msg Type Cable Plug Msg ID Obj Cht Duration Ide     So CBL PD Msg So Reset DPF of UPP 0 0 043,255 us 1,209	Time Stamp
Packet Right P SNK P Neg VCon Swap DP ISNK 2 0 495.256 us	Time         Time Stamp           1.195 ms         1.637 670 000
Control and the second s	Time         Time Stamp           2.329 ms         1.633.685.000
Cert     Cert	Time Time Stamp
Packet At Cable Reset Duration Idle Time Stamp	50.399 ms 1.641 194 000
65         279.972 us         155.028 us         1 . 691 593 000           Packet         99" and         Msg Type         Cable Plug         Msg ID         Obj Cnt         Duration         Idle	Time Stamp
0 CBL PD Msg Soft Reset DFP or UFP 0 0 498.256 us 1.132 r	
Packet         ≥==         CBL         PD Msg         Msg Type         Cable Plug         Msg ID         Dbj Cnt         Duration         Idle           67         →         CBL         PD Msg         Soft Reset         DFP or UFP         0         0         498.256 us         1.131 r	Time Stamp ms 1 . 693 658 000
Packet         Image: CBL         PD Msg         Msg Type         Cable Plug         Msg ID         Obj Cht         Duration         Idle           65         Image: CBL         Soft Reset         DFP or UFP         0         0         498.256 us         1.132 r	Time Stamp           ms         1 . 695 287 000
Packet         @"         CBL         PD Msg         Meg Type         Cable Plug         Meg ID         Obj Cht         Duration         Idle           69         69         CBL         PD Msg         Soft Reset         DFP or UFP         0         0         498.256 us         1.213 r	Time Stamp           ms         1.696 917 000
Packet         81'         CBL         Cable Reset         Duration         Idle         Time Stamp           2         70         →         CBL         Cable Reset         279.972 us         10.243 ms         1 . 698 628 000	

Figure 5. DRP Host Connected to DRP Source PD Trace (Excerpt)

Figure 5 shows the expected sequence of PD operations for this example. This sequence is only a partial trace. The system continues with a Discover Identity, Discover SVIDs/Modes, and mode entry.

- 1. Packets 01 through 37 (not displayed in Figure 5) The EVM set up as "preferred Source" connects as the DFP and "preferred Host" connects as the UFP. This always happens, so long as the EVM programmed with the source settings is powered, and try.SRC is enabled and the host settings are not.
- 2. Packets 38 through 41 A Discover Identity request and three retries are sent to the cable. Because it is a non-e-marked cable, there is no response.
- 3. Packets 42 through 49 The PD power contract is negotiated. See Section 3 of this document for an explanation of the configuration of this stage of PD negotiation.
- 4. Packet 51 The EVM configured as "preferred Host" makes a data role swap request. This occurs because *Initiate Swap to DFP* is enabled in the Control Configuration register of this project and it is currently the UFP. Additional conditions are required for this to occur, as shown in .
- 5. Packet 53 The EVM configured as "preferred Source" accepts the data role swap request. This occurs because *Process Swap to UFP* is enabled in the Control Configuration register of this project and it is currently the DFP. Additional conditions are required for this to occur, as listed in Table 1.
- 6. Packets 55 through 58 The EVM configured as "preferred Host" issues a soft reset command to the cable with three retries. The new DFP always attempts a soft reset to the cable following a data-role swap to reset the message ID to 0. The cable used in this example does not respond because it is not e-marked.
- 7. Packet 59 The EVM configured as "preferred Host" issues a VConn swap. The PD spec requires that a PD port must provide power to the connection cable in order to issue a cable reset. This VConn swap request is preliminary to the cable reset of packet 65.
- 8. Packets 61 and 63 The VConn swap is accepted and then the EVM configured with preferred Host

issues a PS Ready command when it is providing power to the cable.

9. Packets 65 through 70 — The host-configured port issues a *Cable Reset* command. Because the cable is not e-marked, it does not return a *Good CRC* message to this *Cable Reset* (all *Good CRC* messages have been removed from this trace to reduce its size). When no *Good CRC* message is received from the cable, the DFP (host) issues one soft reset and three retries to the cable as a result of not receiving *Good CRC* for the soft reset request. After four *Soft Reset* requests with no *Good CRC*, the port issues one final *Cable Reset* and then continues with the rest of its PD negotiation (not shown).

# 4 Requirements for Data and Power Role Swaps

A number of conditions must be met for the TPS6598x USB PD controller issues or accepts a power or data role swap. If a swap request is not issued or accepted as you expect, these conditions should be checked.

 Table 1 summarizes the requirements for each type of swap to be issued or accepted. The combination of conditions in the *Required Conditions* column must be met as specified in the table for the swap to occur.

 If any of the conditions in the *Blocking Conditions* column are met, the swap does not occur.

ACTION	TYPE	REQUIRED CONDITIONS	BLOCKING CONDITIONS
Issue swap to source Power		Port is currently a Sink AND Initiate Swap to Source == 1 OR SWSr 4CC command issued	A previous swap-to-source request was NAK'd by the far-end PD port controller. Dead Battery flag is set in the Boot Status register (0x2D). The <i>Port Information</i> field in the System Configuration register does not support PR swap.
Accept swap to source Power		Port is currently a Sink AND Process Swap to Source == 1	The <i>Port Information</i> field in the System Configuration register does not support PR swap. Dead Battery flag is set in Boot Status register (0x2D).
Issue swap to sink	Power	Port is currently a Source AND Initiate Swap to Sink == 1 OR SWSk 4CC command issued	A previous swap-to-sink request was NAK'd by the far-end PD port controller. The <i>Port Information</i> field in the System Configuration register does not support PR swap.
Accept swap to sink	Power	Port is currently a Source AND Process Swap to Sink == 1	The <i>Port Information</i> field in the System Configuration register does not support PR swap.
Issue swap to DFP	Data	Port is currently a UFP (Device) AND Issue Swap to DFP == 1 OR SWDF 4CC command issued	A previous swap-to-DFP request was NAK'd by the far-end PD port controller. The <i>Port Information</i> field in the System Configuration register does not support DR swap. An Alternate Mode is Active (has been entered and not exited). A Source or Sink Capabilities message has been received from port partner that does not have Dual Role Data bit set.
Accept swap to DFP	Data	Port is currently a UFP (device) AND Process Swap to DFP == 1	The <i>Port Information</i> field in the System Configuration register does not support DR. An Alternate Mode is Active (has been entered and not exited).
Issue swap to UFP	Data	Port is currently a DFP (Host) AND Initiate Swap to UFP == 1 OR SWUF 4CC command issued	A previous Swap to UFP request was NAK'd by the far-end PD port controller. The <i>Port Information</i> field in the System Configuration register does not support DR. An Alternate Mode is active (has been entered and not exited). A source or sink capabilities message has been received from port partner that does not have Dual Role Data bit set.
Accept swap to UFP	Data	Port is currently a DFP (Host) AND Process Swap to UFP == 1	The <i>Port Information</i> field in the System Configuration register does not support DR. An Alternate Mode is Active (has been entered and not exited).

#### Table 1. Data-Role and Power-Role Swap Requirements

## 5 Verification of Data-Role and Power-Role Swaps

The first step in verification of the data-role and power-role swaps is to verify that the settings read from the device match those that were input into the configuration tool. The relevant settings are stored in the Control Configuration register (0x29) and the System Configuration register (0x28). These settings can be modified at runtime by an external microcontroller and therefore ensuring that the settings read as expected is useful.



Verification of Data-Role and Power-Role Swaps

lings Debug Documents H	eip				
neral Settings Device 1, port	0				
nfiguration Registers Debug	Registers Commands	Scripting			
Debug Mode			Polling	nected )x38 (I2C2)	
ustomer Use terrupt Mask for I2C1 terrupt Mask for I2C2		Port Control (0x29)			
Slobal System Configuration		Field	Value		
ort Configuration		Type-C Current	3 A (strongest pullup)	•	
ort Control ransmit Source Capabilities		PD Mode	Normal PD Behavior	-	
ansmit Sink Capabilities		Process Swap To Sink			
tonegotiate Sink		Initiate Swap To Sink			
ernate Mode Entry Queue 3 Configuration Register		Process Swap To Source	Y		
ent Delay		Initiate Swap To Source	Y		
ansmit Identity Data Object		Process VCONN Swap			
ser Alternate Mode Config splay Port Capabilities		Process Swap to UFP			
tel VID Config Register		Initiate Swap to UFP			
PI VID Configuration		Process Swap to DFP	V		
) Config etimer Debug Register		Initiate Swap to DFP			
pp Config Binary Data Indices		Automatic ID Request	V		
C Master Configuration		Force USB Generation 1			
op configuration Register eep Control Register		Externally Powered			
Manufacturer Info SOP		Automatic Sink Cap			
Source Capabilities Extended	I Data Block	Sink Control Bit			
Battery Capabilities Manufacturer Info SOP Prime		15 kOhm Resistor Present			
		Data Contact Detection Enable			
		Charger Advertise Enable	Charger Advertise Disabled	2	
		USB Disable			

Figure 6. Port Control Register "preferred\_Source"

The settings shown in Figure 6 are verified to match those of the configuration tool as shown in Figure 4. Even when this is the case, you may find cases where swaps do not occur as expected. This section provides two common examples (see Section 5.1 for example 1 and Section 5.2 for example 2) and a walkthrough of a typical debug procedure for these scenarios using the TPS6598x Configuration Tool.

## 5.1 Example 1: Debugging Power Role Swap Exiting Dead Battery Mode Operation

For the first experiment, use the two TPS65987 EVMs programmed as *preferred Source* and *preferred Host* settings from the earlier example. The *preferred Source* EVM is left unpowered, while the *preferred Host* EVM is powered.

As shown in Figure 7, no power-role swap is initiated by the *preferred Source* system, even though it is a sink and has *Initiate Swap to Source* enabled.

	Packet	Right		PD Mag		R PF			Cnt			Voltage Dual Rol	e Fixed		/oltage Dua	
14	32	"Right"			Source Cap D	FP SR			2	3.0	0 A	5.00 V 1		3.00 A 1	2.00 V	0 765.776
•	Packet	Left	SNK	PD Mag	Mag Type DR		Magi	_	Ont Rec					Cap Misma		
ā.	34	"Left"			Request UF	SNK	0	1		3.	/ A00	75.00W 3.00A /	75.00W	0	1	636.363 us
	Packet	Right	SRC $\xrightarrow{SP}$	PD Mag	Mag Type DR	PR	Mag		Cnt	Duration		Time	Time S	tamp		
E I	36	"Right"	and -	PD Mag	Accept DF	SRC	1	0	4	98.256 us	1	30.947 ms	3.0015	26 000		
	Packet	Right	509	•	Mag Type DR	PR	Mag		Cnt	Duration		Time	Time S	tamp		
8	38	"Right"	SRC 🚔	PD Mag	PS Ready DFI	_		0		98.256 us		11.433 ms	3.0324			
	Provide t	Dista									-		and To			
<u>e</u> -	Packet 40	Right "Right"	SRC	PD Mag	Msg Type Vendor Defined	DR DFP	PR SRC	Mag ID 3	Obj Cnt 1	VDM H	eader	Cmd Discover identity	-	pe Obj Pos r 0	PD SID	Duration 632.016 us
-	40	rogin			Vendor Denned			-				Discover identity	/ minato	· · ·	10000	002.010 08
0	Packet	Left	SNK	PD Msg	Mag Type	DR		Mag ID		VDM H	eader	Cmd	-	pe Obj Pos	-	ID Header
ē.	42	"Left"			Vendor Defined	UFP	SNK	1	4			Discover Identity	Resp AC	к 0	PD SID	Texas
0	Packet	Right		PD Msg	Mag Type	DR	PR	Mag ID	Obj Cnt		aadar	Cmd	Cmd Typ	e Obj Pos	Vendor ID	Duration
ă.	44	"Right"		PD Mag	Vendor Defined	DFP	SRC	4	1	VDM H	eauer	Discover SVIDs	Initiator	0	PD SID	632.016 US
	Packet	Left	509	Þ	Msg Type	DR	PR	Mag ID	Obl Cnt	Þ		Cmd	Cmd Typ	e Obj Pos	Vendor ID	SVID 0
8	46	"Left"	📛 SNK	PD Mag	Vendor Defined		SNK	2	3	VDM H	eader				PD SID	SVIDs Display Pc
		- Class										0.000				
<u>e</u> -	Packet 48	Right "Right"	SRC 🌥	PD Msg	Msg Type Vendor Defined	DR DFP	PR SRC	Mag ID 5	Obj Cnt	VDM H	eader	Cmd Discover Modes	Cmd Typ Initiator		Vendor ID Display Po	
-	40	rogin				DFP	and	~				Discover modes			Display Po	032.010 08
0	Packet	Left	SNK	PD Mag	Mag Type	DR			Obj Cnt		eader	Cmd		e Obj Pos	Vendor ID	DP Cap
۵.	50	"Left"			Vendor Defined	UFP	SNK	3	2			Discover Modes	Resp AC	K 0	Display Por	t UFP_
	Packet	Right		PD Mag	Msg Type	DR	PR	Mag ID	Obj Cnt	VDM H	onder	Cmd	Cmd Typ	e Obj Pos	Vendor	ID Durat
ă,	52	"Right"	and —	PD Mag	Vendor Defined	DFP	SRC	6	1	VDM H	eauer	Discover Modes	Initiator	0	Texas Instr	uments 632.01
	Packet	Left	509	Þ	Mag Type	DR	PR	Mag ID	Obj Cnt	Þ		Cmd	Cmd Typ	e Obj Pos	Vendor	ID
2	54	"Left"	📛 SNK	PD Mag	Vendor Defined			4	2	VDM H	eader	Discover Modes			Texas Instr	M odes
						·							-			
•	64 Packets	CBL	PD Msg	Mag Ty		_	-	obj Cnt	VDM H	eader				vendor		Contraction of the Contraction of the Contraction
Δ.	56-119		H	Vendor De	fined DFP or U	P	0	1		Dis	cover	r Identity Initiato	or 0	PD SI	632.0	16 us 113.876
0	Packet	Right		PD Mag	Mag Type	DR		Mag ID	Obj Cnt	VDM H	eader		d Type O		ndor ID	Duration
Ē.	120	"Right"			Vendor Defined	DFP	SRC	7	1			Enter Mode In	itiator	1 Dis	play Port	632.016 us
	Packet	Left	50 <sup>9</sup>	•	Msg Type	DR	PR	Mag ID	Ob  Cnt	•		Cmd Cm	d Type O	D Pos Ve	ndor ID	Duration
2	122	"Left"	SNK 📫	PD Meg	Vendor Defined	UFP	SNK	5	1	VDM H	eader		P ACK			636.363 us
	Packet	Right		•	Maa Tuno	DR	PR	Mag ID	Obj Cnt	•		Cmd	Cred Tu	pe Obj Por	S Vendor II	
8-	124	"Right"	SRC -	PD Msg	Misg Type Vendor Defined		SRC	0	2	VDM H	eader	DP Status (0x10			Display Po	DP Status
						_		-	_							
0	Packet	Left	SNK 🚧	PD Mag	Misg Type	DR		Mag ID	Obj Cnt 2	VDM H	eader	Cmd		pe Obj Pos		DP Status
<u> </u>	126	"Left"			Vendor Defined	UFP	SNK	6	4			DP Status (0x10	, Resp Ac	<mark>ск</mark> 1	Display Po	UF UF
0	Packet	Right		PD Mag	Mag Type	DR		Mag ID	Obj Cnt	VDM H	eader	Cmd		Type Obj		DP Contia
Ē	128	"Right"			Vendor Defined	DFP	SRC	1	2			DP Configure (0)	x11) Initi	ator 1	Display	Port
	Packet	Left		<b>•</b>	Mag Type	DR	PR	Mag ID	Obj Cnt			Cmd	Cmd	Type Obj i	Pos Vendo	r ID Duration
2	130	"Left"	SNK	PD Mag	Vendor Defined	UFP	SNK	7	1	VDM H	eader	DP Configure (0)	(11) Resp			Port 632.016 u
	Packet	Right	522	•	Mag Type	DR	PR	Mag ID	Obj Cnt	•		Cmd Cm	d Type O	bl Pos	Vendor ID	
8	132	"Right"	SRC 并	PD Mag	Vendor Defined		SRC	2	2	VDM H	eader		itiator		as Instrume	nts Undefined Ox
	Berlint							-								
0	Packet 134	Left "Left"	🚢 snk	PD Mag	Msg Type Vendor Defined	DR UFP	PR SNK	Mag ID 0	Obj Cnt	VDM H	eader		d Type OI		Vendor ID as Instrumer	Duration hts 636.363 us
-	104	cen			venuor Denneo		SINK	•	-			Citter Mode rikes	P ACK	i liex	ae metrumer	1000.000 US
0	Packet	Right		PD Mag	Mag Type	DR		Mag ID		VDM H	eader	Cmd		Cmd Type		Vendor ID
E.	136	"Right"			Vendor Defined	DFP	SRC	3	2			SVID Specific C	md (0x14)	Initiator	1 T	exas instruments
0	Packet	Left	📛 SNK	PD Mag	Mag Type	DR	PR	Mag ID	Obj Cnt		ander	Cmd		Cmd Type	Obj Pos	Vendor ID
H	138	"Left"	SNK	PD mag	Vendor Defined	UFP	SNK	1	2	VOM H	eauer	SVID Specific Cr	md (0x14)	Resp ACK	1 T	exas Instruments

Figure 7. PD Flow With DRP Source Unpowered

If the system settings have been verified, but a data-role or power-role swap is not occurring as expected, initiate the role swap manually through the TPS6598x Configuration Tool.

Because the *preferred Source* EVM is not issuing the expected swap request, use debug mode on the TPS6598x configuration tool to this EVM and issue the SWSr command.

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ttings Debug Documents Help eneral Settings Device 1, port 0	
nfiguration Registers Debug Registers Commands	Polling Connected Aardvark, 0x38 (I2C1)
H Firmware Update Hit Firmware Update Raw Register Write Deadattery Flag Clean Abot Abot Wam Retailor Di lard Reset Cable Reset Get Surce Capabilities Get Surce Capabilities Send Source Capabilities Send Source Capabilities Send Source Capabilities Send Source Capabilities Send Request Data Object Swap to Sink Wamp Voon Provider System Resety to Sink Power Enter Alternate Mode Exit Alternate Mode Send Souput Send Souput Set GPPO Low Send VDM Packet ADC Read	Swap to Source (SWSr) Execute SWSr [Clear Output] Execute Status: Output: Task Return Status ABORT_CMD

Figure 8. Failed SWSr When Dead Battery flag is Set to 1 (True)

Figure 8 shows the feedback from the host interface tools. The tool reports that the SWSr command was aborted. You can read Boot flags register (0x2D) to check if the Dead Battery Flag is set.

To correct this, you can power the board and then issue the DBfg command from the host interface which clears the Dead Battery flag as shown in Figure 9. Clearing of the Dead Battery flag should also be verified by reading the Boot Status register (0x2D) as shown in Figure 10.

The board must be powered before clearing the Dead Battery flag otherwise the device resets and reboots again in Dead Battery Mode operation.

eneral Settings Device 1, port 0 onfiguration Registers Debug Registers Commands	Scripting
Debug Mode	Poting Aardvark, 0x38 (I2C1
H Firmware Update Vare Register Read Vare Register Write Dealobattery Flag Clear Abort Varem Rebool Cool Rebool Co	Deadbattery Flag Clear (DBfg) Execute DBfg Clear Output Execute Status: Output: Task Return Status SUCCESS_CMD

Figure 9. Successful DBfg Command to Clear Dead Battery Flag



ings Debug Documents Help		
neral Settings Device 1, port 0 Inflauration Registers Debug Registers Comm		
nfiguration Registers Debug Registers Comm	ands Scripting	
Debug Mode		Polling
Bebug mode		Aardvark, 0x38 (I2C
	A DE LA DE LA DELLA DE LA DELLA DE LA DELLA D	
lode	Boot Flags (0x2d)	
resion		
itatus loot Flags	Field	Value
Build Identifier	Boot Successful	False
Device Info	PP_EXT Switch Closed	True
Received Source Capabilities Received Sink Capabilities	Dead Battery Flag	False
active Contract PDO	SPI Flash Present	True
ctive Contract RDO	Region 0	True
sink Request RDO Power Status		False
PD Status	Region 1 Region 0 Invalid	False
leceived SOP Identity Data Object		False
Received SOP Prime Identity Data Object	Region 1 Invalid	Faise
X Attention structured VDM X VDM Register	Region 0 Flash Error	Faise
Data Control Register	Region 1 Flash Error Reed Solomon Error	False
Iser VID Status Register	LART CRC Fail	False
P SID Status ntel VID Status		False
1 VID Status Register	Region 0 CRC Fail	
Data Status	Region 1 CRC Fail	False
X User VID Attention VDM Register X User VID Other VDM Register	Customer OTP Invalid	False
ype C State Register	2C OTP Bits	0x1
SPIO Status Register	App Customization Version Error	False
	App Customization Length Error	False
	App Customization CRC Check Error	False
	DBG_CTL Bits	0x0
	I2C_ADDR Bits	0x0
	UART Boot	False

Figure 10. Verified Dead Battery flag Cleared to 0 (False)

When the Dead Battery flag has been cleared, the EVM programmed as *preferred Source* can be swapped to the power source by issuing the SWSr host interface command as shown in Figure 11.

eneral Settings Device 1, port 0 onfiguration Registers Debug Registers Con	nmands Scripting
Debug Mode	Poling Aardvark, 0x38 (I2C1
HI Firmware Update Rar Register Weide Rar Register Weide Rar Register Weide Rar Register Weite Ras Register Weite Reset Codd Reteool Do Hard Reset Ged Sink Capabilities Ged Sink Capabilities Ged Sink Capabilities Send Regist Sang to Dank S	Swap to Source (SWSr) Execute SW3r Clear Output Execute Status: Output: Task Return Status SUCCESS_CMD

Figure 11. Successful Swap to Source



#### 5.2 Example 2: Debugging Swap Reversal from non-Persistent Swap Conditions

Using the TPS65987 EVMs programmed as *preferred Source* and *preferred Host* settings from the earlier example, the host interface tools may be used to issue a power-role swap.

Taking the lesson learned from Section 5.1, power both EVMs and then connect. The PD flow should be as was already shown in Figure 5.

As a next step, use the host interface tool to issue a Swap to Sink PD message to the port partner.

Application Customization Tool		
ttings Debug Documents Help		
eneral Settings Device 1, port 0		
configuration Registers Debug Registers Comma	nds Scripting	
Debug Mode		Poiling Aardvark, 0x38 (I2C1)
HI Firmware Update Raw Register Read Raw Register Write	Swap to Sink (SWSk)	Execute SWSk Clear Output
Adv Register Vitie Deadbattery Flag Clear Abort Warm Reboot Cold Reboot PD Hard Reset	Execute Status:	Execute Swork, Great Output
Cable Reset Get Sink Capabilities Get Source Capabilities Send Source Capabilities	Output: Task Return Status SUCCESS_CMD	
Send Request Data Object Swap to Sink Swap to Source		
Swap to DFP Swap to UFP Swap VConn Provider		
System Ready to Sink Power Enter Alternate Mode Exit Alternate Mode Autonegoliate Sink		
Start Alternate Mode Discovery Enable GPIO as Input Enable GPIO as Output Set GPIO High Set GPIO Low		
Send VDM Packet ADC Read		

Figure 12. SWSk Command Page Before Execution

Figure 12 shows the command page for the SWSk (swap to sink) host interface command. The tools are attached to the EVM that have been configured with *preferred Source*, which comes up as the power source always if it has the *try.SRC* feature enabled.

Before issuing SWSk, the PD Status register, displayed at the bottom of the command page, shows that the system is currently the power source (*Source-Sink* field).

After pressing the *Execute Function* button, the tool indicates a successful execution as shown in Figure 13; however, the PD Status register still indicates that the device is the power source, just as it was before issuing the SWSk command. This scenario is referred to as a *swap reversal* which is an accidental scenario that arises from configuring the TPS65987 device with non-persistent swap conditions.



eneral Settings Device 1, port 0			
Debug Mode	s Scripting	Poiling Aardvark, 0x38 (I2C1	
Mode Version Status	Power Status (0x3f)		
Boot Flags	Field	Value	
Build Identifier Device Info	Offer Priority	Connection Present	
Device Info Received Source Capabilities	Source or Sink	Source	
Received Sink Capabilities	Type-C Current	PD Contract Negotiated	
Active Contract PDO	BC 1.2 Detection	USB BC v1.2 connection not yet established	
Active Contract RDO Sink Request RDO	BC 1.2 Status	SDP Detected	
Power Status			
PD Status Received SOP Inter identity Data Object Received SOP Prime identity Data Object RX VDM Register Data Control Register User VID Status Register Data Status miel VID Status Register Data Status VID Status Register Data Status RUS VID VID Register RV User VID Cher VID Register Type C Status Register OPIO Status Register			

Figure 13. SWSk Power-Role Swap to Sink Attempt (Inconclusive Result)

As shown in Figure 13, the host interface tool reports a successful completion of the *Swap to Source* command, but the Power Status register reports that the device is still a source. The reason that the device is still a source after a *Swap to Sink* command that is reported as successful is shown in Figure 14. This PD capture is started at the point in which the SWSk command is issued from the host interface tool. The trace shows that, in fact, a successful *Swap to Sink* PD message sequence operation does occur (packets 1 through 15); however, the system immediately issues another swap request. The reason is shown by revisiting the Port Control register on the device programmed as *preferred Source*.

Packet Left SRC # PD Msg Msg Type DR PR Msg ID Obj Cnt	Duration Time Time Stamp
PR Swap OPP SRC 6 0	501.683 us         1.208 ms         17 . 943 041 000           Duration         Time         Time Stamp
Packet         Right         SNK         PD Msg         Msg Type         DR         PR         Msg ID         Obj Cnt           1         3         "Right"         SNK         5         0	Duration         Time         Time Stamp           498.256 us         32.400 ms         17 . 944 249 000
Packet         Right         PD         Msg Type         DR         PR         Msg ID         Obj Cnt           0         5         "Right"         SNK         PD Msg         PS Ready         UFP SNK         7         0	Duration         Time         Time Stamp           494.949 us         2.647 ms         17.976 649 360
Packet         Left         SRC ➡         PO Mag         Msg Type         DR         PR         Msg ID         Obj Cnt           0         7         "Left"         SRC ➡         PD Mag         PS Ready         DFP SRC 6         0	Duration         Time         Time Stamp           498.256 us         25.808 ms         17 . 979 296 000
Packet         Left         SRC         PD Msg         Msg Type         DR         PR         Msg ID         Obj Cr           9         "Left"         SRC         PD Msg         Source Cap         DFP         SRC         0         2	Preed         Max Cur Voitage         Dual Role         Preed         Max Cur Voitage         Dual Role         Duration         Time           3.00 A         5.00 V         1         Preed         3.00 A         12.00 V         0         765.776 us         1.633 ms
PD Meg Meg Type DR PR Meg ID Obj Cnt 11 "Right" SNK PD Meg Request UFP SNK 0 1	Max Opr Cur/Pow         Opr Cur/Pow         Cap Mismatch         Obj Pos         Duration         Time         Time           3.00A / 75.00W         3.00A / 75.00W         0         1         636.363 us         1.337 ms         18.0
PD Mag Mag Type DR PR Mag ID Obj Cnt 13 "Left" SRC + PD Mag Mag Type DR PR Mag ID Obj Cnt Accept DFP SRC 1 0	Duration         Time         Time Stamp           499.256 us         30.952 ms         18 . 008 074 000
PD Mag Mag Type DR PR Mag ID Obj Cnt. 15 "Left" SRC PD Mag Mag Type DR PR Mag ID Obj Cnt. PS Ready DFP SRC 2 0	Duration         Time         Time Stamp           499.256 us         1.403 ms         18 . 039 026 000
PD Meg Meg Type DR PR Meg ID Obj Cnt 17 "Right" SNK PD Meg Meg Type DR PR Meg ID Obj Cnt PR Swap UFP SNK 1 0	Duration         Time         Time Stamp           503.322 us         1.205 ms         18 . 040 429 000
PD Mag Mag Type DR PR Mag ID Obj Cnt 19 "Left" SRC **** PD Mag Mag Type DR PR Mag ID Obj Cnt Accept DFP SRC 3 0	Duration         Time         Time Stamp           499.256 us         31.547 ms         18 . 041 634 000
PD Mag Mag Type DR PR Mag ID Obj Cnt 21 "Right" SNK PD Mag PS Ready DFP SNK 4 0	Duration         Time         Time Stamp           491.568 us         2.626 ms         18 . 073 181 344
PD Mag Mag Type DR PR Mag ID Obj Cnt. 23 "Left" SRC PD Mag Mag Type DR PR Mag ID Obj Cnt. PD Mag VIPP SRC 2 0	Duration         Time         Time Stamp           501.683 us         5.394 ms         18.075 807 000
PD Meg Type Cable Plug Meg ID Obj Cnt, Dura 25 CBL PD Meg Meg Type Cable Plug Meg ID Obj Cnt, Dura Soft Reset DFP or UFP 0 0 501.6	ation I die Time Stamp 83 us 1.137 ms 18 . 081 201 000
PD Meg Msg Type Cable Plug Msg ID Obj Cnt, Dura 26 PD Meg Soft Reset DFP or UFP 0 0 501.6	
PD Meg Meg Type Cable Flug Meg ID Obj Cnt. Durr 27 CBL PD Meg Soft Reset DFP or UFP 0 0 501.6	ation I die Time Stamp 83 us 1.138 ms 18.084 479 000
PD Msg Type Cable Plug Msg ID Obj Cnt. Durr 28 CBL PD Msg Soft Reset DFP or UFP 0 0 501.6	ation I Gile Time Stamp 83 us 1.274 ms 18.086 119 000
0         4 Packets         ∞1         CBL         PD Msg         Msg Type         Cable Plug         Msg ID         Obj Cnt         VD           0         29-32         CBL         PD Msg         Vendor Defined         DFP or UFP         1         1	Cmd         Cms Type         Obj Pos         Vendor ID         Duration         Time         Time         Time         Time         Stamp           Discover identity         Initiator         0         PD SID         638.442 us         27.812 ms         18.087 895 00
Packet         Left         SRC ➡         PD Msg         Msg Type         DR         PR         Msg ID         Obj Cr           1         33         "Left"         SRC         ➡         PD Msg         Msg Type         DR         PR         Msg ID         Obj Cr	Prxed         Max Cur         Voitage         Dual Role         Prxed         Max Cur         Voitage         Dual Role         Prxed         Max Cur         Voitage         Dual Role         Max Cur         Voit
Packet         Right         SNK         PD Meg         Msg Type         DR         PR         Msg ID         Obj Cnt           35         "Right"         SNK         PD Meg         Request         DFP SNK         0         1	Max Opr Cur/Pow         Opr Cur/Pow         Cap Mismatch         Obj Pos         Duration         Time         Time           3.00A / 75.00W         3.00A / 75.00W         0         3         632.016 us         1.337 ms         18.1
PO Mag Mag Type DR PR Mag ID Obj Cnt 37 "Left" SRC **** PD Mag Mag Type URP SRC 1 0	Duration         Time         Time Stamp           501.683 us         32.020 ms         18 . 118 846 000
Policity SRC 2 0 0 000 CnL 39 TLeft SRC 2 0	Duration Time Stamp 501.633 us 18150.886.000

Figure 14. PD Trace of Manual Power-Role Swap Followed by Automatic Power-Role Swap

Referring back to Figure 6, recall that the source device has the *Initiate Swap to Source* setting enabled. The behavior of this setting is that it initiates a *Swap to Source* request at any time that the device is a sink and none of the blocking conditions of Table 1 are present. So, in this system, when the manual swap requests swaps power roles, the *Initiate Swap to Source* setting immediately swaps the power role back. In fact, any number of *Swap to Sink* requests are immediately swapped back as long as this setting is enabled.



onfiguration Registers					
	Debug Registers	Commands	Scripting		
Debug Mode				Polling	nected 1x38 (12C2
Customer Use Interrupt Mask for I2C1			Port Control (0x29)		
Interrupt Mask for I2C2 Global System Configu			Field	Value	
Port Configuration			Type-C Current	3 A (strongest pullup)	
Port Control Transmit Source Capal			PD Mode	Normal PD Behavior	
ransmit Source Capal ransmit Sink Capabilit			Process Swap To Sink		
Autonegotiate Sink Autonegotiate Sink Autonegotiate Sink Event Delay Vent Delay User Alternate Mode Config Userjaker Port Capabilities User Alternate Mode Config Userjaker Port Capabilities MIP VID Config Register MIP VID Config Register App Config Invary Data Indices 120 Autone Register Sheep Confio Register The Manufacturer Info SOP Th Source Capabilities Etended Data Block Th Sattery Capabilities			Initiate Swap To Sink	6	
		Process Swap To Source	y.		
			Initiate Swap To Source	6	
			Process VCONN Swap	2	
		Process Swap to UFP	2		
		Initiate Swap to UFP			
		Process Swap to DFP	N		
		Initiate Swap to DFP			
		Automatic ID Request	2		
		Force USB Generation 1			
		Externally Powered			
			Automatic Sink Cap	V	
			Sink Control Bit	6	
			15 kOhm Resistor Present	6	
			Data Contact Detection Enable	6	
			Charger Advertise Enable	Charger Advertise Disabled	
			USB Disable		

Figure 15. "preferred Source" With InitSwapToSource Disabled

A simple means of completing this test is to use the host interface tools to disable *Initiate Swap to Sink* in the Control Configuration register (0x29) of the EVM that has been configured with *preferred Source*.

**NOTE:** Register changes made with the host interface tools are made only in the device RAM, not the system FLASH, and is therefore reset back to their default values if there is a device reset or power cycle.

Do not forget to click the Write Register button after making this change.

The *Process Swap to Sink* field does not need to be enabled for the SWSk command to work properly. This field is only used to evaluate swap requests that are initiated by the port partner.

neral Settings Device 1, port 0		
nfiguration Registers Debug Registers Comm	ands Scripting	
		connected
Debug Mode		Polling
		Aardvark, 0x38 (I2C1
	-	
tode /ersion	Power Status (0x3f)	
tatus		
loot Flags	Field	Value
uild Identifier	Offer Priority	Connection Present
evice Info eceived Source Capabilities	Source or Sink	Sink
eceived Sink Capabilities	Type-C Current	PD Contract Negotiated
ctive Contract PDO	BC 1.2 Detection	USB BC v1.2 connection not vet established
ctive Contract RDO ink Request RDO	BC 1.2 Status	SDP Detected
ower Status		
D Status		
teceived SOP Identity Data Object		
teceived SOP Prime Identity Data Object		
IX Attention structured VDM IX VDM Register		
ata Control Register		
Iser VID Status Register		
P SID Status		
Itel VID Status		
I VID Status Register ata Status		
X User VID Attention VDM Register		
IX User VID Other VDM Register		
ype C State Register		
PIO Status Register		

Figure 16. Manual Swap to Sink (Successful and Persistent)



Verification of Data-Role and Power-Role Swaps

Figure 16 shows the successful completion of the SWSk host interface command after disabling *Initiate Swap to Source* field in Control Configuration register (0x29). The Power Status register now shows the device is the power sink in the connection.

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