

# **TPS6598x OCP Mechanism and Programming Guide**

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## ABSTRACT

This document describes the functionality of the overcurrent protection (OCP) mechanism of the TPS6598x device, and how to program it using the *Application Customization Tool*. This guide defines THE peak current and provides steps on how to set the threshold of OCP on the TPS6598x device.

**NOTE:** This tool replaces the TPS6598x Application-Customization Tool; therefore, TI recommends using this tool to receive the latest firmware and features.

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Introduction

## 1 Introduction

The TPS6598x family of devices can be configured to set the OCP threshold of the device. Upon an OCP trip, the device sends out a command to discharge the voltage on VBUS.

## 1.1 Related Documents

- TPS65988 Dual Port USB Type-C & USB PD Controller, data sheet
- TPS65981, TPS65982, and TPS65986 Host Interface Technical Reference Manual

## 1.2 Hardware

The required hardware follows:

- Windows®-based PC with at least one USB 2.0 (or later) port
- TPS6598x-EVM
- Barrel jack, laptop charger, power-supply AC adapter (20 V)
- USB Micro-B to USB Standard-A cable (for the USB2.0 low-speed endpoint [USB EP] option)
- TotalPhase Aardvark USB-to-SPI/I2C Host adapter + USB standard-B to -A cable + jumper wires or LaunchPad<sup>™</sup> EVM to Aardvark adapter (for the Aardvark option)

**NOTE:** Only one of the two adapter options is required: TotalPhase Aardvark or USB Micro-B to USB Standard-A cable. The hardware and setup are different depending on the adapter selected.

## 1.3 OCP Mechanism

The OCP mechanism is primarily set by application firmware. The ILIMPPHV register is configured so that currents which exceed the ILIMPPHV set point over an extended time result in an OCP fault in the system.

**NOTE:** The TPS6598X Application Customization Tool GUI sets the OCP limit as a hard-set value and does not follow the USB PD peak current specifications for variable overload capabilities in the USB PD document, Section 6.4.1.2.3.6. This means that the maximum current and peak current percentage together create the overall OCP threshold.

## 1.4 Recommended Default Settings

When using the TPS65988EVM, the base firmware in the Application Customization Tool automatically sets Peak Current to 100% and the Overcurrent Timeout to 1.28 ms.



# 2 Using the TPS6598x Application Configuration Tool Startup

See the Application Customization Tool User's Guide for the basics on start-up using the Application Configuration Tool.

# 3 Setting OCP Threshold on the TPS6598x

## 3.1 Setting OCP Peak Current Threshold

After the desired firmware is selected, use the following instructions to set the desired OCP threshold. 1. Click on the desired port to be programmed (Device 1, port X), as shown in Figure 1.

TDCCEOQUA-		e 1, port 1		
TE 30396X Ap	plication Customiz	ation Tool	TPS65988_rom1; TPS65988 EVM,	02_DRP_Full_3p02 version 3.02
Firmware Base In	nage (Low-region binary fi	le)		
Change File	tps65987 8 f307 08 pt	0.06 bin		
Firmware Version	n: 1307.8.6 iguration Available: 0x800			
	iguration Available: 0x800			
Device Initializatio	-			
Device millanzario	on Chain			
Number of Con	nected Devices: 1 🔻		Share Settin	gs Across All Channels:
	Device	Ports	Pin Strapping	
		Port1 (0x0)		Port1 I2C1: 0x20
Device 1			I2C_ADDR	Port1 I2C2: 0x38
Derice 1		Port2 (0x0)	0 (R1/R2 = 0.00-0.18) -	Port2 I2C1: 0x24
		No. 22 Address Address Address		Port2 I2C2: 0x3f

Figure 1. Main Window of TPS6598x Application Configuration Tool



#### Setting OCP Threshold on the TPS6598x

2. Navigate to either Transmit Source Capabilities or Transmit Sink Capabilities, depending on the intended use case (see Figure 2).

eral Settings Device Settings Device 1, por			
TPS6598x Application (	Customization Tool	TPS65988_rom1p TPS65988 EVM, v	
ustomer Use		000 000000	
terrupt Mask for I2C1	Active PDO Bank Follows EP		
terrupt Mask for I2C2 ystem Power State	Transmit Source Send Pending		
ort Configuration of Control ransmit Source Capabilities ransmit Sink Capabilities utonegotiate Sink ternate Mode Entry Queue 02 Configuration Dedictor	Number of Bank 0 Source PDOs 1 Source PDO 1		
D3 Configuration Register ransmit Identity Data Object	Field	Value	
ser Alternate Mode Config isplay Port Capabilities	Switch Source	PP1 sources this PDO	
tel VID Config Register	Maximum Current	3A	
exas Instruments VID Config	Voltage	5 V	
pp configuration Register	Peak Current	100%	
C SS Mux Control Register W control Register	Unchunked Extended Msg Supported		
eep Control Register	USB Capable		
Manufacturer Info SOP	USB Suspend Supported		
x Source Capabilities Extende x Battery Capabilities	Supply Type	Fixed Source	
x Manufacturer Info SOP Prim aw View			
	Bank 1 Settings Number of Bank 1 Source PDOs		
	0		

Figure 2. Transmit Source Capabilities Window

3. Click on the Peak Current drop-down box to configure the settings for the desired application (see Figure 3).

Source PDO 1	
Field	Value
Switch Source	PP1 sources this PDO
Maximum Current	3A 👻
Voltage	5 V
Peak Current	100%
Unchunked Extended Msg Supported	100% 130%
USB Capable	150%
USB Suspend Supported	200%
Supply Type	Fixed Source

Figure 3. Peak Current Configuration Drop-down

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## 3.2 Setting OCP Timeout Limit

The following instructions provide details on setting the desired OCP Timeout limit:

1. Navigate to Global System Configuration to configure the intended Overcurrent Timeout value. The drop-down box allows for multiple time-out configuration settings (see Figure 4).

			ersion 3.06
ustomer Use terrupt Mask for I2C1	Global System Configuration (0x27)		
terrupt Mask for I2C2	Field	Value	
obal System Configuration	PP Cable 1 Switch Config	PP Cable Switch as Output, Guaranteed 4.5-5.5V	
ort Control	PP Cable 2 Switch Config	PP Cable Switch as Output, Guaranteed 4.5-5.5V	
	PP 1 Switch Config	PP Switch as Source Only (Output)	
ansmit Sink Capabilities tonegotiate Sink	PP 2 Switch Config	PP Switch as Source Only (Output)	
ternate Mode Entry Queue	PP 3 Switch Config	PP Switch as Sink Only (Input)	
3 Configuration Register ansmit Identity Data Object	PP 4 Switch Config	PP Switch as Sink Only (Input)	
er Alternate Mode Config	87 Emulation Mode	2	
splay Port Capabilities	PP1 Switch to VBUS Map	VBUS 1	
el VID Config Register xas instruments VID Config	PP2 Switch to VBUS Map	VBUS 2	
) Config	PP3 Switch to VBUS Map	VBUS 1	
p configuration Register C SS Mux Control Register	PP4 Switch to VBUS Map	VBUS 2	
V control Register	PP Switch 1 Overcurrent Timeout	1.28 ms	
ep Control Register Manufacturer Info SOP	PP Switch 1 Overcurrent Timeout Enable	10 us 20 us	
Source Capabilities Extende	PP Switch 2 Overcurrent Timeout	80 us	
Battery Capabilities Manufacturer Info SOP Print	PP Switch 2 Overcurrent Timeout Enable	160 us 640 us	
w View	Multiport Sink Policy	1.28 ms	
	Sink Policy Non-overlap Time	6.12 ms 10.24 ms	
	Multiport Alternate Mode Policy	40.96 ms 81.92 ms	
	TBT Controller I2C Port	1201	
	I2C Timeout	15	
	SPI Read Only		

Figure 4. Global System Configuration Window

- 2. After setting the desired Overcurrent Timeout, click the Device menu and then select *Flash App Firmware to Device*.
- 3. Specify the appropriate adapter.



Setting OCP Threshold on the TPS6598x

4. Click the Read Current Region Offsets button to automatically obtain correct offsets (optional), as shown in Figure 5.

Elash Firmware	to De 💡 🔀
Flash Project to D	evice (SPI)
USB to SPI Adap	ter: FTDI -
Read Current R	egion Offsets:
Region 0 :	0x2000 🚔
Region 1 :	0x20000 🚔
ОК	Cancel

Figure 5. Load Application Firmware Window

5. Click OK. If successful, a window displays indicating a successful SPI Flash (see Figure 6).

Flash Firmware to De		23
Flash Project to Device (	SPI)	
	TO	53
Flash to Device		25
SPI Flash to Dev	ce succe	essfu
SPI Flash to Dev	ce succe OK	
	(-	
	OK	

Figure 6. Successful Flash Update

6. Reset the TPS6598x device to load the new firmware.



# 4 Results and Analysis

## 4.1 Test Procedure

To perform the OCP test, do the following:

- 1. Power the TPS65988EVM through the barrel jack or an external power supply.
- 2. Connect a UFP board to the TPS65988EVM through the USB Type-C cable. In the following test case, source PDO of TPS65988EVM was set to 5 V at 3 A.
- 3. Connect an oscilloscope probe onto the VBUS test point of the port that has a UFP board attached.
- 4. Set up an electronic load (e-load) between VBUS and GND on the UFP board.
- 5. Configure the oscilloscope to trigger off the negative edge of the VBUS probe line. This lets the user know when an OCP event has occurred.
- 6. When the test setup has been configured properly, press TRANS to set the current transition. This step controls the current level at which the e-load transitions. If the slew rate is too slow, go to SLEW and set an appropriate level to decrease the time each transition requires to reach the set high current.
- 7. Turn on the INPUT button to start using the e-load and loading the UFP board. At this point, an OCP event should be captured on the oscilloscope.

# 4.2 Test Results

Figure 7 shows the default OCP event waveform.

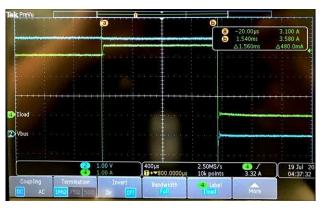


Figure 7. Default OCP Event Waveform

The waveform in Figure 7 has the following configuration flashed onto the TPS65988EVM:

- Voltage: 5 V
- Maximum current: 3 A
- Peak current: 100%
- PP switch Overcurrent Timeout: 1.28 ms
  - **NOTE:** The measurement cursors were set based on when the e-load went above the peak current programmed, to when the VBUS line responded by pulling the voltage to ground. In this example, the Overcurrent Timeout was measured to be 1.56 ms, which implies that some extra delay (approximately 300 µs) caused the time-out to be longer than expected. This falls within the expected time-out value, because the time it takes VBUS to pull low after an OCP event always includes some propagation and a synchronizer timing delay.



Figure 8 shows the default OCP event waveform scope.

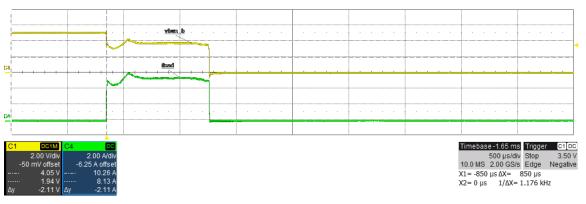


Figure 8. Default OCP Event Waveform (Scope)

The waveform in Figure 8 has the following configuration flashed onto the TPS65988EVM:

- Voltage: 5 V
- Maximum current: 3 A
- Peak current: 130%
- PP switch Overcurrent Timeout: 640 µs

As previously shown, the OCP mechanism can be configured by accessing the Global System Register (0x27). The peak current and time delay can be adjusted to suit the application of the user.

**NOTE:** In this example, the Overcurrent Timeout was measured to be 850 µs, corresponding to the same delay issue of approximately 300 µs seen in the previous waveform (see Figure 7).

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