Application Report

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TPS62366 Thermal and Device Lifetime Information

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DC-DC Converters

ABSTRACT

Wafer-level chip-scale packaging (WCSP) technologies have become one of the industry's leading packaging processes, meeting the continuous trend towards higher performance, smaller size microelectronics devices. As the power density in the devices increases and thermal dissipation turns into a challenge, chip manufacturers must pay special attention to potential reliability constraints, such as electromigration in the flip-chip solder bumps and under-bump metallization (UBM).

Electromigration is described as the diffusive transport of material in a conductor under the influence of electric current. This material flux leads to the formation of regions of mass depletion (voids) or accumulation (hillocks) in the conductor, eventually resulting in electrical failure of the interconnect. Electromigration is a fundamental physical response to the passage of electric current through a conductor and is not specific to a certain device type or manufacturing process.

Local temperature and current density are the dominating factors influencing electromigration and subsequent failure. Black's equation [1, 2] is successfully used as an empirical model estimating the mean time to failure (MTTF) of an interconnect taking electromigration into account:

$$MTTF \; \alpha \; (J^{-n}) \exp (E_a/kT)$$

where J is the current density, E_a is the diffusion activation energy, k is the Boltzmann's constant, T is the temperature and n is a scaling factor.

Electromigration in flip-chip systems and its associated failure mechanisms were the subject of intense research in the last decade. For an overview, please refer to [3-13]

In this note, we investigate and quantify the potential reliability impact of electromigration of wafer-level chip-scale packages, taking Texas Instrument's TPS62366x (4-A peak output current) DC/DC converter family as an example. Measured efficiency and thermal data were used to derive the junction temperature, T_J, at specific (T_{BOARD}, V_{IN}, V_{OUT}, $I_{OUT,AVE}$) operating conditions and compute the expected resulting lifetime by means of a Black's equation. The results show that no significant electromigration-induced lifetime degradation is expected outside of the extreme corners of continuous operating conditions (T_{BOARD} = 85°C with $I_{OUT,AVE}$ > 2.5 A and large V_{OUT}/V_{IN} duty cycles).

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Background

TI's specification for the reliability of the TPS62366xYZH WCSP package (16 bumps, 0.5 mm pitch, 245 µm UBM diameter) is 100 k power-on-hours at T_J = 105°C. This specification is fulfilled by the average current of the current waveform not exceeding I_{AVE} = 1.275 A/pin. Continuously exceeding I_{AVE} = 1.275 A/pin and/or T_J = 105°C might affect the device reliability from electromigration. The next section investigates this impact by concentrating on TPS62366x example use cases.

TPS62366x Lifetime at Example Use Cases

When quantifying the potential effects of electromigration on the TPS62366x lifetime for a given operating point, the current density per ball, as well as the junction temperature, needs to be estimated at those operating conditions.

Current Density per Ball

In the TPS62366x converter family, the two SW balls carrying the output current are the relevant factor limiting electromigration-induced reliability performance at any (V_{IN},V_{OUT},I_{OUT}) operating point. Each SW ball will carry an average output current of $I_{OUT}/2$, which can amount to 2-A peak for $I_{OUT,PEAK}$ = 4 A. Considering an UBM opening diameter of 245 µm, the peak current density per ball reaches J_{PEAK} ~ 4 kA/cm^2 at $I_{OUT,PEAK}$.

Junction Temperature

The junction temperature T_J is calculated as a function of the board temperature T_{BOARD} and the power P_{LOSS} dissipated by the converter:

$$T_J = T_{BOARD} + \theta_{JB} \times P_{LOSS}$$

where θ_{JB} = 30°C/W is the junction-to-board thermal resistance as measured using our reference evaluation board.

P_{LOSS} is estimated using the measured TPS62366x efficiency η at the specific (V_{IN}, V_{OUT}, I_{OUT}) operating point:

$$P_{LOSS} = I_{OUT} \times V_{OUT} (1/\eta - 1) - P_{LOSS,INDUCTOR}$$

with $P_{LOSS,INDUCTOR}$ being the power dissipated in the inductor:

$$P_{LOSS,INDUCTOR} = R_{DC} \times (I_{OUT})^2$$

R_{DC} = 12 mΩ is the assumed DC resistance of the inductor.

Lifetime Estimation and Use Case Assumptions

The TPS62366x MTTF is computed with a standard Black equation with E_a = 1eV and n = 2. The operating conditions in these estimations assume example use cases that are characterized by an average output current of 1.5 A ≤ $I_{OUT,AVE}$ ≤ 3.5 A with a peak output current $I_{OUT,PEAK}$ ≤ 4 A. V_{OUT} is fixed at V_{OUT} = 1.0 V or 1.2 V. The board temperature is T_{BOARD} = 65°C or 85°C. The computed lifetime plots as a function of V_{IN} and $I_{OUT,AVE}$.

Results and Discussion

Figures 1-4 show the calculated TPS62366x lifetime as a function of ($I_{OUT,AVE}$, V_{IN}) for fixed V_{OUT} and T_{BOARD}.

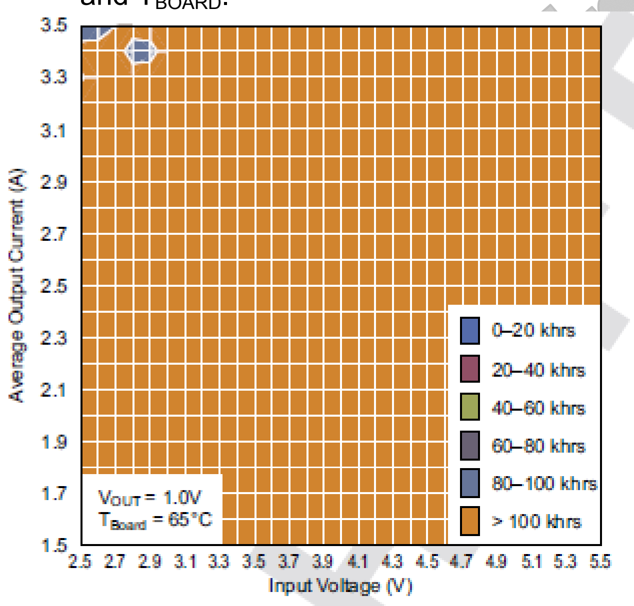

Figure 1. Lifetime for V_{OUT} = 1.0 V, T_{BOARD} = 65°C

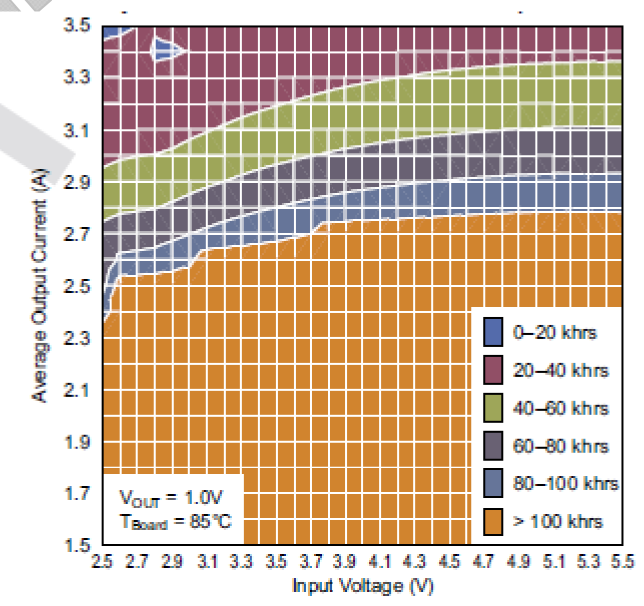

Figure 2. Lifetime for V_{OUT} = 1.0 V, T_{BOARD} = 85°C

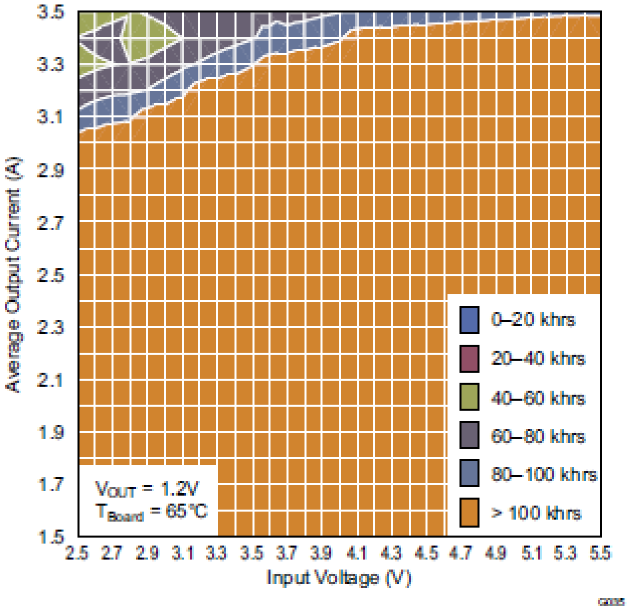

Figure 3. Lifetime for V_{OUT} = 1.2 V, T_{BOARD} = 65°C

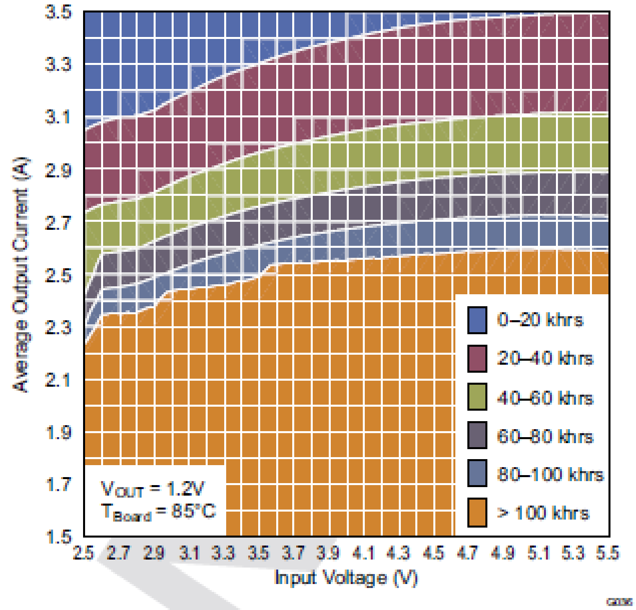

Figure 4. Lifetime for V_{OUT} = 1.2 V, T_{BOARD} = 85°C

These results are summarized in a few key observations:

- For board temperatures up to T_{BOARD} = 85°C, the electromigration-induced lifetime degradation is negligible for all use cases with $I_{OUT,AVE}$ < 2.5 A.
- At the highest board temperature T_{BOARD} = 85°C and large $I_{OUT,AVE}$ currents, the influence of electromigration can be strongly attenuated by operating conditions outside of the largest V_{OUT}/V_{IN} operation duty cycles.
- At board temperature T_{BOARD} = 65°C, the lifetime is only impacted at the most extreme use case conditions ($I_{OUT,AVE}$ > 3A together with larger V_{OUT}/V_{IN} duty cycles).

PCB Layout Recommendations

Proper PCB layout with focus on thermal performance results in smaller junction-to-ambient (θ_{JA}) and junction-to-board (θ_{JB}) thermal resistances, thereby reducing the device junction temperature, T_J for a given dissipated power and board temperature. Wide power traces can sink dissipated heat. This is improved even further on multi-layer PCB designs with vias to different layers. In addition, many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components, affect the power dissipation capabilities of a given device.

Conclusion

The potential impact of electromigration on the reliability of TI's TPS62366x (4A peak output current) DCDC converter family was calculated using Black's equation fed by experimentally measured efficiency and thermal parameters.

Electromigration-induced reliability damage was found to be very low outside of the extreme corners of continuous operating conditions (T_{BOARD} = 85°C with $I_{OUT,AVE}$ > 2.5 A and large V_{OUT}/V_{IN} duty cycles).

PCB layout recommendations were issued, improving thermal dissipation performance and reducing the junction temperature, T_J.

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