

How to Drive High Voltage GaN FETs with UCC21220A

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High-voltage GaN FETs have emerged from theory and laboratory study with commercial technology available from multiple vendors. GaN FETs offer enticing benefits over silicon MOSFETs in certain scenarios, exhibiting minimal gate charge requirements, reduced $R_{DS,ON}$ and size, reduced Q_{OSS} , and increased linearity of C_{OSS} . Thanks to the absence of reverse recovery effects, GaN FETs enable many hard-switching topologies for the first time, notably half-bridge converters and totem-pole PFC. In soft-switching designs such as LLC converters, where the dead time is heavily influenced by the non-linearity in C_{OSS} , GaN FETs yield shorter and more predictable dead time, reduced RMS current, and efficiency improvements. End equipment designers are eager to use GaN FETs for smaller supplies, higher power densities, and lower system temperatures.

The UCC21220A is a dual-channel basic and functional isolated gate driver with 5.5-V UVLO and high dv/dt immunity, suitable for use with high voltage GaN FETs. To maximize the advantages of GaN FETs with UCC21220A, the gate drive circuit must be carefully optimized. Further complicating matters, there are several GaN device constructions from which to choose: cascode, insulated gate, and non-insulated gate. To aid designers in the use of UCC21220A with high voltage GaN FETs, this application note offers a brief introduction to each type of GaN device, and one possible driver circuit for each type of device. Note that suggested passive component values vary with FET manufacturer and part number.

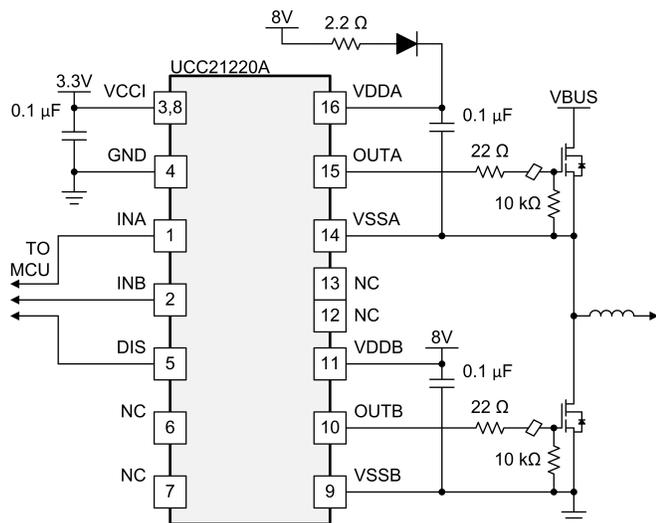


Figure 1. UCC21220A Drives Cascode GaN FETs. Drive Circuit is Similar to Standard MOSFET Circuit.

Cascode GaN FETs

Cascode GaN FETs are devices that combine a high-voltage depletion-mode GaN FET with a low-voltage MOSFET to form a normally-off device. The cascode configuration retains many of the desirable switching characteristics of a GaN FET, including very fast switching speeds and reduced parasitic capacitances. The highly-optimized low-voltage silicon MOSFET gives the cascode device low gate charge and a wide gate drive voltage range. Figure 1 depicts an example cascode GaN drive circuit. Note the similarity with existing MOSFET drive circuits. Even with a large gate resistor, the turn-on and turn-off times of the cascode GaN FET can be remarkably fast. Because of the high di/dt during switching, a ferrite bead in the gate drive loop is sometimes recommended by the manufacturer to eliminate oscillation at the gate pin, especially for standard TO-220 or TO-247 packages with large common source inductance parasitics. See Section 1 for more details on suppressing gate ringing.

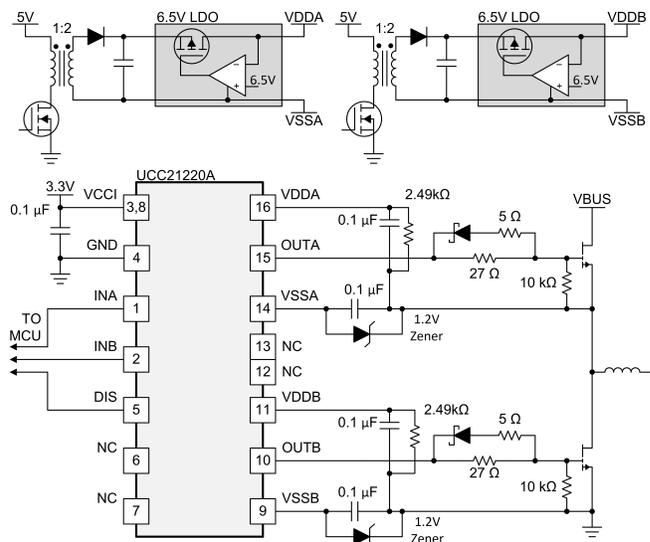


Figure 2. UCC21220A Drives Insulated Gate GaN FETs. Well-regulated Supplies are Required.

Insulated Gate GaN FETs

Insulated gate GaN FETs have a thin insulating layer separating the gate from the channel. Insulated gate GaN FETs behave similarly to existing MOSFETs, but with limited drive voltage range: gate voltages greater than 7 V can easily damage the FET. Furthermore, the threshold voltage for conduction is low, so fast switching can trigger dv/dt -induced turn-on. Negative

turn-off voltage is a common solution to improve the noise immunity. However, excessive negative turn-off voltage increases the source-drain voltage across the FET during the freewheeling period, reducing efficiency. Consequently, minimizing dead time is essential to limit the freewheeling power dissipation.

Figure 2 presents an example drive circuit for insulated gate GaN. The drive circuit requires a well-regulated power supply to prevent damage to the gate and to maintain negative turn-off bias. UCC21220A can support these power supply requirements. Since the driver is isolated, VSS pins may be operated below system ground. An unregulated isolated supply is stepped down to 6.5 V by a low-dropout post-regulator, and a 1.2-V Zener diode generates the negative rail. Split capacitors near the driver supply pins are required to keep the gate drive loop small and low-impedance, since the turn-on loop travels from VDD to COM, and the turn-off loop travels from VSS to COM.

The cautious bias supply approach outlined in **Figure 2** requires many extra components, but for designs where the expected switch node dv/dt and di/dt are small, the supply requirements can often be relaxed. Additional suggestions for simplified power supply circuits with this GaN FET construction are included in the references. TI recommends biasing UCC21220A VDD-VSS pins with at least 6 V to avoid accidental UVLO tripping.

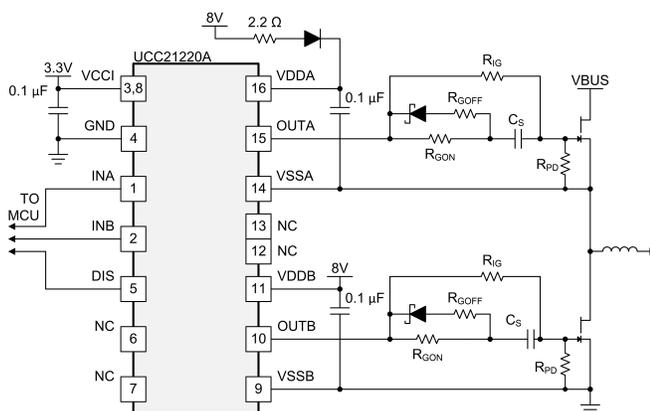


Figure 3. UCC21220A Drives Non-insulated Gate GaN FETs. Supply Requirements are Relaxed, but the Drive Circuit is Complex.

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Non-insulated Gate GaN FETs

Non-insulated Gate GaN FETs are more peculiar with a resistive diode at the gate. As V_{GS} (or V_{GD}) increases above the threshold voltage, the gate begins to conduct in the low milliamp range. The maximum drain current is proportional to the gate current, but the gate can only withstand a few tens of milliamps before damage. The drain-source current path behaves like a standard FET, with a resistive voltage drop and bidirectional current conduction. The choice of VDD, FET characteristics, and required switching times heavily affects external component selection.

Figure 3 shows the drive circuit commonly suggested by non-insulated gate GaN FET manufacturers, modified for use with UCC21220A. The principles of the drive circuit and equations for component selection are discussed in the references. While this material describes a split output, a separate turn-on and turn-off path can be created for UCC21220A with a properly placed Schottky diode as shown. The effective R_{GOFF} of this circuit is $(R_{GON} || R_{GOFF})$. The driver supply voltage of **Figure 3** tolerates some fluctuations, since the gate current is limited by series resistor R_{IG} . Although designers can use bootstrap supplies or loosely-regulated isolated supplies without post-regulation, large changes in the supply voltage affect the peak turn-on and turn-off currents, the steady-state gate current, and the amount of negative turn-off.

1 References

1. [Transphorm Cascode GaN Transistor Application Note](#): See Part IV, Section 2 "Required and Recommended External Components"
2. [GaN Systems Insulated Gate Transistor Application Note](#): See Pages 9-16 (Miller effect, gate ringing, power supply considerations)
3. [Panasonic Gate Injection Transistor Application Note](#): See Section 2.1, 2.2, 2.3 for fundamentals; and Section 3 "Gate Drive Circuit Design"

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