# UCC25710 98-W LLC Resonant Half-Bridge 4-String LED Driver Design Review

# **Application Report**



Literature Number: SLUA601 August 2011



# UCC25710 98-W LLC Resonant Half-Bridge 4-String LED Driver Design Review Texas Instruments Michael O'Loughlin

#### **Introduction:**

Digital TV's and Monitors are much thinner than the old bulky Cathode Ray Tubes (CRT) that were used for these electronic peripherals in past years. These thin digital TVs have been very attractive to consumers because they take up less space. To help meet customer demand and make this digital equipment thinner some manufactures have turned to half bridge LLC resonant converters to drive the LED backlighting of these devices. This is because the zero voltage switching (ZVS) that can be achieved with this topology leads to more efficient higher power density designs, requiring less heat sinking than hard switching topologies. To help meet this need TI has developed the new UCC25710 LLC Resonant Half Bridge Controller, for Multi-String LED driver applications, with PWM dimming. The purpose of this application note is to review the design of 98W LLC Resonant 4 String LED driver using the UCC25710 controller, with PWM dimming.

# **Design Parameters:**

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Design Parameters	
Minimum Input Voltage (V <sub>IN_MIN</sub> )	370V
Nominal Input Voltage (V <sub>IN_NOM</sub> )	390V
Maximum Input Voltage (V <sub>IN_MAX</sub> )	410V
Number of LED Strings/Outputs (N <sub>ST</sub> )	4
Desired LED Current (I <sub>LED1</sub> )	250mA
Forward LED Voltage at 250mA (V <sub>FLED</sub> )	3.06V
Number of LEDs (N <sub>LED</sub> )	32
Resonant Frequency Target (f <sub>o</sub> )	100 kHz
Dimming Frequency (f <sub>DIM</sub> )	300Hz
Minimum PWM Dimming Duty Cycle (D <sub>MIN</sub> )	1%
Output Over Voltage Turnoff (OV)	136V
Output Under Voltage Turnoff (UV)	43V
Efficiency at Maximum Load	92%
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Table 1, Design Specifications



# **Functional Schematic Power Stage:**

The UCC25710 LLC controller was designed to be used to drive multiple LED strings using a multiple transformer approach with PWM Dimming. Please refer to Figure 1. This approach allows the currents in multiple LED strings (LED1 to LEDN) to share current and be controlled by one current sense signal developed across a single current sense resistor (R<sub>S</sub>). This works by using LLC transformer with the same turns ratio (a1) and connecting the primaries of the transformers (T1 through TN) in series and running the outputs in parallel per Figure 1. The premise is that if the primary currents are equal the secondary currents should be equal due to the transformers turns ratio. This allows for controlling the current with only one current sense signal for multiple LED strings.

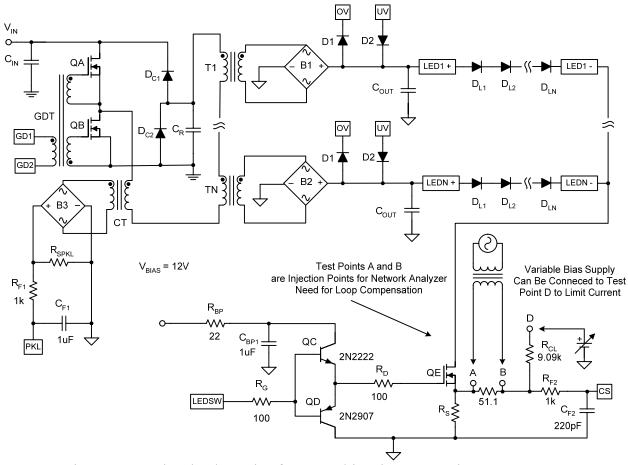


Figure 1, Functional Schematic of LLC Multi-String LED Driver Power Stage



#### **Controller Schematic**

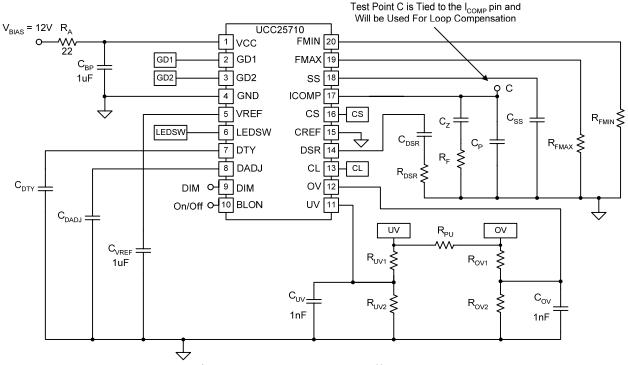


Figure 2, UCC25710 Controller Setup

#### Calculate the Output Voltage for a Single String (V<sub>LED1</sub>)

In this design example Cree XRE LED's were used for the backlight which had a forward voltage ( $V_{FLED}$ ) of 3.06V at 250mA of load current ( $I_{LED1}$ ). This would result in a single string output voltage ( $V_{LED1}$ ) of roughly 98V.

$$V_{LED1} = N_{LED} \times V_{FLED} = 32 \times 3.06 = 97.92V$$

#### **Calculate Total Output Power (Pout)**

Based on the total number of LED strings ( $N_{ST}$ ) and the single string output voltage and the current of the LED strings ( $I_{LED1}$ ), the total output power ( $P_{OUT}$ ) required by this design would be roughly 98W.

$$P_{out} = N_{st} \times V_{LED1} \times I_{out} = 4 \times 97.92V \times 250 mA = 97.92W$$

#### Selecting B1 and B2 Bridge Rectifiers

To meet the efficiency goals of the design B1 and B2 bridge rectifiers were constructed with 1A Schottky rectifiers from STMicrolectronics, part number STPS1150A.



Forward voltage drop of B1 and B2 rectifier diodes (V<sub>F</sub>):

$$V_F = 0.82V$$

Calculated B1 and B2 rectifier diode power dissipation (P<sub>DIODE</sub>):

$$P_{DIODE} = \frac{P_{OUT}}{V_{LED1} \times N_{ST}} = 205mW$$

#### Select FETs QA and QB

Estimate transformer turns ratio (a1)

$$a1 = \frac{\frac{V_{IN\_MIN} \times 0.9}{2}}{N_{ST}(V_{LED1} + 2 \times V_F)} = 0.42$$

Calculate FET QA and QB RMS Current (IQA RMS, IQB RMS)

$$I_{QA\_RMS} = I_{QA\_RMS} = \frac{P_{OUT}}{2 \times \eta \times \left(\frac{2}{\pi}\right) \times N_{ST} \times V_{LED1} \sqrt{2}} \times \frac{1}{a1} \approx 0.36A$$

Based on the efficiency requirements 550V, CoolMoss FETs, part number IPP50R350CP were chosen for the design with following device parameters.

$$R_{DS(on)} = 0.35ohm$$
, FET on Resistance (R<sub>DS(on)</sub>)

$$C_{OSS} = 46 pF$$
, FET Drain to Source Capacitance ( $C_{OSS}$ )

 $V_{DS\_SPEC} = 100V$ , Specified Voltage Where COSS was Measured ( $V_{DS\_SPEC}$ )

$$Q_g = 19nC$$
, Gate Charge

Calculate Average C<sub>OSS</sub> (C<sub>OSS AVG</sub>)

$$C_{OSS\_AVG} = C_{OSS} \sqrt{\frac{V_{DS\_SPEC}}{V_{IN\_MAX}}} \approx 22.7 \, pF$$

Estimate FET QA and QB losses at resonance ( $P_{QA}$  and  $P_{QB}$ )

 $V_{GATE} = 12V$  , Voltage driving the FETs QA and QB ( $V_{GATE}$ )

$$P_{QA} = P_{QB} = \left(\frac{I_{QA\_RMS}}{2}\right)^2 \times R_{DS(on)} + Q_G \times V_{GATE} \times f_O = 61mW$$



#### Transformer T1 through TN, TN =T4:

The design of an LLC half bridge LED driver is an iterative process based mostly on the LLC transformer design/selection. The following equations can be used to design/select the initial transformer used in this design. It is not uncommon to go through a couple of transformer designs/selections to get the optimal desired performance. The following equations were used to select the initial transformer for the design.

The magnetizing current on the primary  $(I_{MP})$  must be sized to achieve ZVS switching based on FET QA and QBs average  $C_{OSS}$ 

 $T_{DT} = 400nS$  , Minimum UCC25710 fixed delay to achieve ZVS

$$I_{MP} = \left(\frac{\left(2 \times C_{OSS\_AVG}\right) \times V_{IN\_MAX}}{\frac{T_{DT}}{2}}\right) \approx 93mA$$

Estimate the maximum transformer magnetizing inductance ( $L_{MP\_MAX}$ ) that will allow for zero voltage switching at resonance. This equation allows for the switching frequency to achieve 2X the resonant frequency ( $2Xf_O$ ) and also accounts for the magnetizing current which is symmetrical around zero amps.

$$L_{MP\_MAX} \le \left(\frac{\frac{V_{IN\_MAX}}{2}}{(2 \times I_{MP}) \times N_{ST}}\right) \left(\left(\frac{1}{(2f_O) \times 2}\right) - T_{DT}\right) = 578uH$$

To save money transformer primary leakage inductance ( $L_{PLK}$ ) was used as the resonant inductor ( $L_r$ ). Figure 3 shows a functional schematic of an LLC half bridge converter using the transformer leakage inductance for the resonant inductor.



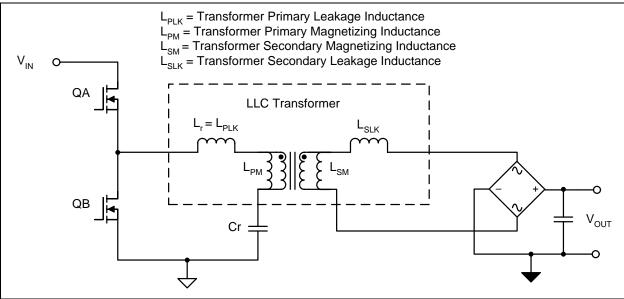


Figure 3, Schematic of an LLC Using L<sub>PLK</sub> for L<sub>R</sub>

Note that the resonant inductance  $(L_r)$  for the multi string LLC half bridge presented in Figure 1 is based on the multiple of transformers used  $(N_{ST})$  in the design and can be calculated as follows.

 $L_r = N_{ST} \times L_{PLK}$ , Total Primary leakage Inductance is Used for Resonant Inductance for the LLC

In most LLC designs that use the primary leakage inductance for the resonant inductor set the ratio of magnetizing inductance and leakage inductance ( $L_n$ ) between 3 and 10 for the initial design. For this design we selected  $L_n$  to be 4.

$$L_n = \frac{L_{MP}}{L_{PLK}} = 4$$

For this design a Vitec transformer part number 75PR8112 with the following characteristics was chosen for the LLC transformers T1 through T4.

 $L_P = 245uH$ , Primary Inductance

 $L_{PLK} = 49uH$ , Primary Leakage Inductance

The primary magnetizing inductance ( $L_{MP}$ ) of the transformer used in this design was less than calculated  $L_{PM\ MAX}$ .

$$L_{PM} = L_P - L_{PLK} = 196uH$$



$$L_n = \frac{L_{MP}}{L_{PLK}} = 4$$
, Transformer 75PR8112 had an Ln of 4

 $L_S = 1050uH$ , Secondary Inductance

 $L_{SLK} = 210uH$ , Secondary Leakage Inductance

 $L_{SM} = L_S - L_{SLK} = 840uH$ , Secondary Magnetizing Inductance

 $DCR_P = 0.118ohm$ , Primary Transformer DC Resistance

 $DCR_s = 0.47$  ohm, Secondary Transformer DC Resistance

Check Transformer Turns Ratio (a1'). Note in a resonant converter the secondary leakage inductance has an effect on the transformer turns ratio. This is because the voltage across the resonant capacitor cancels out the voltage developed across the transformers' primary leakage inductances at resonance.

$$a1' = \frac{L_{SM} \sqrt{\frac{L_{PM}}{L_{SM}}}}{L_{SM} + L_{SLK}} \approx 0.39 \text{ , Effective Transformer Turns Ratio}$$

$$\frac{1}{a1'}$$
 = 2.59, Effective Gain Across the Transformer

# Calculate resonant capacitor (C<sub>r</sub>)

$$C_r = \frac{1}{(2\pi \times f_O)^2 (N_{ST} \times L_{PLK})} \approx 13nF$$

Select standard capacitor for Cr and recalculate resonant frequency

$$C_r = 12nF$$

$$f_o = \frac{1}{(2\pi \times f_o)\sqrt{N_{ST} \times L_{PLK} \times C_r}} \approx 103.8kHz$$



During the evaluation process we had noticed that the design's LED stings shared current the best when the converter was run **above resonance** and the LED outputs were within +/- 2V of each other.

Program the UCC25710 minimum frequency ( $f_{MIN}$ ) to the resonant frequency by properly selecting resistor  $R_{FMIN}$ .

$$9.83k\Omega \le R_{FMIN} \le 102k\Omega$$

$$R_{FMIN} = \frac{0.15}{2 \times 24.6 \, pF \times f_O} \approx 29.38 k\Omega$$

Select a standard resistor value for the design.

$$R_{FMIN} = 30.1k\Omega$$

Double check the minimum frequency (f<sub>MIN</sub>) based on the R<sub>FMIN</sub> selection.

$$f_{MIN} = \frac{0.15}{2 \times 24.6 \, pF \times R_{FMIN}} \approx 101.3 kHz$$

Program the UCC25710 maximum frequency ( $f_{MAX}$ ) to twice the resonant frequency by properly selecting resistor  $R_{FMAX}$ .

$$4.22k\Omega \le R_{FMIN} \le 53.6k\Omega$$

$$R_{FMAX} = \frac{0.0664}{2 \times 24.6 \, pF \left[ 2 \times f_O - f_{MIN} \right]} \approx 12.7 k\Omega$$

Select a standard resistor value for R<sub>FMAX</sub>.

$$R_{FMAX} = 12.7k\Omega$$

Double check maximum frequency limit (f<sub>MAX</sub>) based on the R<sub>FMAX</sub> resistor selection

$$f_{MAX} = \frac{0.0664}{2 \times 24.6 \, pF \times R_{FMAX}} \approx 207.6 kHz$$



Calculate transformer primary RMS current (I<sub>PRMS</sub>) and secondary RMS current (I<sub>SRMS</sub>).

$$I_{PRMS} = \frac{1}{4\sqrt{2}} \times \frac{P_{OUT}}{a1 \times \eta \times VLED1 \times N_{ST}} \sqrt{\frac{a1^4 \left(\frac{V_{LED1}}{I_{LED1}}\right)^2 \left(\frac{1}{f_o}\right)^2}{L_{PM}^2}} = 0.859A$$

$$I_{SRMS} = \frac{I_{LED1}}{\frac{2}{\pi} \sqrt{2}} = 0.278 \,\text{A}$$

Estimate Transformer Loss  $(P_{T1})$  to be 2 times the conduction losses. Note this is only an estimate and may vary based on the magnetic manufacture. It is always a good idea to consult a magnetic expert in regards to determining the exact magnetic losses.

$$P_{T1} = 2(I_{PRMS}^2 \times DCR_P + I_{SRMS}^2 \times DCR_S) \approx 247 mW$$

Check LLC gain over input range to make sure transformers can be used for the design. Start by calculating the minimum  $(M_{MIN})$  and maximum  $(M_{MAX})$  gain needed and then compare to the LLC gain (M(f)) vs frequency.

$$M_{MIN} = \frac{2 \times N_{ST} (V_{LED1} + 2 \times V_F)}{V_{IN\_MAX} - I_{PRMS} \times 0.9 \times R_{DS(on)}} = 1.94$$

$$M_{MAX} = \frac{2 \times N_{ST} (V_{LED1} + 2 \times V_F)}{V_{IN-MIN} - I_{PRMS} \times 0.9 \times R_{DS(qp)}} = 2.15$$

Next will require calculating the total equivalent resistance reflected across the transformer  $(R_{EQ})$ .

$$R_{EQ} = \frac{\left(V_{LED1}\right)^2 N_{ST} \times a1^2}{\frac{8}{\pi^2} P_{OUT}} \approx 72\Omega$$

Next will require calculating the total quality factor (Q) of the LLC.



$$Q = \frac{\sqrt{\frac{N_{ST} \times L_{PLK}}{C_r}}}{R_{EQ}} \approx 1.77$$

Then plot the amplitude of the approximate multi string LLC gain versus frequency (M(f)) starting from the resonant frequency ( $f_O$ ) to two times the resonant frequency ( $2xf_O$ ). Remember the normalized equation for M(f) is just an approximation and the design will have to be fine tuned based on actual performance. However, this approximation will help design or select your initial LLC transformers. The magnitude of M(f) needs to be able to support the gain required by  $M_{MIN}$  and  $M_{MAX}$  of the design. The M(f) gain should go above  $M_{MAX}$  and below  $M_{MIN}$  from the resonant frequency ( $f_O$ ) to two times the resonant frequency ( $f_O$ ). If less gain is desired to meet design requirements it can be obtained by increasing Q. This can be accomplished by increasing the resonant frequency by decreasing  $C_r$  and/or adjusting the transformers primary leakage inductance ( $L_{PLK}$ ). Please refer to Figure 4 for a plot of M(f) with the current Q of 1.77 and of M(f) with a Q of 10. Note a Q of 1.77 worked for this design.

In the approximation for M(f) the normalized switch frequency  $(f_n)$  is defined by the frequency (f) divided by the resonant frequency  $(f_0)$ .

$$f_n = \frac{f}{f_O}$$

$$M(f) = \frac{V_{OUT} \times N_{ST}}{\frac{V_{IN}}{2}} = \frac{\left[ \left( L_n \times f_n \times \frac{1}{a1} \right) + j \left[ \left( L_n + 1 \right) \times f_n^2 - 1 \right] + j \left[ \left[ f_n^2 - 1 \right] \times f_n \times Q \times L_n \right] \right]}{\left[ \left( L_n + 1 \right) \times f_n^2 - 1 \right] + j \left[ \left[ f_n^2 - 1 \right] \times f_n \times Q \times L_n \right]}$$

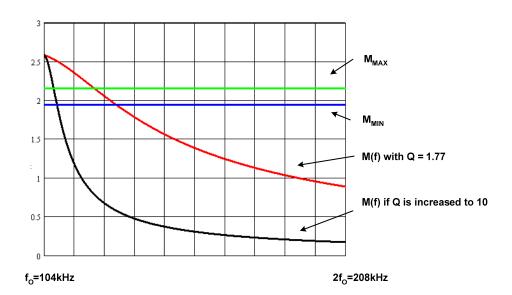


Figure 4, Plot of M(f) vs Frequency

# Selecting Input Capacitor Bank (C<sub>IN</sub>)

In the normal application the LED driver would be preceded by a PFC pre-regulator and the input capacitor would be sized for holdup during one line cycle of dropout.

$$C_{IN} \ge \frac{2\left(\frac{P_{OUT}}{\eta \times 60Hz}\right)}{V_{IN-NOM}^2 - \left(V_{IN-NOM} \times 0.7\right)^2} \approx 46uF$$

Calculate low frequency RMS if converter follows a PFC pre-regulator ( $I_{CIN\_RMS\_LF}$ ). Note this frequency is 2X the line frequency powering the PFC pre-regulator.

$$I_{CIN\_RMS\_LF} = \frac{P_{OUT}}{V_{IN\_MIN} \times \frac{2}{\pi} \times \eta} \times \frac{1}{\sqrt{2}} \approx 320 mA$$

Calculate High Frequency RMS Current (I<sub>CIN RMS HF</sub>)

$$I_{CIN\_RMS\_HF} = \sqrt{I_{PRMS}^2 - I_{CIN\_RMS\_LF}^2 - \left(\frac{P_{OUT}}{V_{IN\_MIN} \times \eta}\right)^2} \approx 743 mA$$

To meet the voltage and RMS requirements five 10 $\mu$ F, 450V aluminum electrolytic capacitors, Panasonic part number EEUEB2W100, were used in parallel for  $C_{IN}$ .

$$C_{IN} = 50uF$$

#### **Selecting Output Capacitors (COUT)**

$$I_{COUT\_RMS} = \sqrt{I_{SRMS}^2 - I_{LED1}^2} \approx 121 mA$$
, Output Capacitor RMS Current

Calculated minimum C<sub>OUT</sub> based on capacitance ripple voltage being 0.5% of the output.

$$C_{OUT} \ge \frac{I_{LED1}}{V_{LED1} \times 0.005 \times f_O} \approx 4.9 uF$$

Calculate maximum output capacitance equivalent series resistance ( $ESR_{COUT\_MAX}$ ) based on ripple voltage across the output capacitance ESR to be 0.5% of the output voltage.



$$ESR_{COUT\_MAX} \leq \frac{V_{LED1} \times 0.005}{I_{SRMS} \sqrt{2}} \approx 1.25\Omega$$

To meet  $C_{OUT}$  RMS current, output voltage and ripple voltage requirements two 10 uF, 160V aluminum electrolytic capacitors from Panasonic, ECA2CM100, were used in parallel for  $C_{OUT}$ .

$$C_{OUT} = 20uF$$

#### **Selecting FET QE for PWM Dimming**

To meet the power and efficiency requirements a 250V 51A, FET, FDP51N25 from Fairchild was chosen for the design with the following device parameters.

$$R_{DS(on)} = 0.06ohm$$
, FET on Resistance (R<sub>DS(on)</sub>)

 $V_{DS\_SPEC} = 25V$ , Specified Voltage Where COSS was Measured ( $V_{DS\_SPEC}$ )

$$Q_g = 55nC$$
, Gate Charge

$$C_{OSS} = 530 pF$$
, FET Drain to Source Capacitance (Coss)

Calculate Average C<sub>OSS</sub> (C<sub>OSS AVG</sub>):

$$C_{OSS\_AVG} = C_{OSS} \sqrt{\frac{V_{DS\_SPEC}}{V_{IN\_MAX}}} \approx 22.7 \, pF$$

 $t_r \approx 465 ns$ , Typical Estimated  $V_{DS}$  rise time from FET data sheet

 $t_{\it f} \approx 130 \it ns$  , Typical Estimated  $V_{\rm DS}$  fall time from FET data sheet

Estimated Dimming FET Losses (PQE)

$$P_{OE-RDS(on)} = (I_{LED1} \times N_{ST})^2 R_{DS(on)} = 60 mW$$
, Calculated FET Conduction Losses

$$P_{QE\_SWITCH} = \frac{I_{LED1} \times N_{ST}}{2} (t_r + t_f) f_{DIM} \times V_{LED1} = 8.74 mW$$
, Calculated FET Switching Losses

$$P_{QEg} = 2 \times Q_g \times F_{DIM} \times V_{GATE} \approx 0.4 mW$$
 , Calculated FET Gate loss

$$P_{QE\_COSS} = \frac{2 \times C_{OSS\_AVG} \times V_{LED1}^2 f_{DIM}}{2} \approx 0.38 mW$$
, Calculated Average FET Coss loss



$$P_{QE} = P_{QE\_RDS(on)} + P_{QE\_SWITCH} + P_{QEg} + P_{QE\_COSS} \approx 69.5 mW$$

## **Programming the UCC25710 for PWM Dimming**

DSR Slew Rate Programming:

This control IC has an input for PWM dimming (DIM, Pin 9) was design to receive a low frequency ( $f_{DIM}$ , 300 Hz) 0 to 5V diming signal and controls the brightness of the LEDs by adjusting the duty cycle of  $f_{DIM}$ .

To ensure smooth current transitions during PWM dimming the UCC25710 has a feature called dimming slew rate (DSR Pin 14) that can be programmed by properly selecting the  $C_{DSR}$  and  $R_{DSR}$  passive components.

Set DSR slew rate ( $t_{SLEW}$ ) to 0.5 of dimming period and calculate slew rate capacitor ( $C_{DSR}$ ). This feature was added to reduce overshoot and potential audible noise. It may have to be adjusted pending on individual design performance.

$$t_{SLEW} = \frac{0.5}{f_{DIM}} \approx 16.7us$$

$$C_{DSR} = \frac{44uA \times t_{SLEW}}{2.6V} = 282 \, pF$$

$$R_{DSR} = \frac{0.7V}{40uA} = 17.5k\Omega$$

Select standard component values for  $C_{DSR}$  and  $R_{DSR}$ .

$$C_{DSR} = 270 pF$$

$$R_{DSR} = 17.8k\Omega$$

Programming PWM Dimming Duty Cycle Adjust:

To ensure that a the peak current can be controlled down to 1% duty cycle the UCC25710 has a PWM dimming duty cycle adjust feature, which extends the LEDSW duty cycle to ensure the



peak current can be reached. This feature can be correctly setup by properly selecting the  $C_{DTY}$  and  $C_{DADJ}$  capacitors. Note for a more detailed explanation of the PWM Duty Cycle Adjust feature can be found in the UCC25710 data sheet [5].

$$C_{DTY} = \frac{15.65uA \times \frac{1}{f_{DIM}}}{0.1V} = 522nF$$

$$C_{DADJ} = \frac{20 \mu A \times \sqrt{\frac{D_{MIN} \times 0.05}{f_{DIM}^{2}} - \frac{D_{MIN}}{f_{DIM}}}}{\left[ (1 - D_{MIN}) \times 2.5V \right] + 0.1V} \approx 320 pF$$

Standard components were selected for CDTY and CDADJ

$$C_{DTY} = 470nF$$
,  $C_{DADI} = 330pF$ 

# Selecting Average Peak Input Current Sensing Resistor (R<sub>SPKL</sub>)

The UCC25710 has an average input over current shutoff. Resistor  $R_{SPKL}$  is used to monitor the input current through current sense transformer (CT). Resistor  $R_{F1}$  and  $C_{F1}$  form a low pass filter that is setup to have a low frequency pole at 159Hz allowing only the average current sense signal developed across  $R_{SPKL}$  to be passed to the current limit (CL) pin of the UCC25710.

Sizing  $R_{SPKL}$  requires knowing the CT turns ratio (a2), which for this design was 0.001. The following equation describes the transformer turns ratio in terms of secondary current ( $I_S$ ) and primary current ( $I_P$ ) of the current sense transformer.

$$a2 = \frac{1}{100} = \frac{I_s}{I_p}$$

Average input over current ( $I_{IN\_AVG\_OC}$ ) was set to 150% of average reflected output current across the LLC transformer.

$$I_{IN\_AVG\_OC} = \frac{I_{SRMS} \times \sqrt{2} \times \frac{2}{\pi} \times 1.5}{a1 \times \eta} = 1.05A$$

The UCC2510 control IC has a peak current limit threshold of 0.95V, which would require an  $R_{SPKL}$  of 94.8 ohms.



$$R_{SPKL} = \frac{0.95V}{I_{IN-AVG-OC} \times a2} \approx 90.7\Omega$$

A standard resistor is selected for R<sub>SPKL</sub>.

$$R_{SPKL} = 100\Omega$$

### Selecting Average Current Sense Control Resistor (R<sub>S</sub>)

Tying the CREF pin of the UCC25710 to ground sets the current amplifier control voltage to a well regulated 0.5V, which the lowest current sense signal that can be accurately used with this device. Please refer to figure 2.

$$R_S = \frac{0.5V}{N_{ST} \times I_{LDED1}} = 0.5ohms$$

To increase noise immunity a low a pass filter formed by  $R_{F2}$  and  $C_{F2}$  with a pole at roughly 723 kHz. Depending on the amount of noise in the system this may have to be adjusted. The output of this low pass filter is then fed into the CS pin of UCC25710 (Pin 16).

#### Program Output Over Voltage Turnoff (OV)

The UCC25710 has programmable OV feature that turns off the FETs during an over voltage condition. This can be setup by properly selecting  $R_{\rm OV1}$  and  $R_{\rm OV2}$  resistor divider.

Calculate minimum R<sub>OV1 MIN</sub> resistor value so LEDs strings share current within 1%

$$R_{OV1\_MIN} > \frac{V_{LED1}}{I_{LED1} \times D_{MIN} \times 0.01} = 3.92 M\Omega$$

Select Standard Value for R<sub>OV1</sub> greater than R<sub>OV1</sub> MIN:

$$R_{OV1} = 5.36M\Omega$$

Calculate  $R_{OV2}$  based on  $R_{OV1}$  and estimated D1 forward voltage drop ( $V_{D1}$ ):

$$V_{D1} = 0.6V$$



$$R_{OV2} = \frac{R_{OV1} \times 2.6V}{OV - 2.6V - V_{D1}} = 104.9k\Omega$$

Select standard resistor value for R<sub>OV2</sub>

$$R_{OV2} = 105k\Omega$$

Double check over voltage threshold (OV)

$$OV = \frac{2.6V(R_{OV1} + R_{OV2})}{R_{OV2}} + V_{D1} = 136V$$

Calculate OV hysteresis ( $OV_{HYST}$ ) based on  $R_{OV1}$  and  $R_{OV2}$  selection to ensure it meets your design requirements.

$$OV_{HYST} = OV - \frac{2.4V(R_{OV1} + R_{OV2})}{R_{OV2}} + V_{D1} \approx 11V$$

# **Setup Output Under Voltage Turnoff (UV)**

The UCC25710 also comes with a programmable output under voltage FET driver turnoff that can be setup by properly selecting the under voltage lockout pull up resistor ( $R_{PU}$ ) and the resistor divider formed by  $R_{UV1}$  and  $R_{UV2}$ .

$$R_{PU} = \frac{R_{OV1}}{5} \approx 1.07 M\Omega$$

$$R_{UV1} = R_{OV1} - R_{PU} \approx 4.26 M\Omega$$

Select standard resistor values for R<sub>PU</sub> and R<sub>UV1</sub>

$$R_{PU}=1M\Omega$$

$$R_{UV1} = 4.22M\Omega$$

Calculate  $R_{UV2}$  based on  $R_{PU}$ ,  $R_{UV1}$  and the forward voltage drop of D2 ( $V_{D2}$ ).

$$V_{D2} = 0.6V$$

$$R_{UV2} = \frac{\left(R_{UV1} + R_{PU}\right) \times 2.4V}{UV - 2.4V - Vd2} \approx 311.4k\Omega$$



Select a standard resistor value for R<sub>UV1</sub>.

$$R_{UV1} = 316k\Omega$$

Double check under voltage threshold (UV)

$$UV = \frac{2.4V(R_{UV1} + R_{UV2} + R_{PU})}{R_{UV2}} + V_{D2} = 43V$$

Calculate UV hysteresis ( $UV_{HYST}$ ) based on  $R_{UV1}$  and  $R_{UV2}$  selection and ensure it is enough to meet your design requirements.

$$UV_{HYST} = \frac{2.6V(R_{UV1} + R_{UV2} + R_{UP})}{R_{UV2}} + V_{D2} - UV \approx 3.6V$$

# **Setting up Soft Start (SS)**

The UCC25710 control IC has soft start control during power up that can be set by selecting a soft start time ( $t_{SS}$ ) and properly selecting a soft start capacitor ( $C_{SS}$ ).

Note during power up PWM dimming is disabled please refer to the UCC25710 data sheet for details.

$$t_{SS} = 50ms$$

$$C_{SS} = \frac{2.5uA \times t_{SS}}{2.6V} \approx 48nF$$

Select a standard capacitor for C<sub>SS</sub>

$$C_{ss} = 47nF$$

#### **Initial Power up Recommendations**

During the design phase before the current loop is setup and optimized.

It is recommended that the output current and input voltage be brought up slowly. First connect an eternal bias supply initially set to 5.5V connected to test point D per Figure 1. This will put 545mV at the CS pin of the UCC25710. This will fake out the controller so the output does not demand any current. Apply the input voltage and bias supplies per figure 1 and 2. With UCC25710 biased and the input voltage set within the desired input



voltage range (370 to 410V) the bias supply connected to test point D then can be adjusted slowly to zero volts allowing the output current to come up proportionally to the decrease in the bias voltage at test point D.

#### **Evaluate Transformer and ZVS During Initial Power Up.**

While bringing up the power supply initially and slowly bringing up the output current it is a good idea to evaluate the transformers to ensure there is enough magnetizing current to achieve ZVS. Please refer to figure 5 for an example of what the LLC transformer (T1 through TN) primary current should look like (CH4) during normal operation. CH2 shows the switch node voltage at the drain of FET QB and CH1 is the gate voltage of FET QB. FETs QA and QB in this design example are driven with a 1:1:1 gate drive transformer. The gate voltage of QA is the inverse of QBs gate voltage. From the wave form below it can be observed that the switch node (CH2) is fully transitioned by the magnetizing current during the UCC25710s fixed dead time, while the gates of QA and QB are at zero volts, obtaining zero voltage switching. During the design process if it is discovered that the switch node does not fully transition before FETs QA and QB gates are activated there may not be enough magnetizing current to achieve ZVS. This may require redesigning the transformer for more magnetizing current to achieve ZVS. It is not uncommon to go through several transformer designs/selections in a resonant half bridge before settling on the final transformer to be used in the design.

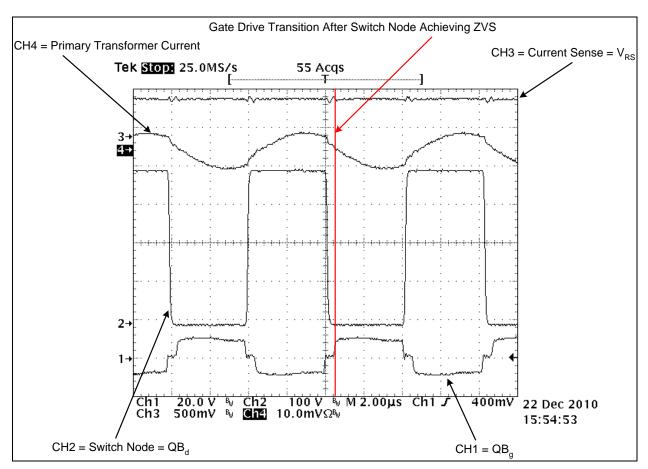




Figure 5, Evaluate Transformer and ZVS During initial power up.

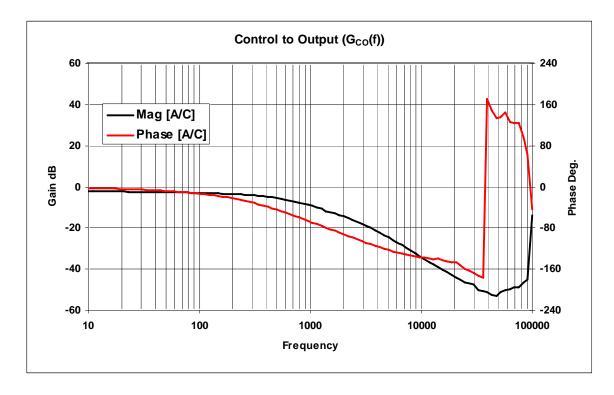
# Compensating the Current Loop $(G_{CL}(f))$

The easiest way to compensate an LLC half bridge is with a network analyzer. Start by setting capacitor feedback capacitor  $C_P$  to 1nF, while not populating feedback components  $C_Z$  and  $R_F$ . This will roll the gain of the current amplifier off fairly early and should control the power LED driver well enough to measure the control to output transfer with a network analyzer.

$$C_P = 1nF$$

The isolated signal from the network analyzer can be injected across the 51.1 ohm that is connected between test points A and B (Figure 1). The control to output transfer ( $G_{CO}(f)$ ) function can then be measured across test points A and C. Test point C can be found in the controller schematic of Figure 2.

$$G_{CO}(f) = (A/C)$$





# Figure 6, Measure Control to Output Transfer Function

Set crossover frequency (f<sub>C</sub>) to a 20<sup>th</sup> the resonant frequency (f<sub>O</sub>).

$$f_C = \frac{f_o}{20} \approx 5.2kHz$$

From the control to output transfer function record the magnitude of the measured gain at the crossover frequency  $(G_{CO}(f_C))$ , this is typically in dB and for this design was -25dB.

 $|G_{CO}(f_C)| = -25dB$ , Record magnitude of control to output transfer function

GM = 510uS, Current Amplifier Transconductance Gain

Calculate feed back resistor (R<sub>F</sub>) to adjust loop gain at crossover

$$R_F = \frac{10^{\frac{-|G_{CO}(f_C)|}{20}}}{GM} \approx 34.9k\Omega$$

A standard resistor value closest to the calculated value should then be chosen for the design.

$$R_F = 33.2k\Omega$$

Calculate feedback capacitor  $(C_Z)$  to put a zero at one tenth the crossover frequency.

$$C_Z = \frac{1}{2\pi \times \frac{f_C}{10}} \approx 9.2nF$$

Select a standard capacitor value for the design and unpopulate capacitor  $C_{P_{\cdot}}$ 

$$C_Z = 10nF$$

$$C_P = Not Populated$$

After the feedback components have been selected it is recommended to measure the current loop ( $G_{CL}(f)$ ) with a network analyzer and check the circuit for stability. In the design example the current loop crossed over at roughly 5 kHz with a phase margin of greater than 45 degrees. Note if the phase margin is less than 45 degrees different compensation components should be selected for the design.

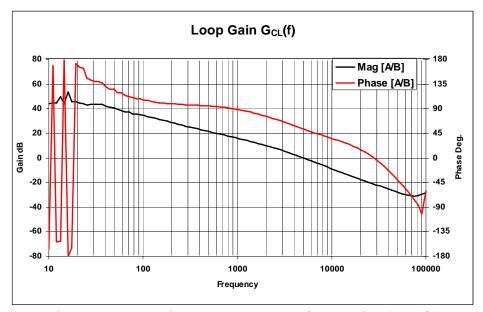


Figure 7, Measured Current Loop Transfer Function (G<sub>CL</sub>(f))

# 98W Reference Design Evaluation

Based on the design equations presented in this application note a 98W LED driver using this topology was constructed and tested. Please refer to Figure 8 and 9 for schematics.



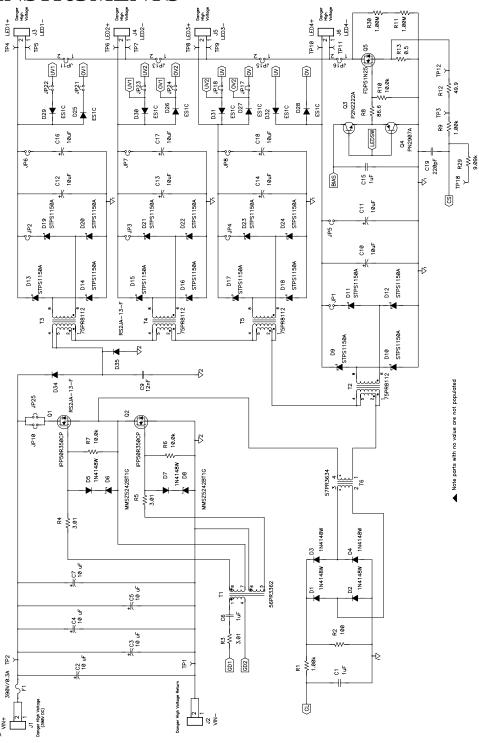


Figure 8, Power Stage Schematic



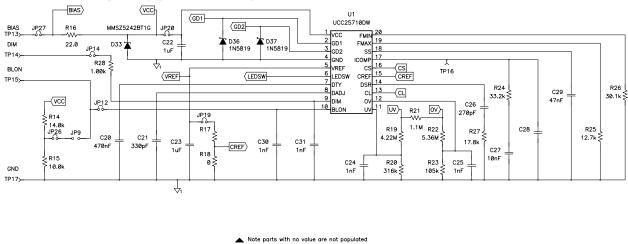


Figure 9, Daughter Board Schematic

#### **Test Data**

# **Current Matching with PWM Dimming**

The following graphs were taken with a 300 Hz PWM dimming frequency. Note each LED output was loaded with 32 Cree XLamp XR-E diodes. At full load the current was controlled to a target current of 250mA through each LED output string.

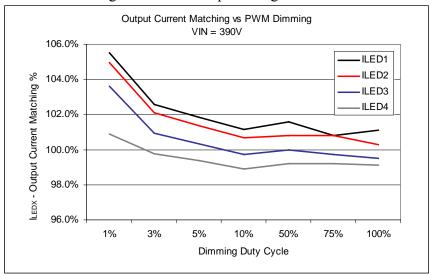


Figure 10, V<sub>IN</sub> = 390V, Current Matching



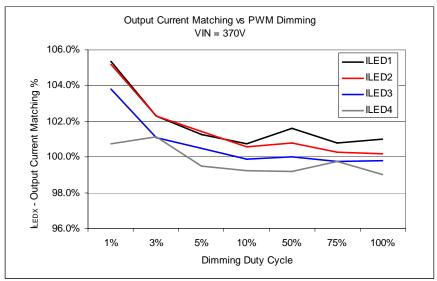


Figure 11,  $V_{IN}$ = 370V, Current Matching

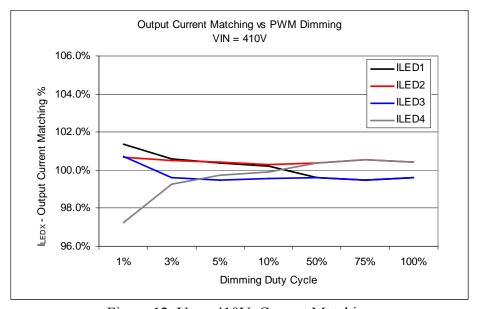


Figure 12,  $V_{IN}$  = 410V, Current Matching



# **Efficiency**

Note to measure efficiency with PWM dimming requires the use of power analyzers on the LED output/s. The following efficiency table was taken with LED voltage strings set to roughly 98V.

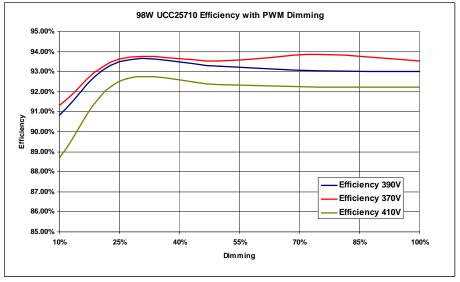
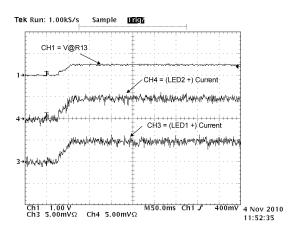


Figure 13, Efficiency 10% to 100% PWM Dimming

LED Current Startup Behavior ( $V_{IN}$  = 390V) Total LED Current = 1A, Individual LED Current  $\approx 0.25$ A



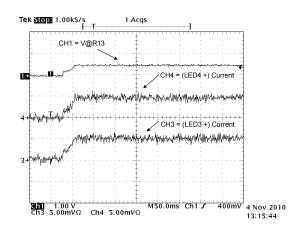
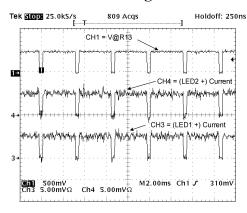


Figure 14, Current LED1 (CH3) and LED2 (CH4)

Figure 15, Current LED3 (CH3) and LED4 (CH4)



#### LED Current during 300 Hz PWM Dimming (V<sub>IN</sub> = 390V) 90% PWM Dimming



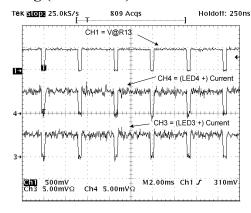


Figure 16, Current LED1 (CH3) and LED2 (CH4) Figure 17, Current LED3 (CH3) and LED4 (CH4)

#### 1% PWM Dimming, Peak LED Current ≈ 0.25A

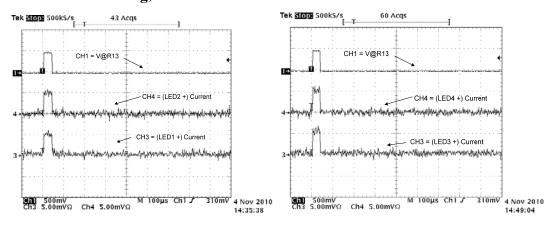


Figure 18, Current LED1 (CH3) and LED2 (CH4) Figure 19, Current LED3 (CH3) and LED4 (CH4)

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- [3] Hong Huang, "Design an LLC Resonant Half Bridge Power Converter" Texas Instruments Power Supply Design Seminar 1900, Topic 3, 2010-2011



[4] Bing Lu, Wenduo Liu, Yan Liang, Fred C. Lee, Jacobus D. van Wyk "*Optimal Design Methodology for LLC Resonant Converter*," 0-7803-9547-6/06/ 2006 IEEE. pp533..538. [5] UCC25710 "*LLC Half Bridge Controller for Multi-String LED Lighting*," Data Sheet, SLUSAD7, 2011

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