
PFC Pre-Regulator Frequency Dithering Circuit

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1 Introduction

In off-line AC-to-DC converters dithering the pulse width modulator (PWM) frequency has proven to reduce EMI by changing it from narrowband to broadband. This article covers a novel technique to dither the switching frequency 20% of an off-line Power Factor Corrected (PFC) pre-regulator. The circuitry used to dither the frequency is accomplished by taking advantage of the PWM's internal timing circuitry.

2 Typical Off-line PFC Pre-regulator

[Figure 1](#) is a schematic of a 250-W AC-to-DC off-line power converter with PFC that was designed for a universal input voltage. This application is similar to many off-line converters that use a pulse width modulator (PWM) to manage the power converter. A good portion of these PWMs develop timing through internal circuitry and it is this internal circuitry that can be taken advantage of to dither the converters switching frequency to lower narrowband EMI.

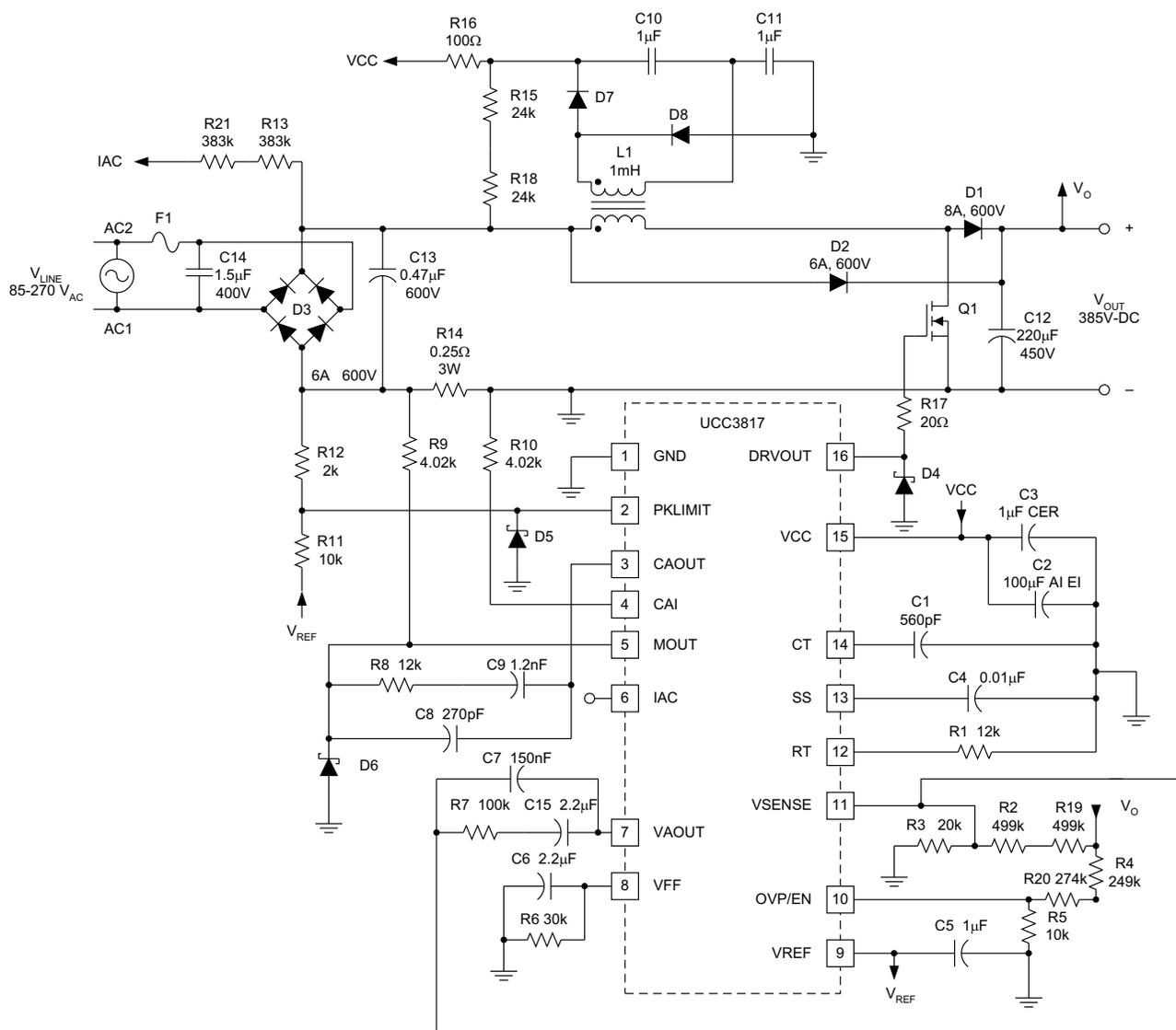


Figure 1. 250-W AC-to-DC Off-Line Power Converter Schematic

3 Frequency Dithering

The frequency dithering technique reduces the narrowband EMI by spreading out the noise spectrum of the power supply. There are limitations on how much the oscillator frequency (f_s) can be dithered. Some of the limiting factors are switching losses and magnetic design. To keep the boost inductor as small as possible and to keep the switching losses in check the frequency dithering should be no more than 20% to 30% of the fundamental frequency. The circuitry presented in this paper was designed to vary the duty cycle from 80% to 100% as a function of the input voltage sine wave. At input line crossover the oscillator frequency will be at 80% of its maximum and will increase and decrease proportionally with changes in the line voltage. Figure 2 shows how f_s varies with input voltage.

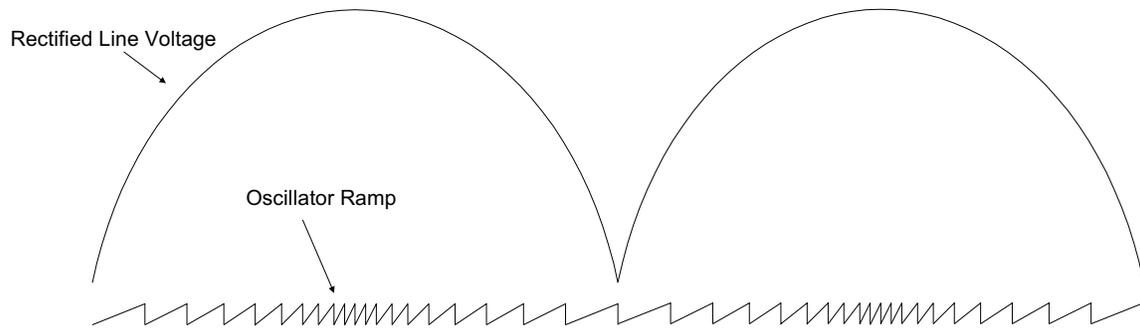


Figure 2. Frequency Dithering with Rectified Line Voltage

4 Internal PWM Timing

Figure 3 shows a functional block diagram of the internal circuitry that generates the oscillator signal of the PWM controller in Figure 1. The timing is set up by an R and C and a comparator. RT sets the charging current in the timing capacitor (CT) through the current mirror formed by Q1 and Q2. An internal comparator with hysteresis will control when CT will charge and discharge forming the PWM timing. To dither the switching frequency of the PWM, circuitry will be added to the converter to modulate CT's charging current.

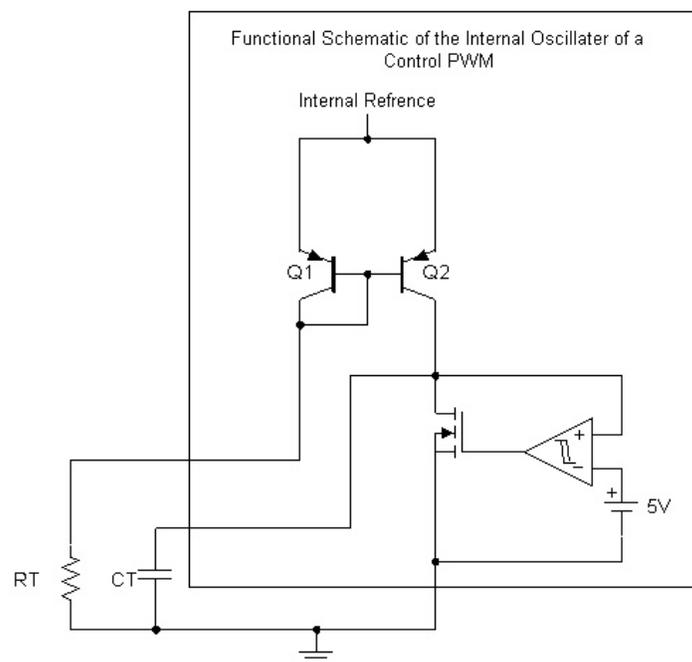


Figure 3. PWM Oscillator Timing Circuitry

5 Circuitry Used for Dithering the PWM Oscillator Frequency

The additional circuitry in Figure 4, when added to the power converter in Figure 1 dithers the PWM oscillator frequency (f_s) by 20% as a function of the input voltage sine wave. This is accomplished by varying the charging current of CT by 20% as the line voltage varies. This is accomplished by using resistors RA through RE and transistor Q2 to vary the oscillating timing circuitry's charging current 20%. R1 is the timing resistor in Figure 1. Capacitor CA is used to filter out any high frequency switching noise.

PFC pre-regulators are typically designed for a universal input line voltage of 85 V to 265 V. These changes in line amplitude would cause changes in the PWM oscillator frequency (f_s) if not corrected. A majority of PFC PWM devices use a multiplier to shape the input current waveform. The multiplier typically has a voltage feed forward function for power limiting and easier control loop compensation. The voltage feed forward circuitry generates a dc voltage (VFF) that is proportional to the rectified line voltage amplitude. In the UCC3817 control device this VFF voltage comes out at pin 8 of the device and is filtered with a resistor and a capacitor. The dithering circuitry uses the VFF signal to correct for changes in line amplitude and is accomplished by replacing R6 in Figure 1 with R6A and R6B and electrical components RF and Q1. As the input voltage amplitude varies with peak line voltage the VFF signal changes proportionately. The VFF voltage controls the current sink formed by Q1 and RF and sinks any changes in current through RA caused by varying peak line voltage. This function ensures that f_s vary as a function of a rectified input sine wave and not function of changing line amplitude.

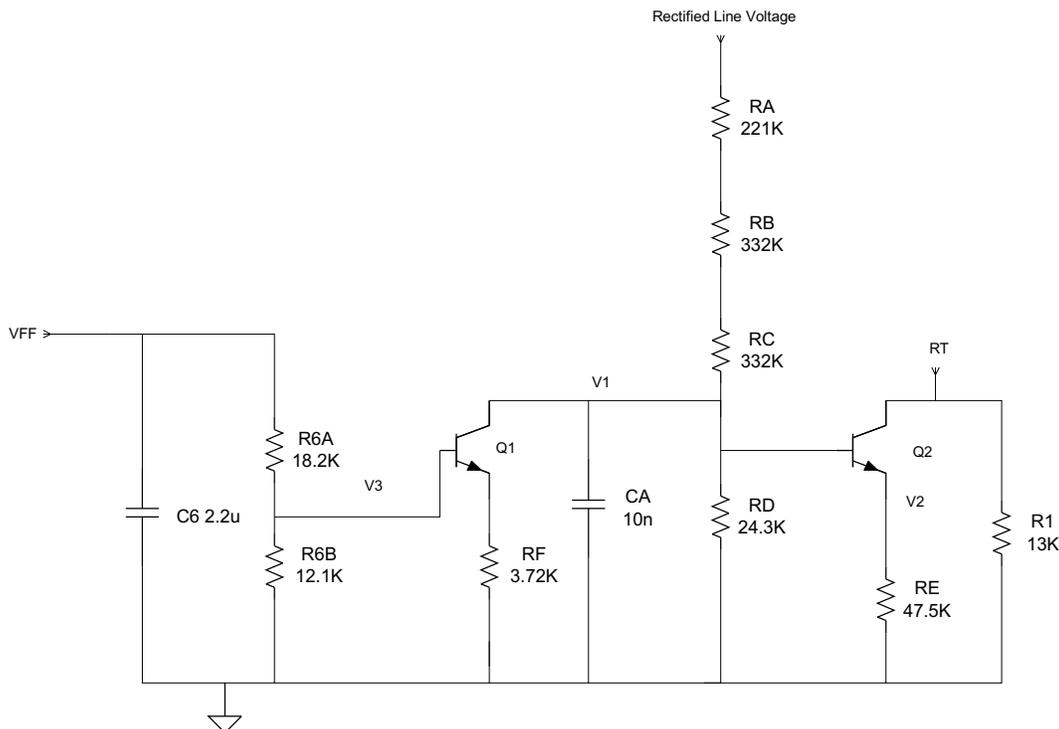


Figure 4. Dithering Circuitry

6 Component Selection for Frequency Dithering Circuitry (Figure 1 and Figure 4)

The first step in selecting the components for the design is the frequency range. For this design a minimum frequency (f_{MIN}) of 80 kHz and a maximum frequency (f_{MAX}) of 100 kHz were chosen for the design. A timing capacitor CT of 560 pF was chosen based on the device's manufacturer data sheet. Equation 1 describes the oscillator frequency behavior of the control device used in this design and varies with different manufactures.

$$f_s = \frac{0.6}{RT \times CT} \quad (1)$$

R1 is selected for f_{MIN} and is the frequency where the converter will operator at line crossover.

The transistors for this design are not going to see excessive voltage or current, thus choosing a 2N2222 for Q1 and Q2. These transistors are setup in this circuit to have a V_{CE} of 500 mV to keep the transistors out of saturation.

$$R1 = \frac{0.6}{f_{\text{MIN}} \times CT} \approx 13 \text{ k}\Omega \quad (2)$$

Selected resistor RE is based on voltage at RT (V_{RT}) and the 500-mV design requirement of V_{CE} and f_{MAX} . The voltage at RT is determined by the device's internal circuitry and can typically be found in the data sheet, for this design V_{RT} was 3 V. RT is the equivalent resistance required to attain f_{MAX} and I_{RT} is the current through RT. I_{R1} and I_{RE} are the currents in resistors R1 and RE respectively.

$$RT = \frac{0.6}{f_{\text{MAX}} \times CT} \approx 10.7 \text{ k}\Omega \quad (3)$$

$$I_{\text{RT}} = \frac{V_{\text{RT}}}{RT} \quad (4)$$

$$I_{\text{R1}} = \frac{V_{\text{RT}}}{R1} \quad (5)$$

$$I_{\text{RE}} = I_{\text{RT}} - I_{\text{R1}} \quad (6)$$

$$RE = \frac{V_{\text{RT}} - V_{\text{CE}}}{I_{\text{RE}}} \approx 47.5 \text{ k}\Omega \quad (7)$$

The next step in the design is to select the components for the divider formed by RA through RD. For this design the peak voltage at the base of Q2 (V1) was 3.2 V and was calculated with the use of Equation 8. V_{BE} for this design was estimated to be roughly 0.6 V.

$$V1 = V_{\text{RT}} - V_{\text{CE}} + V_{\text{BE}} \quad (8)$$

The voltage dividers resistors can then be selected based on Equation 9 trying to minimize loss. $V_{IN(min)}$ is the minimum RMS line voltage of 85 V for this design. The rectified line voltage was obtained by connecting to the output of diode bridge D3 in the schematic of Figure 1.

$$\frac{V1}{RD} = \frac{V_{IN(min)}\sqrt{2}-V1}{RA + RB + RC} \quad (9)$$

To prevent f_s from varying with line amplitude components RF, R6A, R6B and Q1 must be properly selected. The determining factors on selecting these components are changes in current through RA caused by varying line amplitude variations in the VFF signal. The changes in current through RA will be denoted by variable IRA. The design of the power converter determined the VFF signal. In this design VFF varied proportionally with line from 1.4 V to 4.2 V. R6 was also determined by the design requirements and is 30 kΩ. To implement the frequency dithering R6 in figure 1 must be replaced with R6A and R6B of Figure 2. These two resistors can be sized with Figure 1 and Equation 11.

$$R6B = \frac{V_{BE} \times R6}{VFF_{MIN}} \approx 12.1 \text{ k}\Omega \quad (10)$$

$$R6A = R6 - R6B \approx 18.2 \text{ k}\Omega \quad (11)$$

Transistor Q1 and resistor RF form a controllable current sink to suppress the excess current caused by changing peak line voltages. The resistor RF can be selected based on the maximum VFF voltage (VFF_{MAX}) and the change in peak current as the line varies between the minimum ($V_{IN(min)}$) and the maximum ($V_{IN(max)}$) RMS input voltages. The following equation can be used to select RF for proper current sinking.

$$RF = \frac{VFF_{MAX} \times \frac{R6B}{R6A + R6B} - V_{BE}}{\frac{V_{IN(max)} \times \sqrt{2} - V_{IN(min)} \times \sqrt{2}}{RA + RB + RC}} \approx 3.72 \text{ k}\Omega \quad (12)$$

7 Circuit Performance

The circuitry in Figure 4 was added to the circuitry in Figure 1 and the oscillator frequency dithered as a function of the rectified sine wave input voltage and did not vary with the changes in line amplitude. through show the oscillator frequency varying with rectified line voltage, were CH1 is the rectified line voltage and CH2 is the PWM oscillator frequency. The oscillator frequency varied with the input from 82 kHz to 100 kHz.

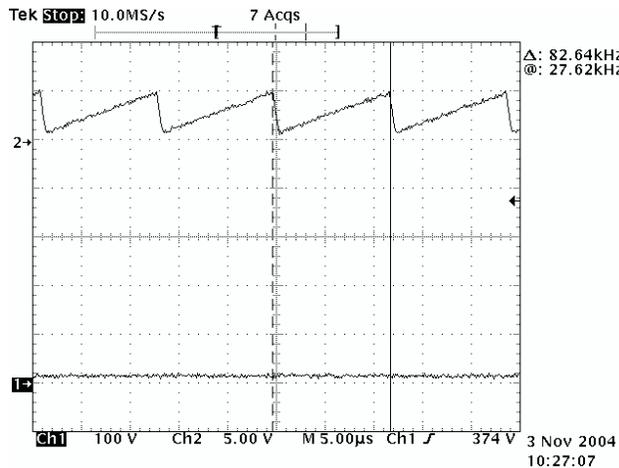


Figure 5. Crossover

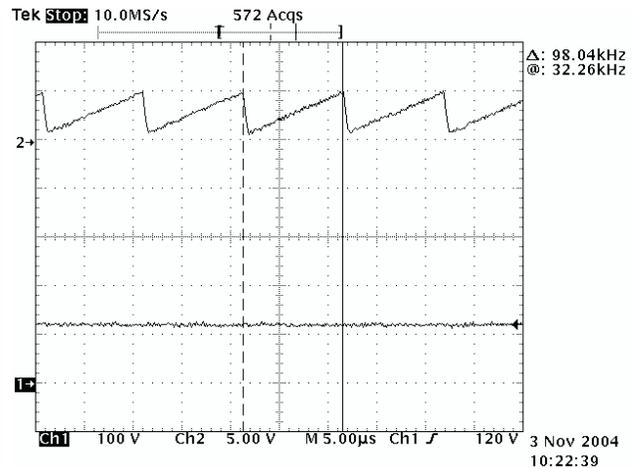


Figure 6. $V_{IN} = 85 V_{RMS}, 120 V$ Peak

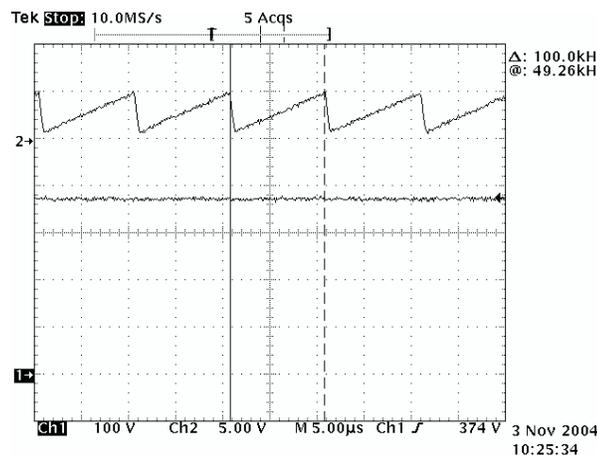


Figure 7. $V_{IN} = 265 V_{RMS}, 374 V$ Peak

8 Conclusion

The frequency dithering technique is presently being used in industry to reduce EMI. The circuitry presented in this paper when added to an active PFC pre-regulator can achieve 20% frequency dithering. This unique approach takes advantage of the internal timing circuitry that can be found in most PWMs to achieve frequency modulation.

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