Startup Current Transient of the Leading Edge Triggered PFC Controllers

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The leading edge triggered PFC converter controllers offer some advantages to the customer. The chief advantage is that the control chip operates in a manner that results in the PFC converter delivering current to the output capacitor at the same time the follow on converter is trying to take current from that same capacitor. This operation results in the RMS current in the output capacitor of the PFC being significantly reduced during operation.

The action of the switch of the leading edge triggered topology is such that the switch for the PFC is turned on when the ramp voltage of the clock crosses the voltage present on the output of the current error amplifier.

This system has an initial condition problem. When the chip is first powered the voltage on the output of the current error amplifier is clamped to ground as are the inputs. Further because the feedback configuration is for an integrating amplifier the output has a limited dv/dt capability. This results in the a large current transient on the initial powering up of the converter.

This can lead to overvoltage conditions on the output depending on the initial precharge state of the output capacitor and the initial input voltage conditions.

The solution to this is the addition of a circuit to clamp the initial peak current limit to a significantly lower value than the designed peak limit. This clamp quickly releases and allows the current peak limit to increase but by then the current error amplifier has taken over control.

This is accomplished by the attached circuit, Figure 1. The diagram is with respect to the circuit on page 13 of the UCC38500 datasheet, SLUS419.

The resistor R29 from V_{REF} to PKLIMIT is split in two R29A and R29B. These two resistors add to the previous value with the resistor connected to V_{REF} equal to 1/3 of the previous value and the resistor connected to PKLIMIT equal to 2/3 of the previous value. The emitter of an added PNP signal transistor (Q100) is connected to the junction of these two resistors. The collector of the transistor is connected to ground. The base of the transistor is connected to the junction of an added resistor (R100) and added capacitor (C100). The other side of the added capacitor is connected to ground and the other side of the resistor is connected to VREF. This ratio of R12a to R12b makes certain the transistor is off once the capacitor is fully charged.

When the controller is first powered the voltage across the added capacitor C100 is zero and it holds the transistor on, holding the voltage at the junction of R29A and R29B at close to ground. This reduces the peak current limit that the converter can generate. As the voltage across the capacitor (C100) increases by the charging current through R100 the voltage on the junction of R29A and R29B increases allowing the peak current to increase until the effects of the added circuit are eliminated and the peak current limit is as per the initial design. The selection of C100 and R100 should be such that the time constant is less than any soft start circuits on either the PFC or the down stream converter.

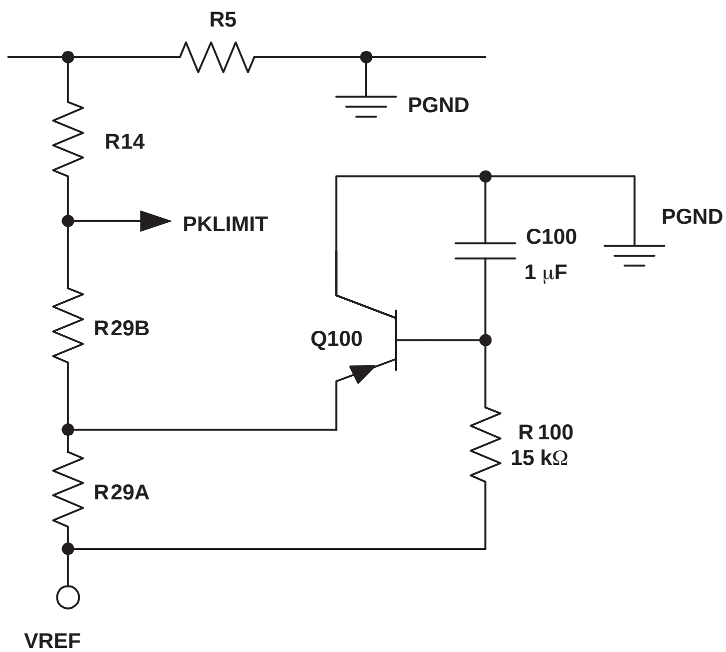

Figure 1. Modifications to Overcome Startup Current Transient

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