

# Load-Sharing TPS40050 Modules Using the UCC39002 Load-Share Controller

Lisa Dinwoodie

System Power

#### ABSTRACT

This application report features the UCC39002 BiCMOS 8-pin load-share controller and specifically illustrates equal current sharing between two TPS40050 synchronous buck controlled modules. The TPS40050 wide-input synchronous buck controller was used to convert a  $12 V_{DC}$  bus to  $1.8 V_{DC}$ , a common voltage to meet the demands for many modern electronic applications. The TPS40050 controller provides the necessary control and drive functions to implement these converters with the added benefit of high efficiency and small size. The individual converter design operates at 300 kHz and delivers 1.8 V at 15 A. In order to supply 30 A to the load, without completely redesigning the existing circuit, two TPS40050 converters were paralleled using the UCC39002 load-share controller. The result is a known converter design; complete with all of the original desired features, in a modular, higher current application.

### 1 Introduction

The UCC39002 is an advanced, high performance, low cost load-share controller that provides all the necessary functions to parallel multiple independent dc-to-dc modules. The UCC39002 can easily parallel currently available and popular synchronous buck converters, such as those designed with the TPS40050 controller. This design maintains all of the desirable features of the individual TPS40050 dc-to-dc converter but is capable of providing twice the load current with less than 1% current-share error at full load. The TPS40050 design used in the report is similar to the TPS40051EVM and is detailed in the product folder development tool which converts a +12-V bus to +1.8 V at 15 A.

### 2 Features

- Based upon the TPS40051 evaluation modules, detailed in Reference[1]
- Input voltage range of 10 V<sub>DC</sub> to 14 V<sub>DC</sub>
- 1.8-V output voltage at 30 A<sub>DC</sub>
- Less than 1% current-share error at full load
- Single wire load-share bus
- Able to start into full system load

### 3 Schematic

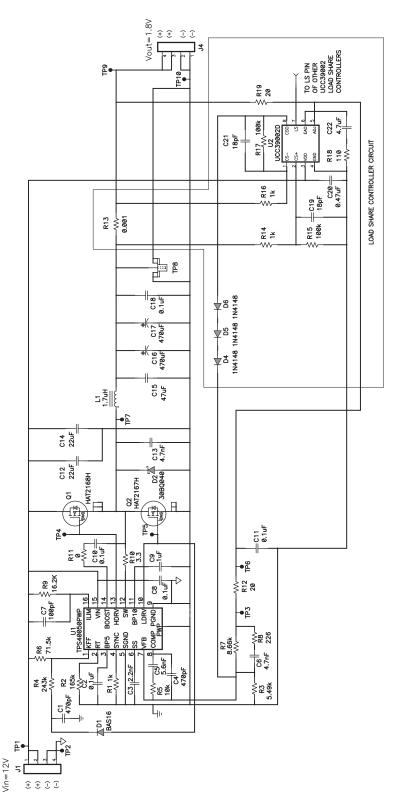


Figure 1. Schematic of TPS40050 Module with the UCC39002 Load-Share Circuit

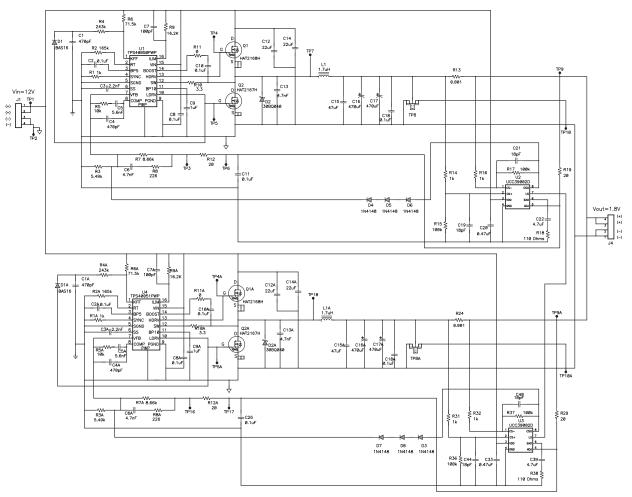


Figure 2. Complete Schematic Showing Two TPS40050 Converters in Parallel



### 4 Circuit Discussion

#### 4.1 Using the TPS40050 Instead of the TPS40051

The load-share design shown in Figures 1 and 2 is based upon the TPS40051 evaluation module but replaces the synchronous buck controller circuit with the TPS40050 device. This is due to the fact that the TPS40051 output stage has the capability to both source and sink drive currents whereas the TPS40050 is limited to only sourcing output drive currents. Load sharing multiple modules requires each individual module to start up into a pre-biased load and not sink current supplied by other modules supporting the output. Detailed analysis of the TPS40051 circuit performance can be found in the device's product folder.

#### 4.2 Starting into a Full System Load

One of the features of the TPS40050 synchronous buck converter design is a high-side current limit. While this is desirable in an individual converter, the full system load for paralleled converters usually exceeds the set over-current trip point for an individual module. Due to component tolerances and production variances, the start up profiles of any two modules will be slightly different. When one TPS40050 module starts up into a full system load of 30 A before another, the over-current hiccup response will be triggered. To prevent this, three diodes were added to form an offset voltage between the feedback node of the TPS40050 and the normal operation of the CSO in the UCC39002. When the load-share controller's CSO output rises beyond its normal operating range of 15 A individual output current, it begins to forward bias the diodes and drives current into the TPS40050's feedback node, thereby driving the output voltage low, limiting the output current. The diode forward voltage will vary over temperature which will result in the current limit also varying over temperature. The current limit due to temperature will be higher at low temperature and lower at high temperature. The result is a simple solution with a desirable temperature coefficient to minimize stresses on the circuit.

#### 4.3 Load-Share Design Details

#### 4.3.1 UCC39002 Bias

The UCC39002 load-share controller requires a minimum bias voltage,  $V_{DD}$ , of 4.575 V to ensure enabling the load-share bus. The 12-V input to the non-isolated TPS40050 converters was used to bias the UCC39002 controllers directly. The signal ground plane of the TPS40050 circuit served as the ground reference and –Sense for the load-share circuit.

$$V_{DD} = 12 V$$

### 4.3.2 Unity Gain Crossover Frequency of the TPS40050

The unity gain crossover frequency was provided in the closed loop performance discussion of the TPS40051 based design user's guide<sup>(1)</sup> and shown in Figure 3. The crossover frequency,  $f_{CO(module)}$ , was measured to be 11 kHz.

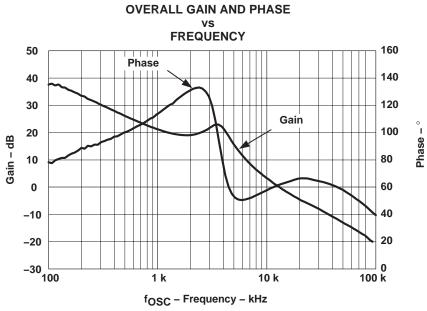


Figure 3. Unity gain crossover frequency of the TPS40050 converter

#### 4.3.3 Current Sensing

The output adjustment range of the load-share circuit was selected to be 2% of the total output voltage. Selecting a sense resistor value of 1 m $\Omega$  limited the power dissipation to less than 1/4 W and left plenty of margin, approximately 21 mV, for output voltage adjustment after the 15-mV voltage drop across this resistor at full load was accounted for. The current sense resistor for the UCC39002 current sense amplifier was placed in series with the output capacitors and the output connector of the TPS40050 circuit for high-side current sensing. The current sense output, V<sub>CSO(max)</sub>, of the UCC39002 is limited to an absolute maximum voltage of 2 V less than the V<sub>DD</sub> bias voltage of the device, or 10 V. This means the current sense amplifier gain, A<sub>CSA(max)</sub>, can not be greater than approximately 600 in order to keep the amplifier out of saturation:

 $V_{\rm CSO(max)} = VDD - 2 V$ 

 $R_{SENSE} = 1 \ m\Omega$ , designated as R13 in Figure 1

 $I_{OUT(max)} = 15 A$ 

for each converter

$$A_{CSA(max)} = V_{CSO(max)} / (R_{SENSE} \times I_{OUT(max)})$$

The gain across the current sense amplifier, A<sub>CSA</sub>, was chosen to be 100 and a high frequency pole set at approximately 100 kHz was added for noise filtering.



### 4.3.4 Determining R<sub>ADJUST</sub>

The input to the resistor divider circuit of the voltage feedback for the TPS40050 module was disconnected from the output voltage bus and connected to the ADJ pin of the load share controller. Then, a resistor was placed in series between this ADJ pin and the output voltage bus of the TPS40050, creating an artificial Sense+ voltage from the voltage drop across R<sub>ADJUST</sub> due to the current sunk by the internal NPN transistor. The voltage at the ADJ pin must be maintained at approximately 1 V above the voltage at the EAO pin. This is necessary in order to keep the transistor at the output of the internal adjust amplifier from saturating. To fulfill this requirement, R<sub>ADJUST</sub> can be calculated using the following equation:

$$R_{ADJUST} \geq \frac{\left[ \varDelta V_{ADJ(\max)} - \left( I_{OUT(\max)} \times R_{SENSE} \right) \right] \times 500 \,\Omega}{\left[ V_{OUT} - \left[ \varDelta V_{ADJ(\max)} - \left( I_{OUT(\max)} \times R_{SENSE} \right) \right] - 1 \,V \right]}$$

 $R_{ADJUST} \ge 13.5 \, \Omega$ 

Also needed for consideration is the actual adjust pin current. The maximum sink current for the ADJ pin,  $I_{ADJ(max)}$ , is approximately 6 mA as determined by an internal 500- $\Omega$  emitter resistor and 3-V clamp. The value of the adjust resistor,  $R_{ADJUST}$ , is based upon the maximum adjustment range of the module,  $\Delta V_{ADJ(max)}$ . This resistor is determined using the following formula:

$$R_{ADJUST} \geq \frac{\left[ \varDelta V_{ADJ(max)} - \left( I_{OUT(max)} \times R_{SENSE} \right) \right]}{I_{ADJ(max)}}$$

 $R_{ADJUST} \ge 3.5 \, \Omega$ 

By selecting a 20- $\Omega$  resistor for R<sub>ADJUST</sub>, designated as R19 in Figure 1, the ADJ pin will be at least 1.25 V greater than the EAO voltage and the adjust pin sink current will not exceed its 6 mA maximum.

#### 4.3.5 Error Amplifier Compensation

The total load-share loop must be configured for a unity gain crossover frequency well before the crossover frequency of the module,  $f_{CO(module)}$ , as shown in Figure 3. This is best accomplished by placing a zero in the error amplifier compensation at least one decade before the module's crossover frequency. Taking advantage of the relatively high crossover frequency of the module, this design places the zero at almost two decades before it, at 300 Hz. Compensation of the transconductance error amplifier is done by placing the compensation resistor,  $R_{EAO}$ , and capacitor,  $C_{EAO}$ , between EAO and GND. The values of these components are determined by the following loop gain equations and the closest available value components are used:

$$C_{EAO} = \left(\frac{Gm}{2 \times \pi \times f_{ZERO}}\right) (A_{CSA}) (A_{V}) (A_{ADJ}) (A_{PWR(fco)})$$

 $C_{FAO} = 4.7 \,\mu$ F, designated as C22 in Figure 1

Where:

- Gm is the transconductance of the error amplifier, typically 14 ms,
- f<sub>ZERO</sub> is equal to the desired frequency in Hz of the zero to be added to the load-share loop,
  - f<sub>ZERO</sub> = 300 Hz
- A<sub>CSA</sub> is the gain across the current sense amplifier,
  - $A_{CSA} = 100$
- A<sub>V</sub> is the voltage gain,
  - $A_V = R_{SENSE}/R_{LOAD}$
  - $R_{LOAD} = V_{OUT}/I_{OUT(max)}$
- A<sub>ADJ</sub> is the gain associated with the adjust amplifier,

- A<sub>ADJ</sub> = R<sub>ADJUST</sub>/500  $\Omega$ 

 A<sub>PWR(fCO)</sub> is the measured gain of the power module at the desired inserted zero frequency, 30 dB according to Figure 3 and converted from dB to 31.6 V/V.

Once the C<sub>EAO</sub> capacitor is determined, R<sub>EAO</sub> is selected to achieve the desired loop response:

$$R_{EAO} = \frac{1}{\left(2 \times \pi \times C_{EAO(actual value used)} \times f_{ZERO}\right)}$$

 $R_{EAO} = 110 \, \Omega$ , designated as R18 in Figure 1

## 5 Test Results

As shown in Figure 4, at full load, the TPS40050 converters performed with a load-share error of less than 0.9%. The modules were sharing within 10% load-share error at less than 25% full-system load.

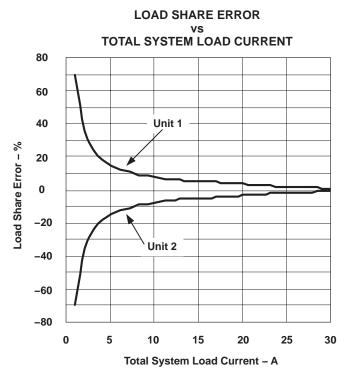


Figure 4. Load-Share Error Results of Paralleling Two TPS40050 Converters

### 6 Teat Board Layout

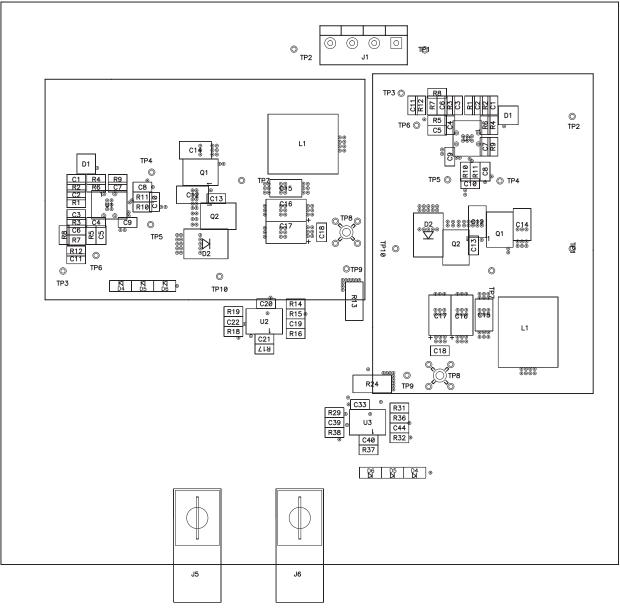


Figure 5. Top Side Component Assembly

The large rectangular outlines show the size of the original TPS40050 converter modules.



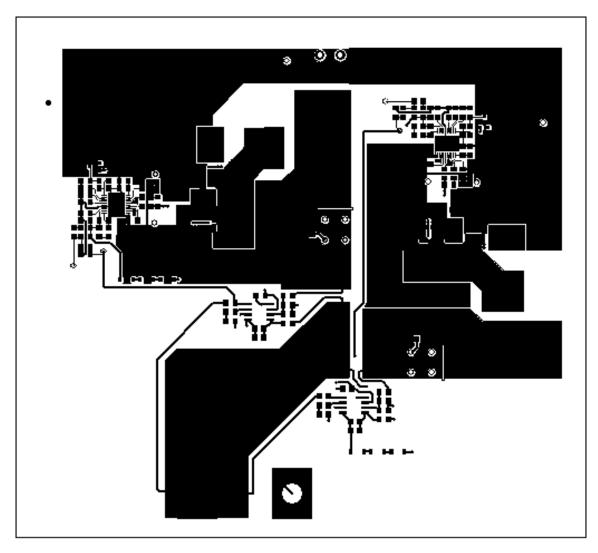
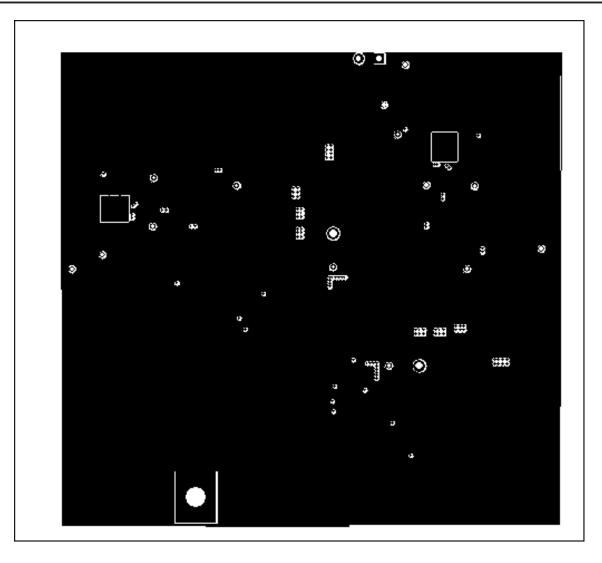


Figure 6. Top Side Copper





### 7 References

- 1. Dennis, Mark, *TPS40051–Based Design Converts 12-V Bus to 1.8 V at 15 A (SLUP195)*, Texas Instruments Literature Number SLUU161
- 2. Dinwoodie,Lisa, UCC39002 Advanced Load-Share Controller's User's Guide, HPA027A, Texas Literature Number SLUU116A
- 3. Advanced 8-Pin Load Share Controller, Texas Instruments Literature Number SLUS495B
- 4. *Wide-Input Synchronous Buck Controller*, Texas Instruments Literature Number SLUS540D

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