Application Report
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Buffer Op Amp to ADC Circuit Collection

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ABSTRACT

This document describes various techniques that interface buffer op amps to ADCs. These techniques provide designers with a toolkit of ideas that can be readily adapted to their application. Fully differential, transformer coupled, and single-ended techniques are described. Reference techniques and circuits are also described in Appendix A.

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1 Introduction

In most cases, analog to digital converters (ADCs) also require a buffer amp. The choice of buffer op amp, and how to connect it to the ADC, are some of the most challenging tasks facing experienced analog designers—much more so with digital designers who are often assigned the task. This document presents designers with a library of interface techniques, but leaves the choice of op amp to other documents. In general, however, op amp specifications that are important to the system design should be much better than the equivalent specification of the ADC Otherwise, money is wasted on an expensive ADC. A good buffer op amp is usually an order of magnitude less expensive than the ADC, and economizing on a buffer op amp is a poor decision.

This document assumes a differential input ADC, which is standard for high performance ADCs. Section 2 describes the input and reference scheme of differential op amps.

1.1 Interface Architectural Scheme

Designers should first decide on an architectural scheme to interface to the ADC. There are three schemes to choose from:

- **Fully differential op amps:** The best performance comes when fully differential ADCs are buffered with fully differential op amps.

- **Transformer coupling:** This is also a commonly used method, but it has significant limitations such as frequency response, dc blockage, and the size, cost, and lack of standardization of the transformer.

- **Single-ended op amps:** If a fully differential op amp cannot be selected to meet system performance requirements, one or more single-ended op amps may be used to simulate fully differential architecture.

There are several choices to be made within each architectural category. These are dictated by system constraints and include:

- Single-ended input signal vs fully differential input to the buffer op amp.

- Single-ended interface to the ADC (where one input is tied to a reference or a common mode level) vs fully differential input. Single-ended input should only be used when performance and accuracy are not of paramount importance, but board space and cost are.

- AC-coupled vs dc-coupled signal chain. Most RF and audio applications can be ac-coupled, which greatly simplifies design. Many transducer interface applications must be dc-coupled.

- Single-supply vs dual-supply power. The vast majority of applications are single supply, as the ADC is probably operated from a single supply and its input range is entirely within a positive range that does not include ground. A single supply op amp whose supply voltage matches that of the ADC is preferable—to avoid the possibility of damage to the ADC.

There may be performance constraints on the op amp, however, that dictate the use of a dual supply variety.

These four items give 16 different possibilities—and in some cases there are multiple implementations for each possibility. Fortunately for the designer, not all of these combinations make sense. Transformer coupled applications, for example, do not need to include dc coupled cases because the transformer itself blocks dc. Fully differential op amp configurations do not use a single-ended connection scheme to the ADC. It makes no sense to purchase a fully differential op amp, and then not use the differential output to interface to the differential input of the ADC. In most cases, the dual supply implementation is a trivial change from the single-supply implementation, so schematics may not be included.

1.2 Circuit Icons

For the designer's convenience, reference icons are included with each schematic to allow the designer to quickly identify the configuration being discussed:

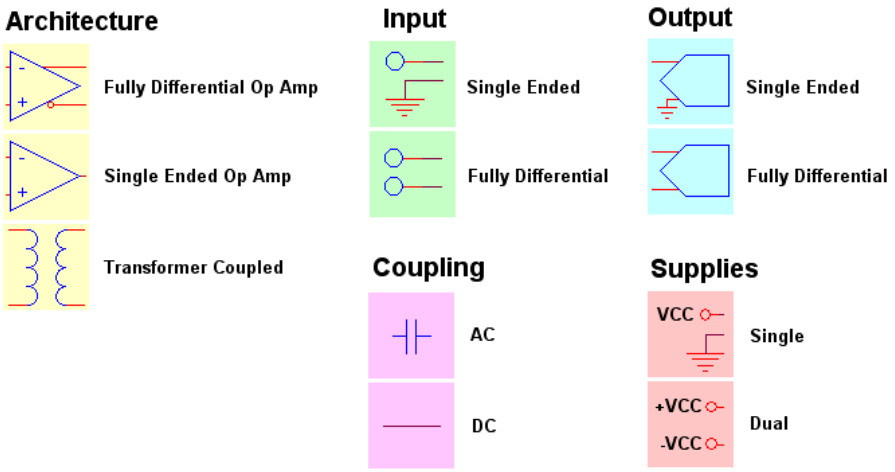


Figure 1. Circuit Configuration Icons

Icons are also included that give the designer a quick *heads up* on design scheme limitations. These icons are:

ADDITIONAL COST: Using this circuit requires additional active circuitry, usually to buffer the reference.

DIFFICULT CALCULATIONS: The circuit calculations are beyond simple algebra, and require iteration or goal seeking. Texas Instruments provides engineering tools on its web site for these cases.

ADDITIONAL POWER: The circuit draws more current than the designer might be expecting due to consumption in passive components. The designer should double check the wattage of resistors, and be aware that the op amp may consume more power on one feedback path and / or power supply than the other.

MATCHED RESISTORS REQUIRED: The designer should be aware that matched resistors are needed in the two feedback paths of fully differential circuitry—even if it is implemented with single-ended op amps. This icon is not included for those cases. It is intended to warn designers that matched resistors are needed elsewhere in the circuit, in an unexpected location. The text accompanying the schematic spells this out.

MISMATCHED POTENTIALS: The common-mode potential of the buffer op amp may be slightly different than that of the ADC, because the common-mode potential for the buffer op amp comes from a different source than the CM pin of the ADC.

1.3 Schematic Conventions

Some conventions and simplifications to follow are noted in the schematics of this application note. These conventions allow the designer to see the important details of implementation, without getting caught up in details that are covered in ADC data sheets, or in other application notes.

1.3.1 ADC Details

ADC power supply connections, digital and control interfaces, and other pins are not shown. This application note is primarily concerned with analog input and common mode reference techniques for ADCs, and the designer is left with the job of connecting data busses, logic control lines, etc. It is assumed that the designer is already familiar with these topics, and needs no help other than that provided in the ADC data sheet. The designer is also responsible for the power supply connections of the ADC, and decoupling those connections properly. In passing, however, it is recommended that analog and digital power and ground connections of the ADC be made to the analog power and ground system exclusively. The ADC chip designers actually rely on the circuit designer to make these connections externally, as it is difficult to create low enough impedance connections internal to the chip.

1.3.2 Decoupling

Refer to Reference 1 for proper decoupling techniques. It explains how to select capacitors to maximize system performance and minimize noise. Designers should analyze the nature of noise in their system, both conducted from the system itself, and radiated into it—and then select capacitors that are self-resonant at those frequencies.

These schematics omit some decoupling capacitors, but not all. Op amp power supply connections are shown only to differentiate between single-supply and dual-supply operation. Even though it is not shown, these connections must be properly decoupled. Decoupling capacitors that appear in unexpected locations are included, but the value is not specified.

ADC data sheets specify decoupling techniques for their reference outputs. The designer is responsible for decoupling these references.

1.3.3 ADC Compensation Components

ADC inputs can present a substantial capacitive load to the buffer op amp. This invites instability, particularly at high frequencies. ADC data sheets suggest compensation components. These components are included on these schematics, because it is not immediately evident in all cases where to place them.

1.3.4 Termination Resistors

Many high-speed applications employ termination resistors, with 50 Ω being the most common value. Video systems may employ 75 Ω, and other values are possible, particularly in RF systems. Most of these schematics include termination resistors. If they are not needed, the designer can simply omit them.

1.3.5 Reference Buffers

In some cases, the drive capability of the ADC reference outputs is not enough to source or sink current required by the buffer op amp circuitry. In these cases, a generic buffer amp symbol is used to represent the fact that more drive is required. The designer is responsible for ensuring that enough drive / sink capability is present in the ADC, and buffering it if there is not enough drive. Appendix A makes some suggestions on how to implement these circuits.

2 ADC Input and Reference Structure

The vast majority of data converters contain references, which are meant to make the designer's job easier by providing the converter's internal reference to op amp buffer circuitry.

The exact architecture of reference and input circuitry varies greatly. A survey of data converters manufactured by Texas Instruments reveals several different architectures. Combining the wide range of possible input signals and power supply voltages leads to a great variety of circuits. Therefore most data acquisition systems are custom designs. In addition, this note shows some of the more creative implementations for ADC circuits. This in no way limits the designer to the applications shown here—there are many possibilities.

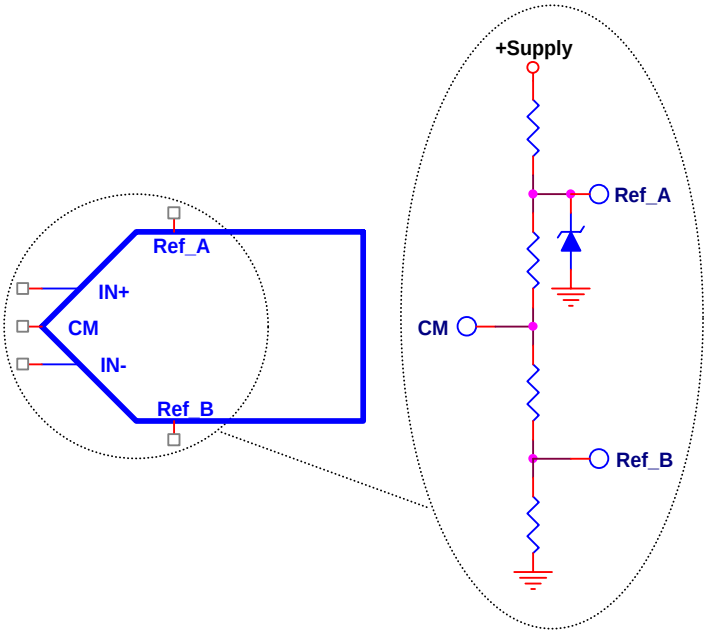


Figure 2. Reference Structure of Common ADCs

Figure 2 shows a simplification of a typical reference structure. Power for an internal ADC reference (REF_A) is derived from the positive power supply. The reference structure is completed by an internal precision resistor voltage divider. The absolute value of these resistors is usually specified over a range that may be more than 20%, but they are carefully matched to give very precise ratios. The three taps in the voltage divider chain represent the following voltage levels:

- Reference A (Ref_A) represents the value of input voltage (IN+ – IN-) that produces a pattern of all logic high at the data converter output.
- Reference B (Ref_B) represents the value of input voltage that produces a pattern of all logic low at the data converter output.
- Common Mode (CM) represents the value of input voltage that produces a mid-scale pattern at the data converter logic output (the value at which the most significant digit in the data bus switches from 0 to 1).

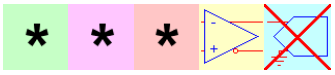
Some ADCs omit the common mode output, and include only Ref_A and Ref_B outputs. Other data converters may only have the common mode output, or may only have one reference. In general, however, high precision ADCs have all three. Some ADCs may have internal buffers for Ref_A, Ref_B, and / or CM – and these buffers have to be disabled by a logic level on a control pin if external voltages drive them. The designer should consult the ADC data sheet and fully understand its unique architectural features before committing to a buffer op amp interface circuit.

3 Fully Differential Op Amp Architecture

By far, the most important innovation for ADC interfacing in recent years has been the introduction of new models of fully differential op amps. These components have fully differential outputs that are ideal for connection to the fully differential inputs of ADCs.

The chief advantage to using a fully differential op amp is reduced second order harmonic distortion—which is particularly important in communications systems. This advantage can only be realized, however, if the resistors used for gain and feedback are well matched. Traditional 1% resistors do not provide much improvement over other techniques.

It makes no sense for a designer to purchase a fully differential op amp, and then use single-ended techniques to interface to a fully differential ADC, so those circuit configurations are not shown:



3.1 Single-Ended Input, AC-Coupled, Single Supply

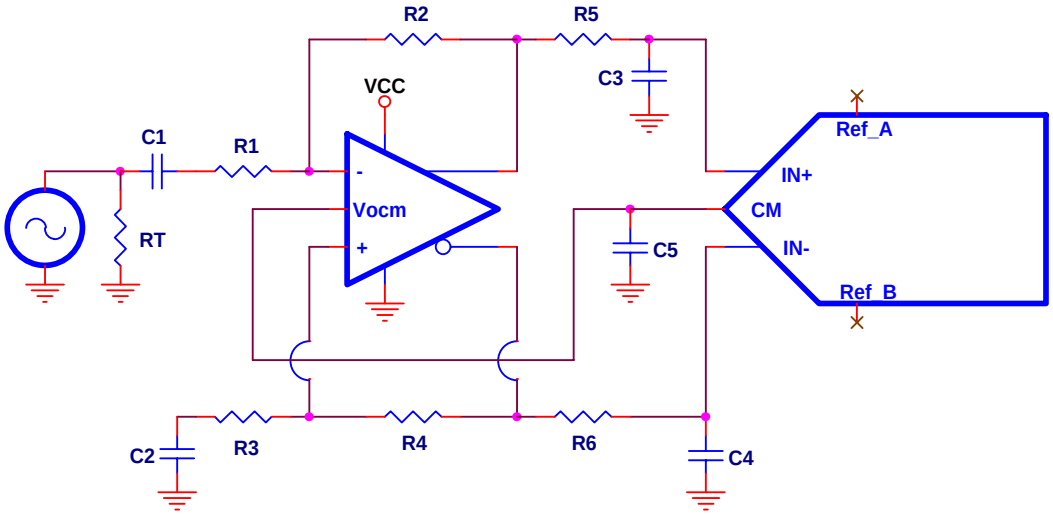


Figure 3. Single-Ended Input, AC-Coupled, Single Supply

In Figure 3, a source is terminated with a termination resistor RT. Capacitors C1 and C2 are dc blocking capacitors (consult Reference 3 for more information). Designers should note that C2 is important in establishing a correct dc operating point for the circuit. Resistors R1 through R4 set the gain of the fully differential op amp. R5, R6, C3, and C4 are ADC compensation components. Capacitor C5 decouples the common mode output of the ADC.

3.2 Single-Ended Input, AC-Coupled, Dual Supply

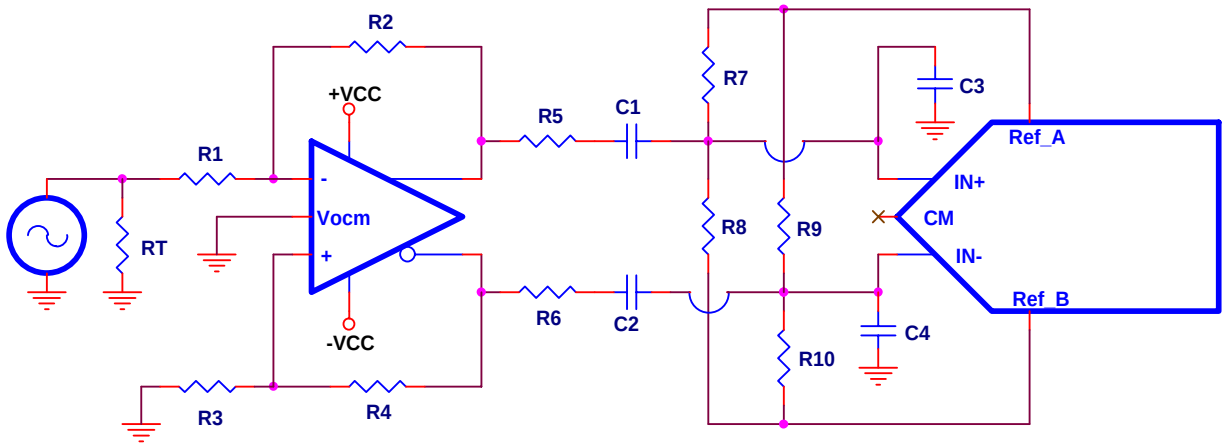
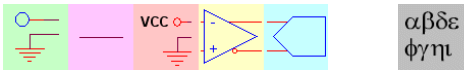


Figure 4. Single Ended Input, AC-Coupled, Dual Supply

This architecture presents a challenge for the designer. The termination resistor RT, in parallel with the source impedance, forms a portion of the gain resistor R1. Changing the gain resistor, of course, also changes the gain of the stage, and unbalances the top and bottom feedback pathways. Re-balancing the feedback paths changes the gain, etc. The design process is iterative, and goal seeking. Texas Instruments has an engineering design utility to handle this case. The utility can be accessed through the Texas Instruments web site.

Resistors R1 through R4 set the gain of the stage. Capacitors C1 and C2 are ac coupling capacitors. Resistors R7 through R10 sets the common mode voltage of the two inputs. R5, R6, C3, and C4 are ADC compensation components.

3.3 Single-Ended Input, DC-Coupled, Single Supply



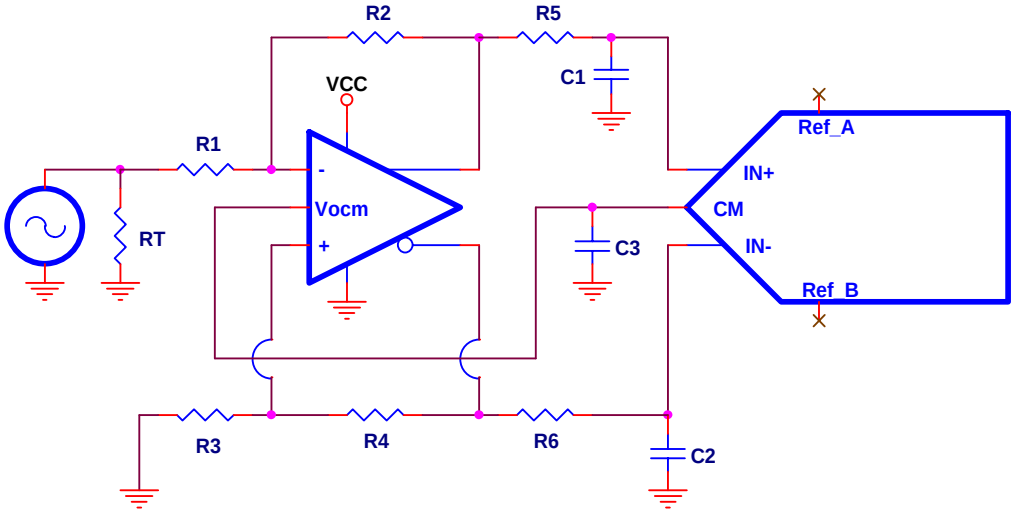
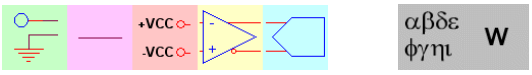


Figure 5. Single-Ended Input, DC-Coupled, Single Supply

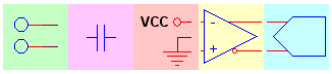
This is also a challenge for the designer. The termination resistor RT, in parallel with the source impedance, forms a portion of the gain resistor R1. Changing the gain resistor, of course, also changes the gain of the stage, and unbalances the top and bottom feedback pathways. Re-balancing the feedback paths changes the gain, etc. The design process is iterative, and goal seeking. Texas Instruments has an engineering design utility to handle this case. The utility can be accessed through the Texas Instruments web site.

3.4 Single-Ended Input, DC-Coupled, Dual Supply



The change to a dual supply for the op amp is trivial; simply replace the ground connection in Figure 5 with a connection to the negative potential. There is little advantage to doing this—the common mode range of the op amp is already set by the CM output of the ADC. This increases the power consumption of the circuit, and does nothing to decrease the complexity of calculation.

3.5 Differential Input, AC-Coupled, Single Supply



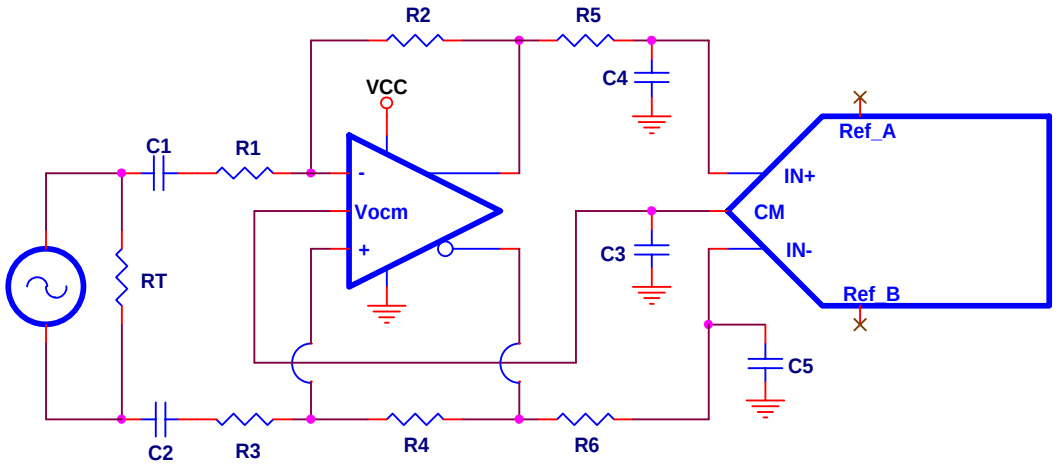
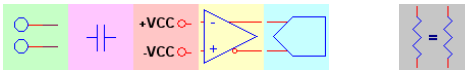


Figure 6. Differential Input, AC-Coupled, Single Supply

In Figure 6, a differential voltage source is terminated with a termination resistor RT. Capacitors C1 and C2 are ac-coupling capacitors. They should be equal in value to balance both feedback pathways of the op amp. The designer should remember that the capacitors appear in series and are effectively reduced to half their value. Resistors R1 through R4 set the gain of the fully differential op amp. R5, R6, C5, and C4 are compensation components specified on the ADC data sheet. Capacitor C3 decouples the common mode output of the ADC.

3.6 Differential Input, AC-Coupled, Dual Supply



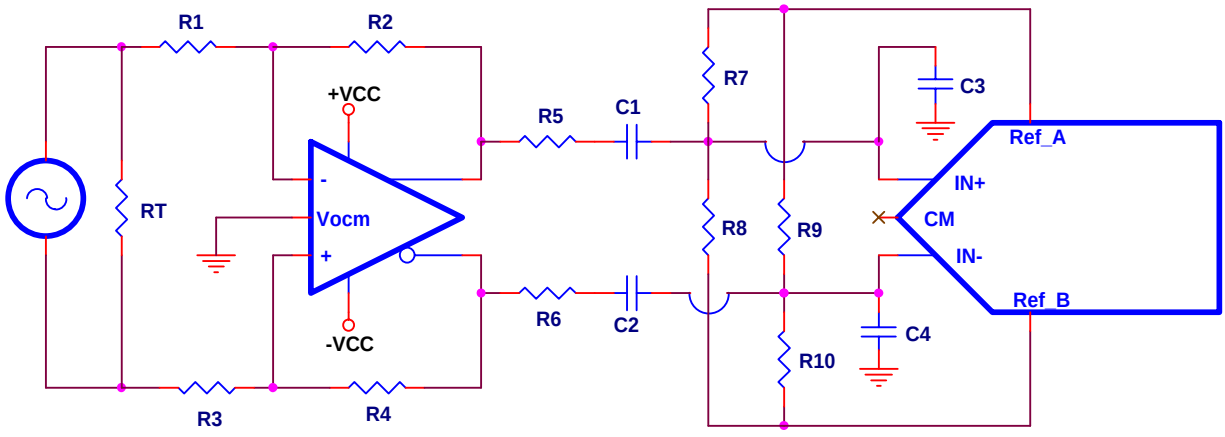


Figure 7. Differential Input, AC-Coupled, Dual Supply

In Figure 7, resistors R1 through R4 set the gain of the stage. Capacitors C1 and C2 are ac-coupling capacitors. Resistors R7 through R10 set the common mode voltage of the two inputs. R5, R6, C3, and C4 are ADC compensation components.

3.7 Differential Input, DC-Coupled, Single Supply

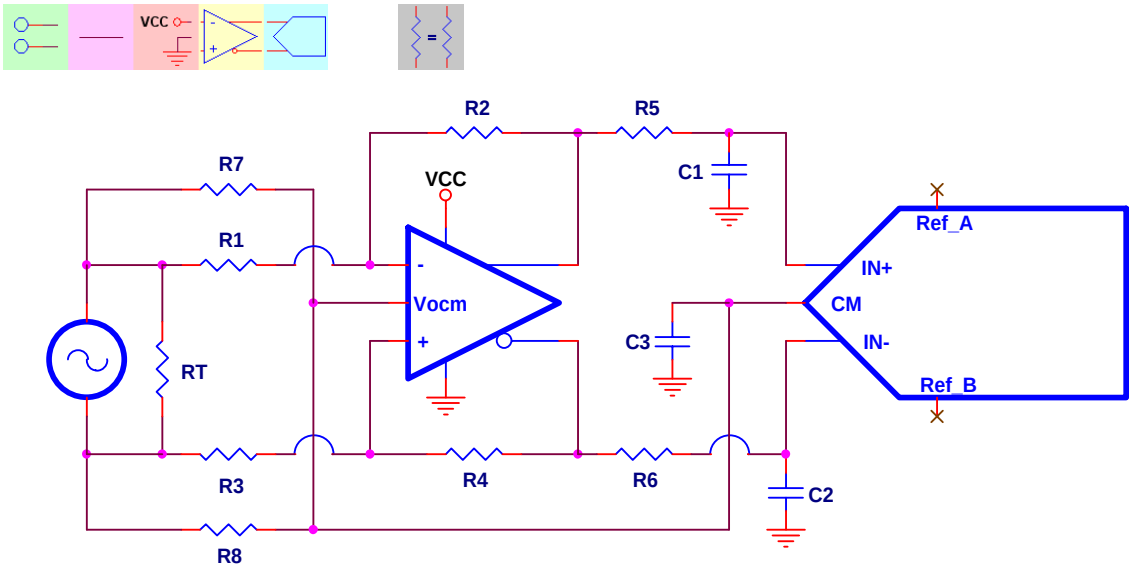


Figure 8. Differential Input, DC-Coupled, Single Supply—Common Mode From Source

In Figure 8, a differential voltage source is terminated with a termination resistor RT. Resistors R1 through R4 set the gain of the fully differential op amp. R5, R6, C1, and C2 are compensation components specified on the ADC data sheet.

The common mode voltage for this circuit comes from the source, and is bypassed by capacitor C3. Resistors R7 and R8, which must be matched, present the common mode potential to both the op amp and the ADC. The designer must be certain that the common mode voltage of the source, ± the ac amplitude of the source, is within the common mode limits and operational range of both the buffer op amp and the ADC. If this is not the case, then connect the common mode pin of the ADC to the Vocm input of the buffer op amp as shown in Figure 9. The common mode voltage appearing on the source is rejected, and the common mode voltage of the ADC becomes the common mode point of the circuit.

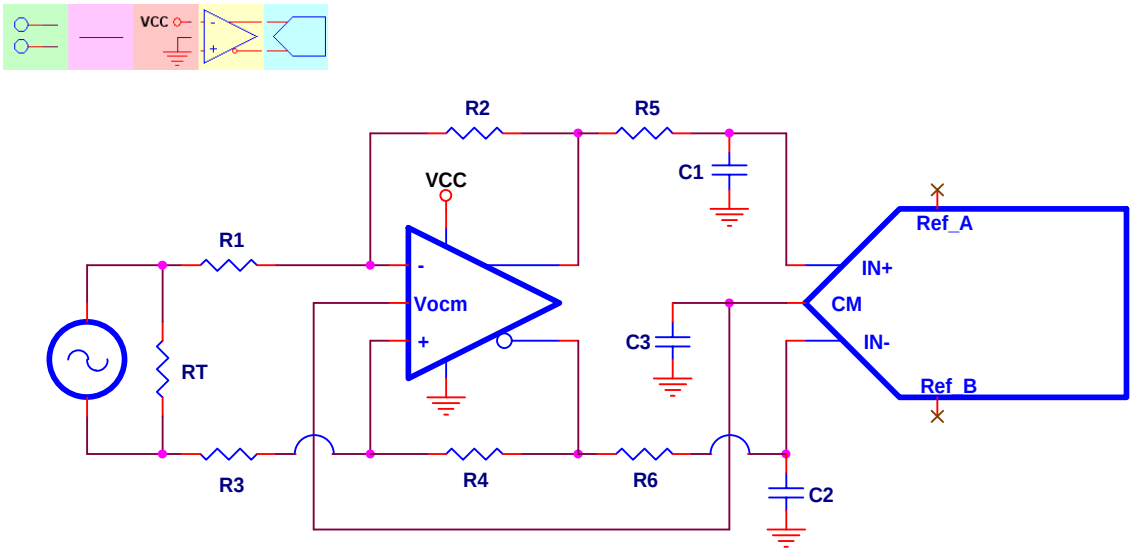
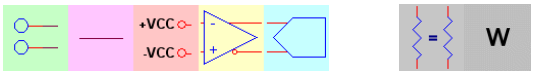


Figure 9. Differential Input, DC-Coupled, Single Supply—Common Mode From ADC

These circuits cannot accommodate a dc potential across the input, only a common mode dc voltage.

3.8 Differential Input, DC-Coupled, Dual Supply



The change to a dual supply for the op amp is trivial; simply replace the ground connection in Figures 8 and 9 with a connection to the negative potential. There is little advantage to doing this—the common mode range of the op amp increases, but not that of the ADC. This also increases the power consumption of the circuit.

3.9 Antialiasing Techniques With Fully Differential Op Amps

A relatively common application for fully differential buffer op amp interfaces is antialiasing filtering of the input. Traditionally this has been done with single pole filters, perhaps using two single (real) pole filters. The single pole technique works, but with a few extra components, the designer can implement a double pole MFB low pass filter as shown in Figure 10:

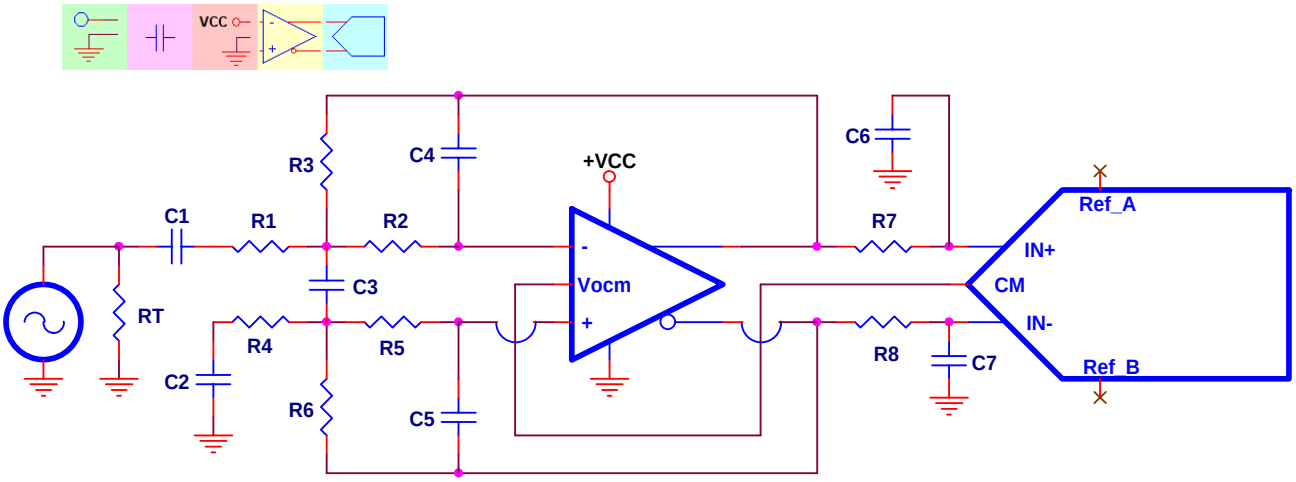


Figure 10. Antialias Filter Using a Fully Differential Op Amp

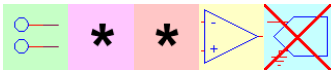
In Figure 10, a fully differential op amp is used as a two-pole MFB low pass antialiasing filter. As with any MFB filter, amplitude, ripple, and corner frequency all interrelate. A good reference on MFB design—or a good filter design program such as Texas Instruments Filter Pro™ should be used. Programs like Filter Pro design utilizing single-ended op amps, therefore C3 is the series combination of two capacitors from the separate feedback pathways, and therefore is half the value suggested by the reference or filter design program. The common mode point of the fully differential op amp is set by the ADC CM output. R7, R8, C6, and C7 are compensation components specified by the ADC data sheet.

The designer is reminded that ac-coupling Capacitors C1 and C2 form a single high-pass pole with resistors R1 and R4.

4 Single-Ended Op Amp Techniques

It is possible to drive a differential input ADC with conventional, single-ended op amps,although performance is not as good as with a fully differential op amp.

It makes little sense to interface a fully differential input source to a differential input ADC with a single ended technique, so those combinations are not shown.



This leaves twelve cases. Of these, the first four (the single-ended input / single-ended output cases) are the *low end* solutions. They throw away many of the advantages of fully differential input ADCs in return for minimizing components. Nevertheless, these cases are shown because many designers may be forced to use a fully differential ADC for system reasons, and yet not need to utilize full accuracy.

4.1 Single-Ended Output, Single-Ended Input, AC-Coupled, Single Supply

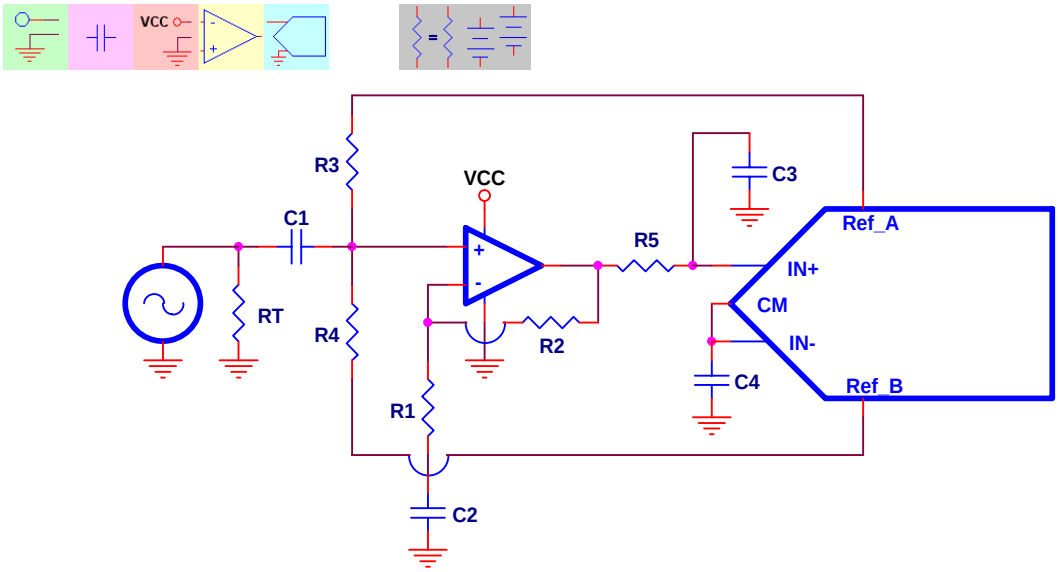


Figure 11. Single-Ended Output, Single-Ended Input, AC-Coupled, Single Supply

In Figure 11, the ADC IN- input is connected to the common mode output of the ADC, and decoupled with C4. This sets the input range of the ADC as the common mode voltage to +Ref_A. The input source is coupled through C1 to the noninverting input of the op amp. Non-inverting stage gain is set by R2 and R1. The local virtual ground is created from Ref_A and Ref_B though resistors R3 and R4, which should be equal in value. Capacitor C2 isolates the virtual ground potential. R5 and C3 are ADC compensation components.

This circuit may have a dc error due to the fact that the common mode input to IN+ is slightly different than the dc potential created by R3 and R4.

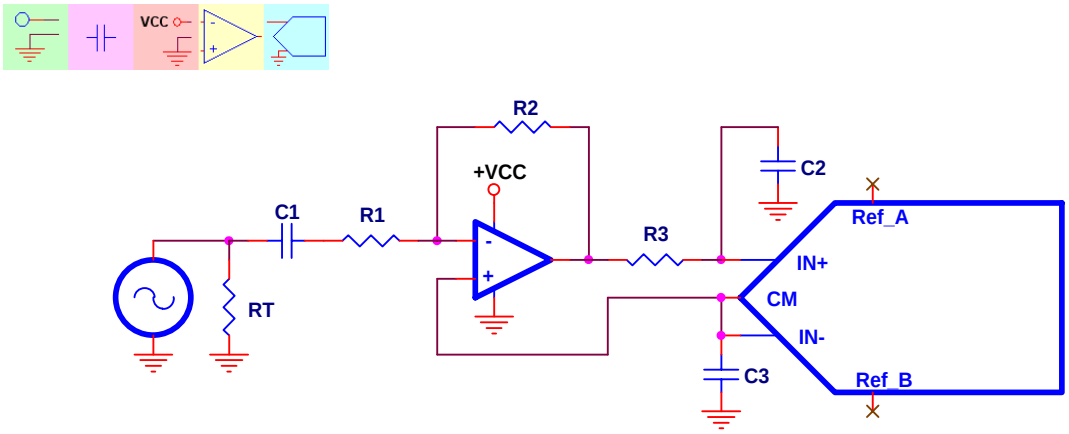


Figure 12. Single-Ended Output, Single-Ended Input, AC-Coupled, Single Supply

This circuit differs from the previous implementation in that the gain stage is inverting, and common mode voltage is injected into the noninverting input of the op amp instead of being derived from Ref_A and Ref_B. It has the advantage of having an accurate common mode voltage that comes directly from the ADC, but the disadvantage that the buffer circuit introduces a phase shift of 180°.

4.2 Single-Ended Output, Single-Ended Input, AC-Coupled, Dual Supply

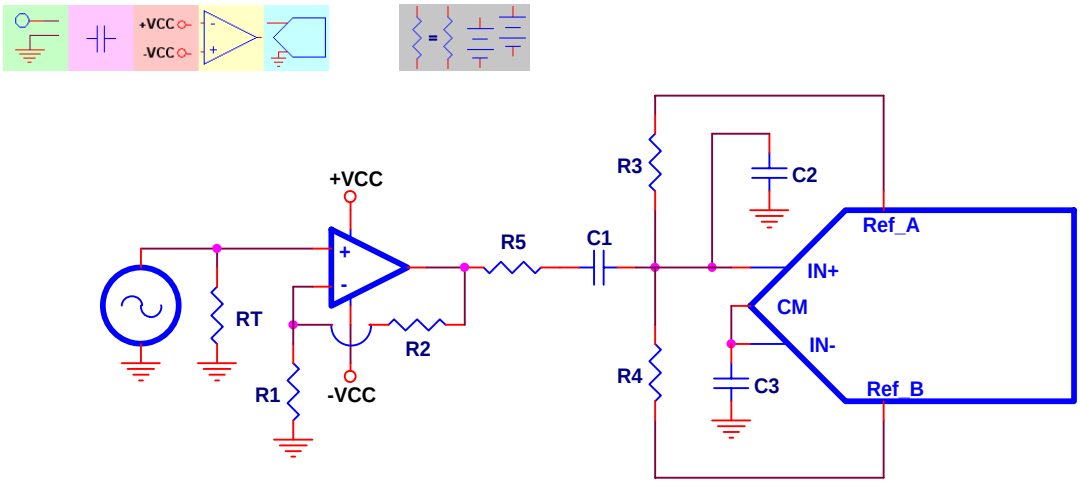


Figure 13. Single-Ended Output, Single-Ended Input, AC-Coupled, Dual Supply

In Figure 13, the ADC IN- input is again connected to the common mode output of the ADC, and decoupled with C3. This sets the input range of the ADC as the common mode voltage to +Ref_A. The input source is coupled to the noninverting input of the op amp. Noninverting stage gain is set by R2 and R1. The op amp stage output is ac coupled through capacitor C1. The local virtual ground for IN+ is created from Ref_A and Ref_B though resistors R3 and R4, which should be equal in value. R5 and C2 are ADC compensation components.

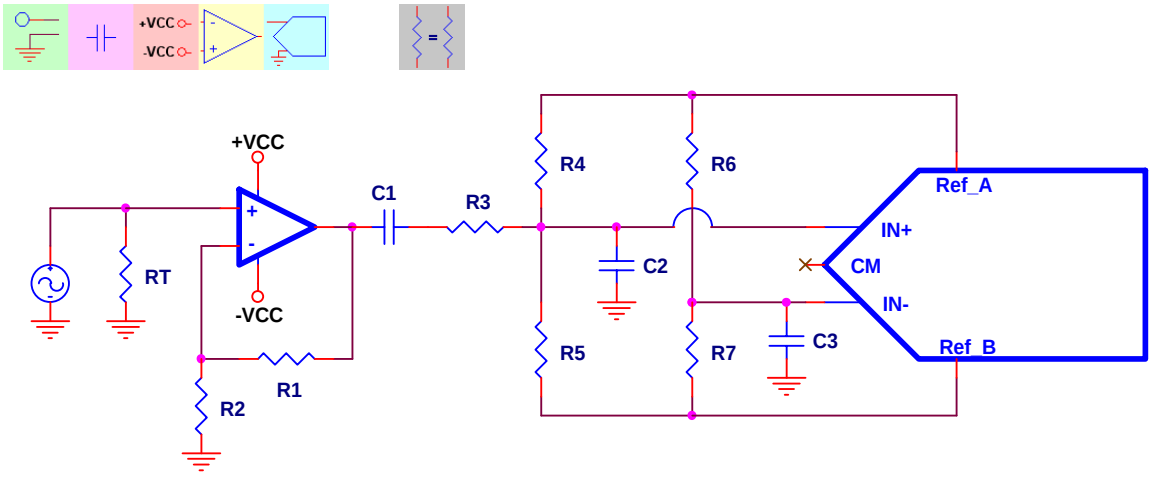


Figure 14. Single-Ended Output, Single-Ended Input, AC-Coupled, Dual Supply

Figure 14 shows an example of a single-ended input ac-coupled to an ADC, which is used as if it were a single-ended converter. R1 and R2 are selected to provide non-inverting gain. C1 is a dc-blocking capacitor. R3 and C2 are ADC compensation components. R4 through R7 are equal in value, and are used to provide a derived common mode voltage to both the IN+ and IN- inputs. IN- is held at the common mode voltage, and bypassed by capacitor C3.

4.3 Single-Ended Output, Single-Ended Input, DC-Coupled, Single Supply

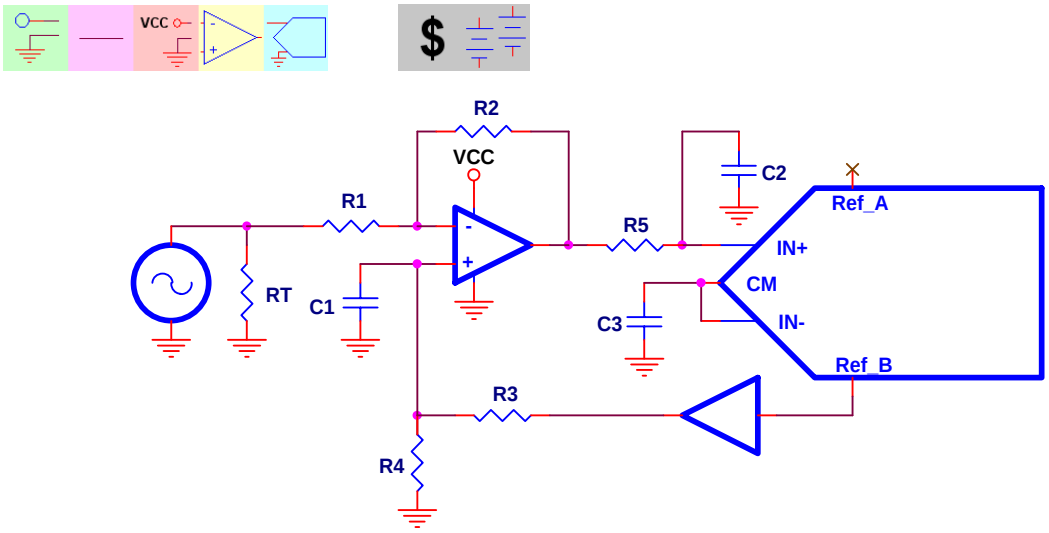
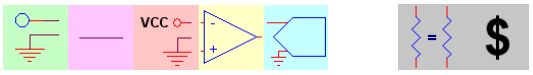


Figure 15. Single-Ended Output, Single Ended Input, DC Coupled, Single Supply

In Figure 15, the ADC IN- input is again connected to the common mode output of the ADC, and decoupled with C3. This sets the input range of the ADC as the common mode voltage to +Ref_A. Resistors R1 and R2 set the inverting gain of the op amp. Because it is dc-coupled, the designer needs to consider the dc offset of the source, and the dc gain of the stage. Reference B is buffered and used to generate the common mode point of the stage through voltage divider resistors R3 and R4. The noninverting dc gain of the stage on this common mode voltage must also be considered in the design. Capacitor C1 decouples the common mode voltage of the stage. Resistor R5 and capacitor C2 are ADC compensation components.

This circuit has a potential dc offset error, because the common mode voltage level at the op amp may not perfectly match that of the ADC.



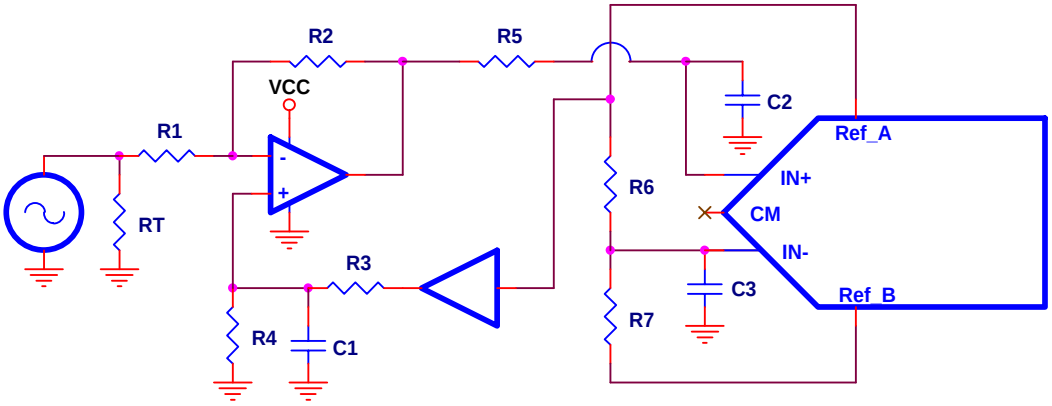
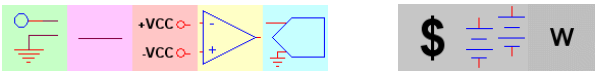


Figure 16. Single-Ended Output, Single-Ended Input, DC-Coupled, Single-Supply

Figure 16 shows an example of a single-ended input dc coupled to an ADC, which is again used as if it were a single-ended converter. R1 and R2 are selected to provide inverting gain. The noninverting input is used to input a dc reference derived from Ref_A, which is divided to the correct level by resistors R3 and R4. The op amp provides noninverting dc gain on this divided reference, boosting it to the common mode voltage level of the ADC. R6 and R7 generate the same common mode voltage and supply it to the ADC on its IN- input. C1 and C3 are decoupling capacitors. R5 and C2 are compensation components specified by the ADC data sheet.

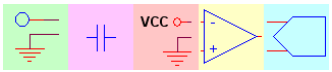
This circuit is not as desirable as some others, because it is difficult to keep the reference provided to the op amp at the same level as the reference presented to the ADC.

4.4 Single-Ended Output, Single-Ended Input, DC-Coupled, Dual Supply



The change to a dual supply for the op amp is trivial; simply replace the ground connection in Figure 15 or 16 with a connection to the negative potential. There is little advantage to doing this since it increases the power consumption of the circuit.

4.5 Differential Output, Single-Ended Input, AC-Coupled, Single Supply



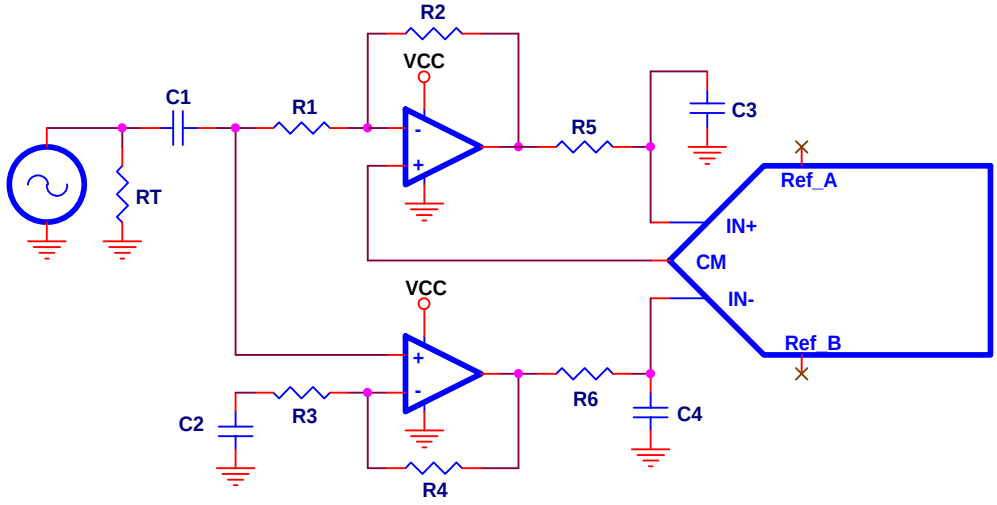


Figure 17. Differential Output, Single-Ended Input, AC-Coupled, Single Supply

Figure 17 shows an implementation that takes advantage of the characteristics of inverting and noninverting op amp stages. The common mode voltage from the ADC is coupled to the inverting op amp stage (on the top) as its virtual ground. This dc voltage is superimposed on the ac-coupled signal as its virtual ground. There is no dc return, so there is no dc gain. The virtual ground potential appears at the op amp output, the inverting input, and (because no dc current flows through blocking capacitor C1) the junction of R1 and C1. This potential is also connected to the noninverting input of the bottom op amp stage, and appears at its output and inverting input as well. Because C2 also blocks dc current, the dc voltage is prevented from being amplified by 2 in the bottom stage, which looks like a unity gain buffer to dc. R5, R6, C3, and C4 are ADC compensation components.

The chief disadvantage of this approach is that it is hard to come up with resistor values that match the inverting and noninverting stages.

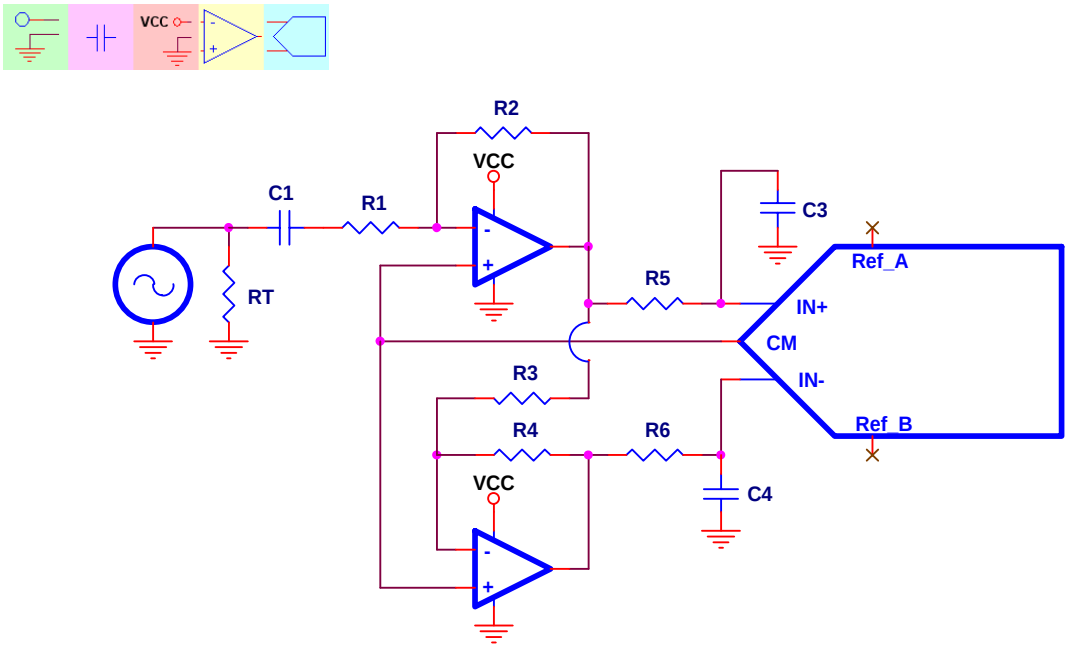


Figure 18. Alternative Differential Output, Single-Ended Input, AC-Coupled, Single Supply

Figure 18 modifies the interface of Figure 17 by converting both stages to inverting stages. Gain is accomplished in the first stage with R1 as the input resistor and R2 as the gain resistor. R3 and R4 are equal, creating a unity-inverting gain inverting stage. The common mode output of the ADC provides the virtual ground for both stages. The advantage of this approach is that C2, the second dc blocking capacitor, is eliminated. The disadvantage of course, is that the bottom signal is delayed by the additional delay of the bottom stage with respect to the top. Therefore, the input signal arrives at IN+ before IN-.

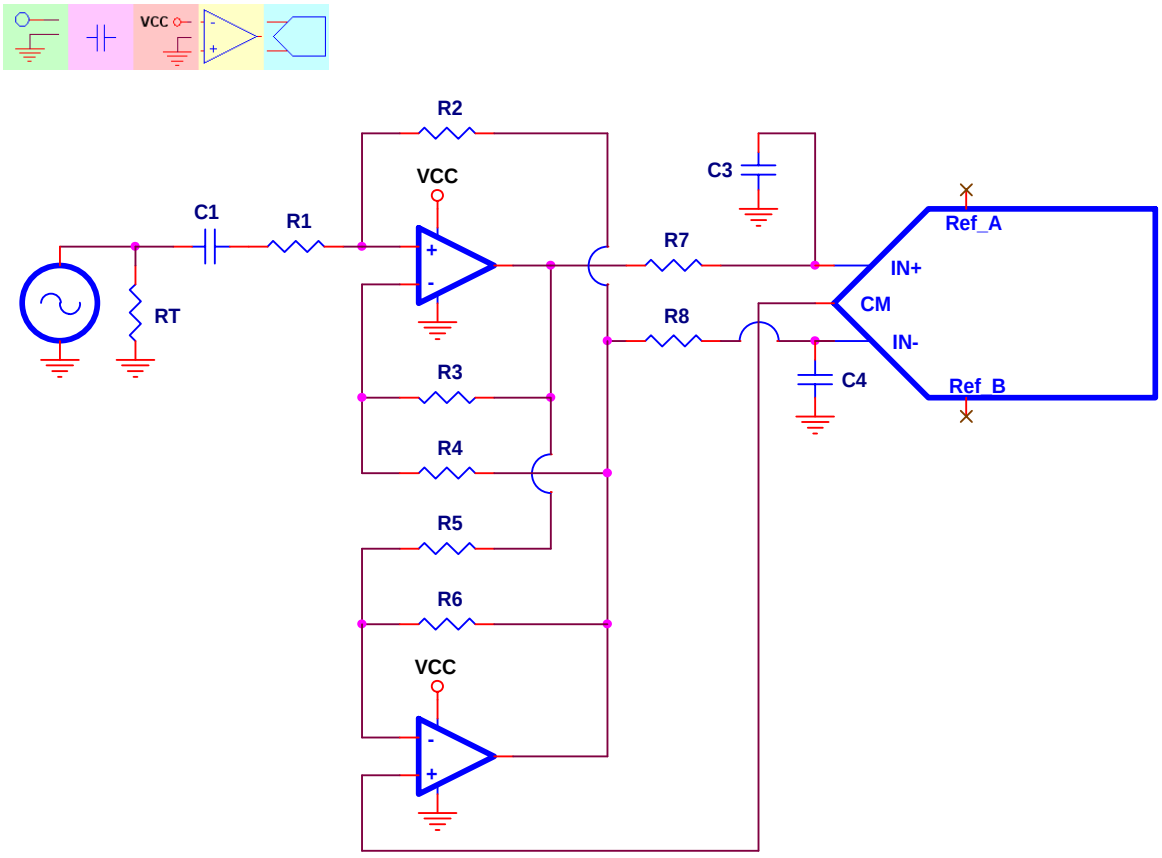


Figure 19. Alternative Differential Output, Single-Ended Input, AC-Coupled, Single Supply

Like Figure 18, the circuit of Figure 19 achieves fully differential output by cascading two inverting op amp stages. The top op amp with R3 and R4, forms the first stage. The second consists of the bottom op amp, R5 and R6. The overall circuit consists of an inverting gain stage consisting of input resistor R1, feedback resistor R2, and both op amps (with the bottom op amp performing the inversion for the top op amp). To use this circuit, R3 through R6 should all be the same value and closely matched. R2 and R1 are the values required to set the gain of the circuit. R7, R8, C3, and C4 are ADC compensation components.

The chief advantage of this stage is that the delays for each signal are matched—both signals have to go through two op amps before connection to the ADC.

4.6 Differential Output, Single-Ended Input, AC-Coupled, Dual Supply

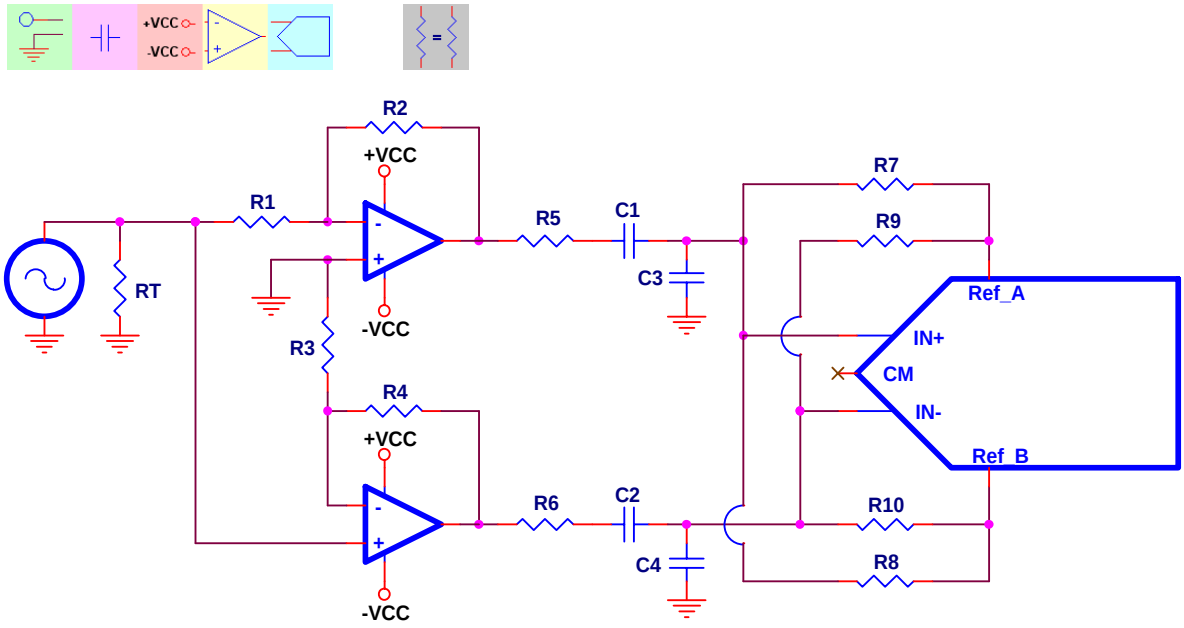


Figure 20. Differential Output, Single-Ended Input, AC-Coupled, Dual Supply

In Figure 20, an inverting and a noninverting op amp gain stage are again used to present two polarities of an input signal to a differential input ADC. The resistors R1 and R2 set the inverting gain of the top op amp. The bottom op amp is a noninverting gain stage. R4 and R3 set the stage gain, which must match the top gain stage. R5, R6, C3, and C4 are ADC compensation components. C1 and C2 are dc-blocking capacitors, which allow a split supply op amp to interface with single supply ADC, or allow a single supply op amp with a virtual ground at one voltage to interface to an ADC with a different common mode voltage. R7 through R10 must be matched, because they create a common mode voltage for the IN+ and IN- voltages off of the top and bottom reference voltages.

4.7 Differential Output, Single-Ended Input, DC-Coupled, Single-Supply

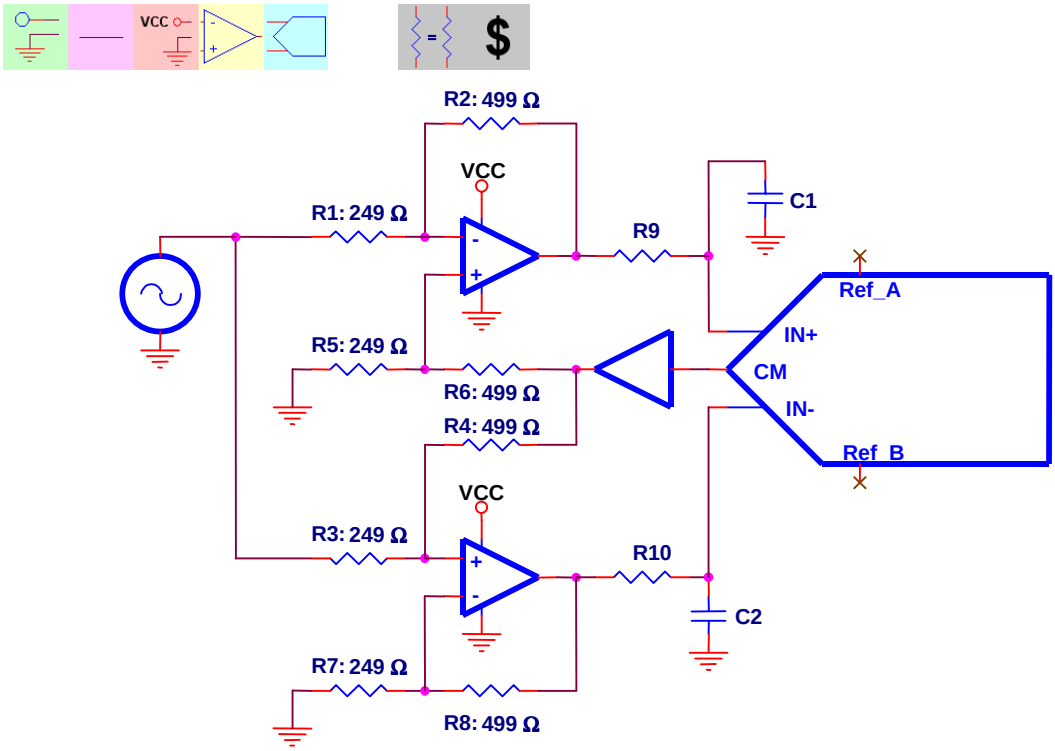


Figure 21. Differential Output, Single-Ended Input, DC-Coupled, Single Supply

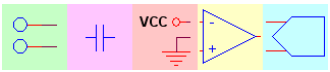
When the application calls for dc-coupling, the designer's problems are multiplied. In ac-coupled applications, the designer only has to consider the ac gain of the stages. In a dc-coupled application, the designer has to take the dc gain of the stages into account as well. The dc operating point and input common mode range of the op amps have to be considered, because dc gain can easily upset it. Power consumption for high-speed dc-coupled applications is probably higher than in ac-coupled applications, because common mode voltage levels to couple to ground through the low value resistors normally found in high-speed applications. A problem related to this is the current that the common mode source has to provide may exceed the capability of the ADC.

Figure 21 shows a specific application. The common mode source from the ADC is coupled to the op amps through a buffer stage—see Appendix A for ideas about specific implementations. AC gain of the top stage is determined by R2 and R1, and is fixed at 2. This gain is mirrored in the bottom stage, where gain is determined by R8 and R7. The noninverting input of both the top and bottom op amps is presented with common mode reference, voltage divided by 3 in resistors R6 and R5 for the top op amp, and resistors R4 and R3 for the bottom op amp. The dc gain of both op amps is the gain of a non-inverting op amp stage—in this case 3. The dc common mode of the ADC is thus preserved at the op amp output, because its common mode output is divided by 3 in the voltage divider, and then multiplied by 3 in the noninverting gain of the op amps. R9, R10, C1, and C2 are the compensation components required by the ADC.

4.8 Differential Output, Single-Ended Input, DC-Coupled, Dual-Supply

The change to a dual supply for the op amp is trivial; simply replace the ground connection in Figure 21 with a connection to the negative potential. There is little advantage to doing this since it increases the power consumption of the circuit.

4.9 Differential Output, Differential Input, AC-Coupled, Single Supply



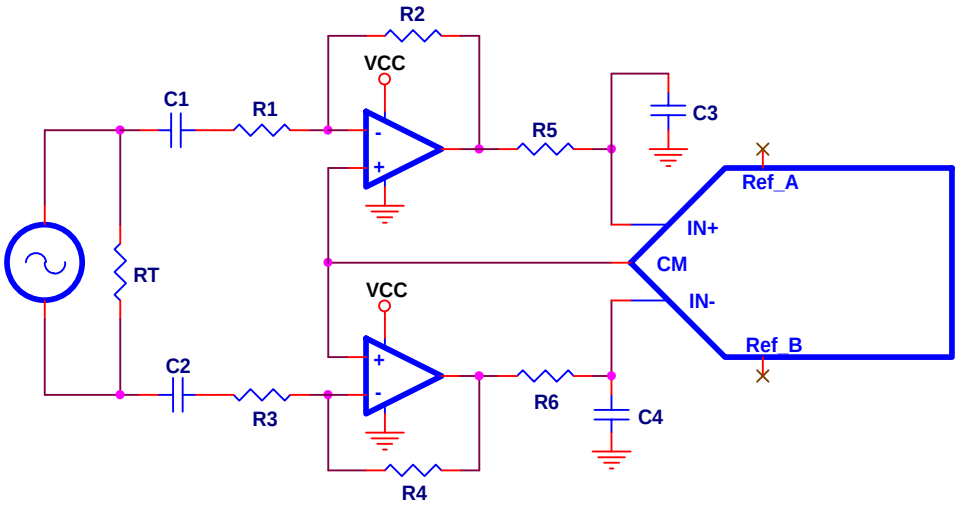


Figure 22. Differential Output, Differential Input, AC-Coupled, Single Supply

In Figure 22, resistors R1 through R4 determine inverting gain for the top and bottom op amps. The common mode voltage from the ADC is coupled to both op amp stages as their virtual ground. There is no dc return, so there is no dc gain. Capacitors C1 and C2 are coupling capacitors. R5, R6, C3, and C4 are ADC compensation components.

4.10 Differential Output, Differential Input, AC-Coupled, Dual Supply

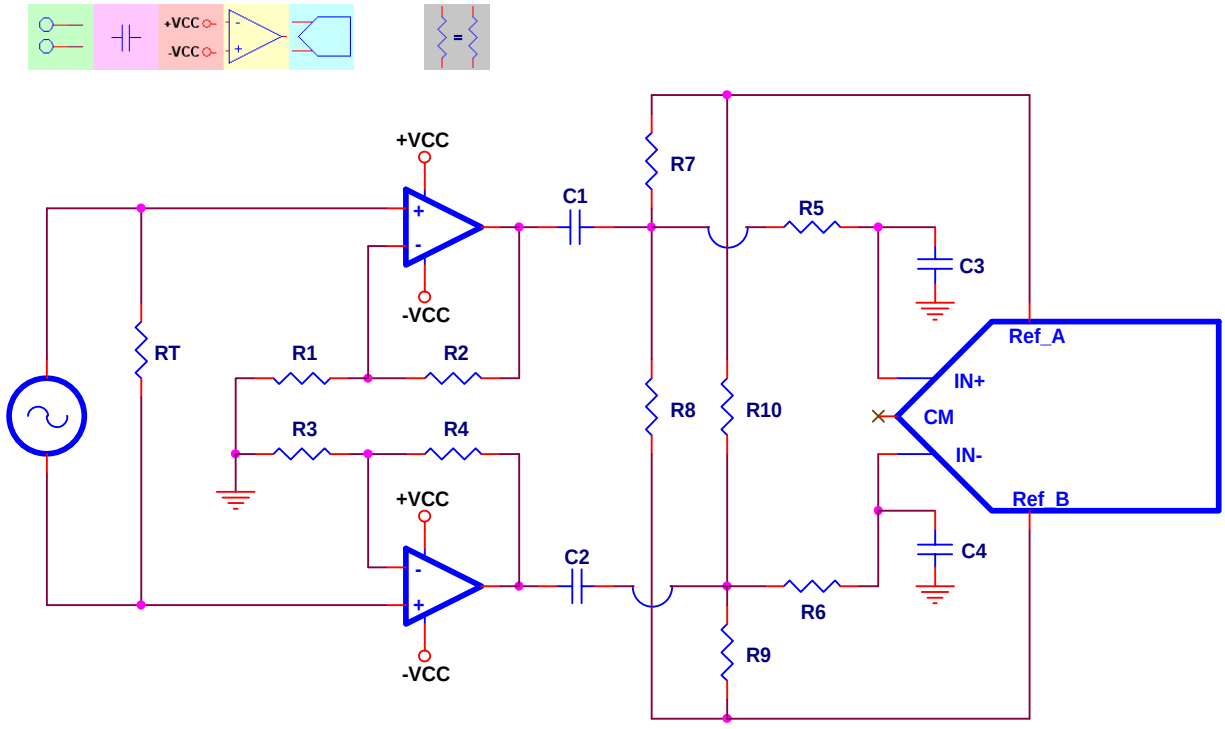


Figure 23. Differential Output, Differential Input, AC-Coupled, Dual Supply

In Figure 23, resistors R1 through R4 determine noninverting gain for the top and bottom op amps. The common mode voltage from the ADC is coupled to both inputs through resistors R7 through R10, which should be matched. Capacitors C1 and C2 are coupling capacitors. R5, R6, C3, and C4 are ADC compensation components.

4.11 Differential Output, Differential Input, DC-Coupled, Single Supply

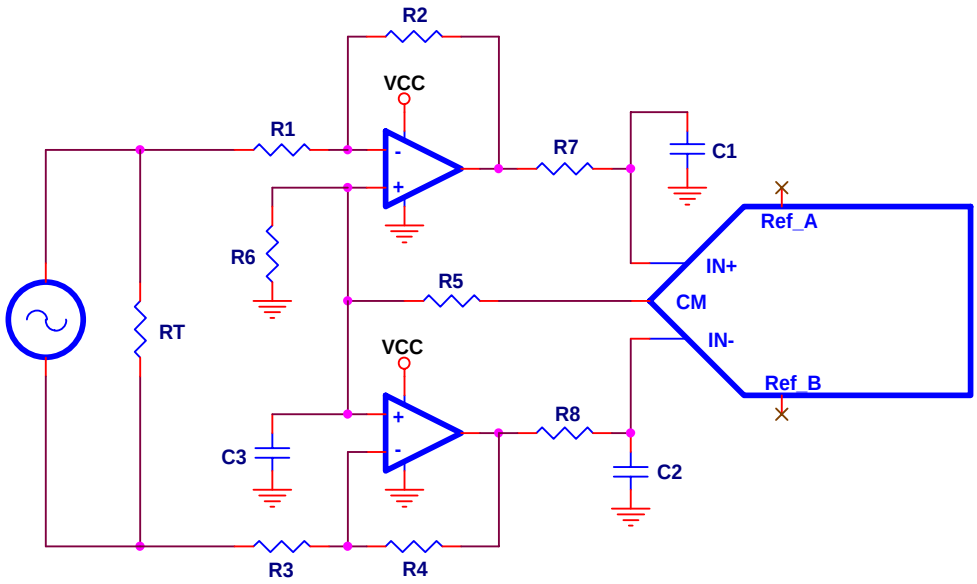


Figure 24. Differential Output, Differential Input, DC-Coupled, Single Supply

In Figure 24, R1 through R4 determine the inverting stage gain on the differential input. Resistors R5 and R6 are used to provide a common mode voltage to the stages. Resistors R1 through R4 also give noninverting gain to the dc voltage present on the noninverting input. Capacitor C3 decouples the common mode voltage provided to the two stages. The designer must be very careful not to load the common mode output of the ADC—a buffer stage may be necessary. Resistors R7 and R8, and capacitors C1 and C2 are ADC compensation components.

4.12 Differential Output, Differential Input, DC Coupled, Dual Supply

The change to a dual supply for the op amp is trivial; simply replace the ground connection in Figure 24 with a connection to the negative potential. There is little advantage to doing this since it increases the power consumption of the circuit.

5 Transformer Coupled Interface Techniques

Transformer coupling is a way of converting a single-ended input to a differential output without a buffer op amp. In practice, however, it is a problematic technique. The low impedance of the transformer usually dictates that a buffer op amp drive the transformer. Transformers block dc, and are expensive, large, and not standardized. What is worse, a decision by a manufacturer to change the design of a transformer, discontinue the part necessitating a change to a different part, etc. could force a designer to repeat FCC qualification tests costing tens of thousands of dollars. It is far better to avoid transformers whenever possible.

It makes no sense for a designer to purchase a transformer, and then use single-ended techniques to interface to a fully differential ADC, so those circuit configurations are not shown. Furthermore, the transformer blocks dc, so there is no point in showing dc coupled schematics:

This leaves four possible combinations.

5.1 Single-Ended Input, AC-Coupled, Single Supply

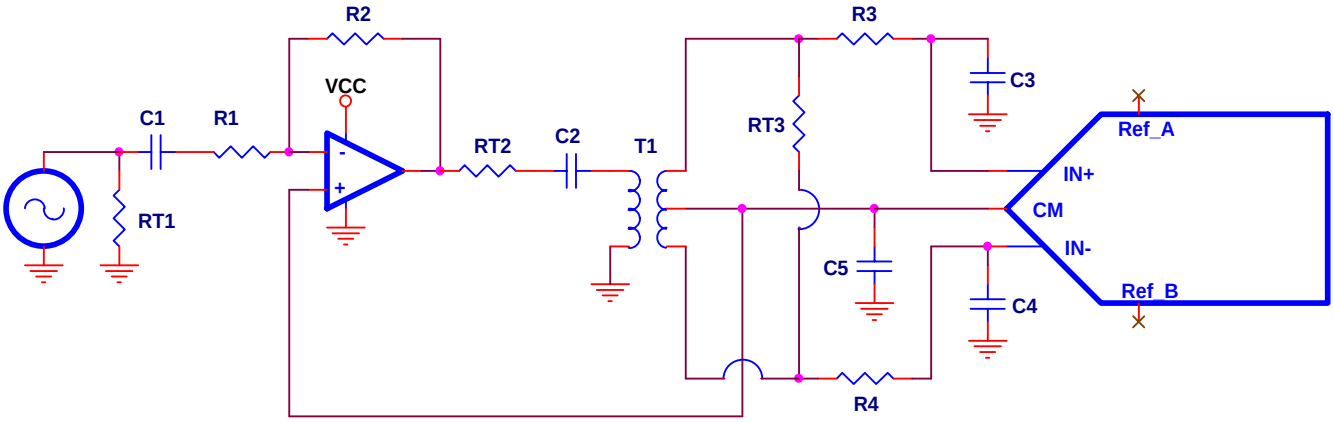


Figure 25. Single Ended Input, AC-Coupled, Single Supply

In Figure 25, resistors R1 and R2 set the inverting gain of the op amp to the desired level. Using the common mode output of the ADC to drive the noninverting input of the op amp creates the virtual ground for the op amp. The virtual ground level is isolated from the input by C1. Resistor RT2 isolates the output of the op amp from the capacitive / inductive load created by coupling capacitor C2 and the primary of T1. It also acts as a matching resistor for termination resistor RT3, which terminates the secondary of transformer. Resistors R3 and R4, and capacitors C3 and C4 are compensation components specified on the ADC data sheet. Capacitor C5 is a decoupling capacitor selected to reject noise in the system. The common mode point of the ADC is connected to the center tap of the secondary of T1, which sets the common mode point for the signals connected to IN+ and IN-.

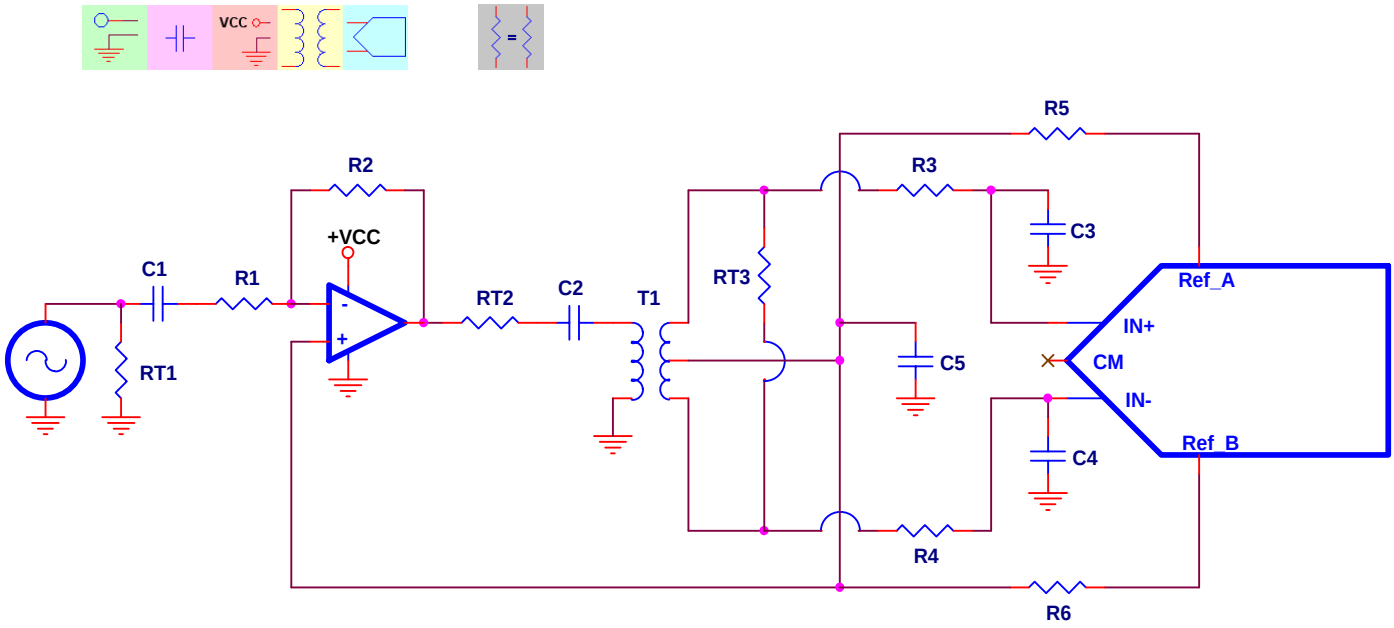


Figure 26. Transformer Coupled, Pre-Transformer, Derived Reference

Figure 26 shows how a reference for the transformer secondary can be derived from Ref_A and Ref_B. The gain for the inverting stage is determined by R2 and R1. RT2 isolates the op amp output from the reactive load formed by C2 and the primary of T1, and also operates to terminate the input. The common mode input for the secondary of T1, and the virtual ground for the buffer op amp stage, is generated by resistors R5 and R6, and bypassed by C5. R5 and R6 should be matched. R3, R4, C3, and C4 are ADC compensation components. RT1 terminates the input source, RT2 terminates the transformer primary, and RT3 terminates the transformer secondary (calculated by the turn ratio of the transformer).

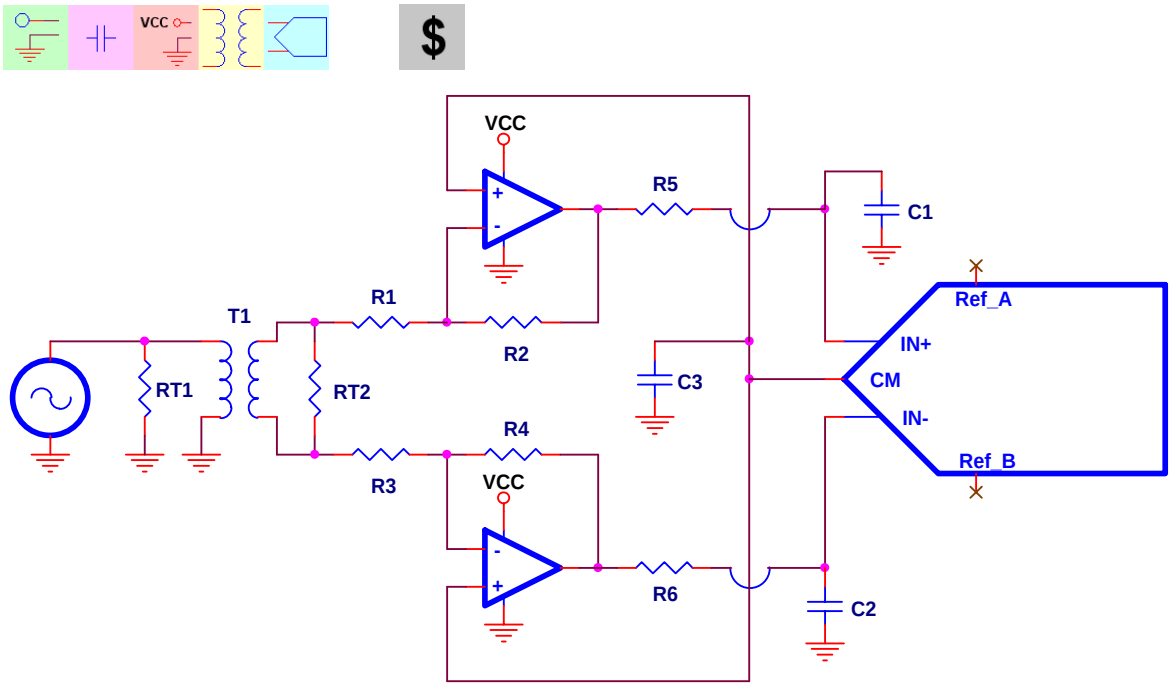


Figure 27. Transformer Coupled, Buffer on the Secondary Side

In Figure 27, a transformer T1 is again used as the coupling element. A center tap is not required. This time, however, the op amp interface is on the secondary side. Primary termination resistor RT1 is selected to match the source impedance. Secondary termination resistor RT2 is selected to match the turn ratio of the transformer and termination resistor RT1. Resistors R1 through R4 set the inverting gain of the two op amps—R1 is equal to R3, and R4 is equal to R2. Common mode point of the op amps is set by the common mode output of the ADC, decoupled by C3. R5, R6, C1, and C2 are compensation components specified on the ADC data sheet.

5.2 Single-Ended Input, AC-Coupled, Dual Supply

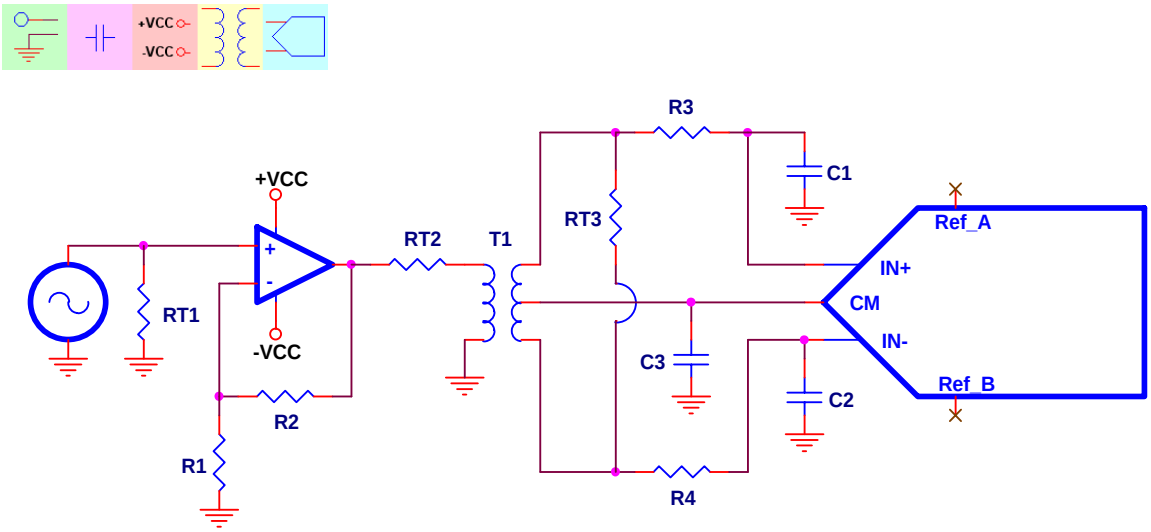


Figure 28. Single Ended Input, AC-Coupled, Dual Supply

In Figure 28, resistors R1 and R2 set the non-inverting gain of the op amp to the desired level. Resistor RT2 isolates the output of the op amp from the inductive load created by the primary of T1. It also acts as a matching resistor for termination resistor RT3, which terminates the secondary of transformer. Resistors R3 and R4, and capacitors C1 and C2 are ADC compensation components. Capacitor C3 decouples the ADC common mode output. The ADC CM output is connected to the center tap of the secondary of T1, which sets the common mode point for the signals connected to IN+ and IN-.

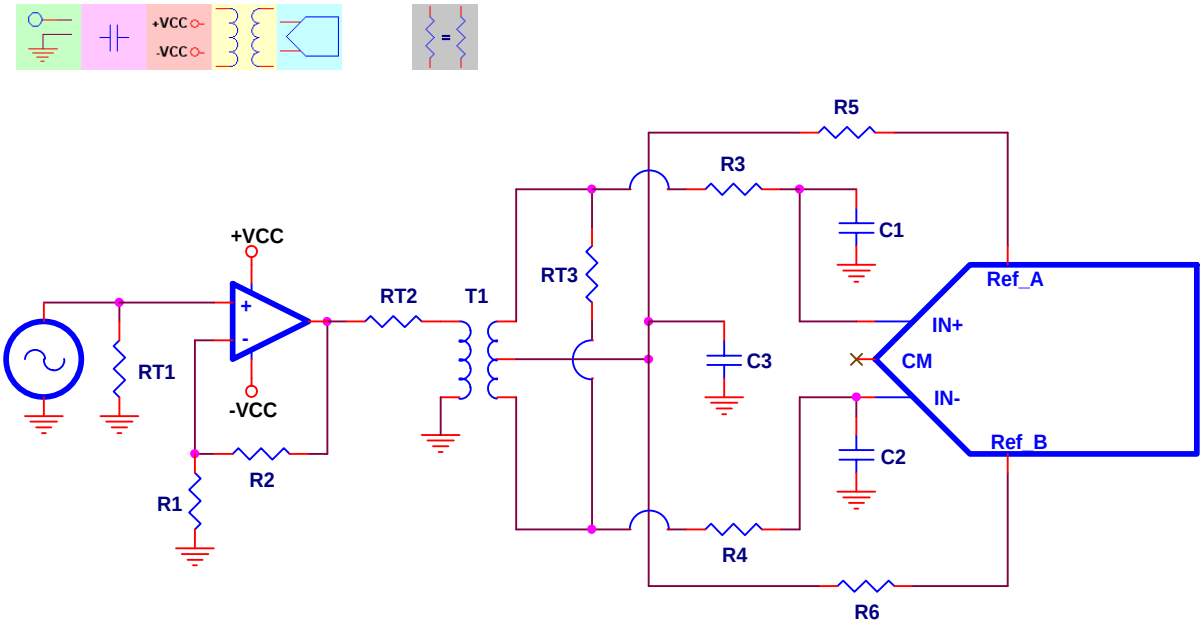


Figure 29. Single-Ended Input, AC-Coupled, Dual Supply

Figure 29 modifies the schematic of Figure 27 by using a derived common mode reference. Resistors R1 and R2 set the noninverting gain of the op amp to the desired level. Resistor RT2 isolates the output of the op amp from the inductive load created by the primary of T1. It also acts as a matching resistor for termination resistor RT3, which terminates the secondary of transformer. Resistors R3 and R4, and capacitors C1 and C2, are ADC compensation components. Resistors R5 and R6, which should be matched, are used to derive a common mode reference. The reference derived from resistors R5 and R6 is connected to the center tap of the secondary of T1, which sets the common mode point for the signals connected to IN+ and IN-. Capacitor C3 bypasses the derived common mode reference.

5.3 Differential Input, AC Coupled, Single Supply

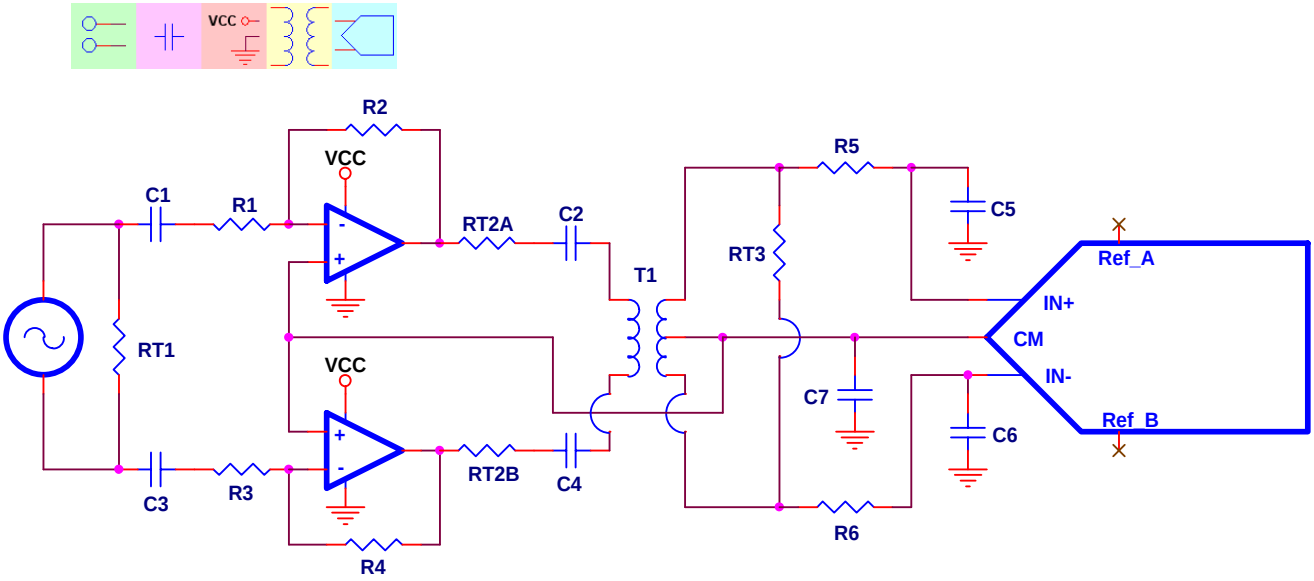


Figure 30. Differential Input, AC-Coupled, Single Supply

In Figure 30, resistors R1 through R4 set the inverting gain of the op amps to the desired level. Using the common mode output of the ADC to drive the noninverting inputs of the op amps creates the virtual ground. The virtual ground level is isolated from the input by C1 and C3. Resistor RT2A and RT2B isolate the output of the op amp from the capacitive / inductive load created by coupling capacitors C2 and C4, and the primary of T1. It also acts as a matching resistor for termination resistor RT3, which terminates the secondary of transformer. Resistors R5 and R6, and capacitors C5 and C6 are compensation components specified on the ADC data sheet. Capacitor C7 is a decoupling capacitor selected to reject noise in the system. The common mode point of the ADC is connected to the center tap of the secondary of T1, which sets the common mode point for the signals connected to IN+ and IN-.

The primary use of this circuit is for gains of less than 1, which are adjusted by the turn ratio of transformer T1 – not by attempting a gain of less than 1 in the buffer op amp stages.

5.4 Differential Input, AC-Coupled, Dual Supply

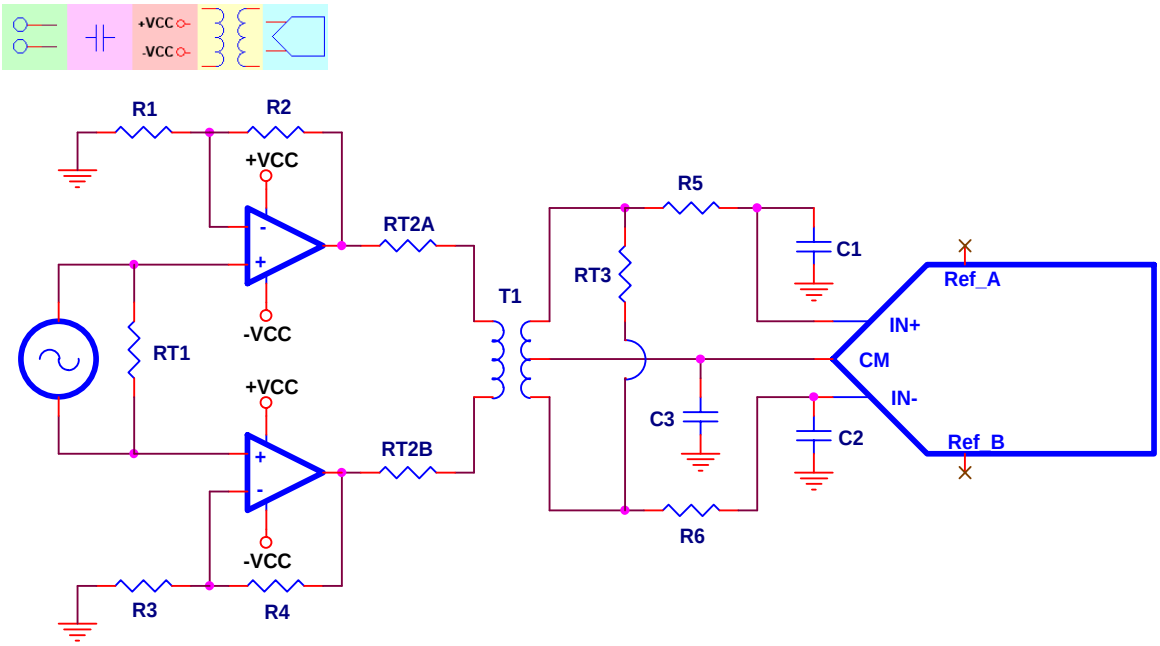


Figure 31. Differential Input, AC-Coupled, Dual Supply

In Figure 31, resistors R1 through R4 set the noninverting gain of the op amps to the desired level. Resistor RT2A and RT2B isolate the output of the op amp from the inductive load created by the primary of T1. It also acts as a matching resistor for termination resistor RT3, which terminates the secondary of transformer. Resistors R5 and R6, and capacitors C1 and C2, are ADC compensation components. Capacitor C3 decouples the ADC common mode output. The common mode output of the ADC is connected to the center tap of the secondary of T1, which sets the common mode point for the signals connected to IN+ and IN-.

The primary use of this circuit is for gains of less than 1, which are adjusted by the turn ratio of transformer T1.

References

1. *How (Not) to Decouple High Speed Op Amp Circuits*, Texas Instruments SLOA069
2. *Op Amp Noise Theory and Applications*, Texas Instruments SLOA082
3. *Differential Op Amp Single-Supply Design Techniques*, Texas Instruments SLOA072
4. *Gain and Offset in Thirty Seconds,* Texas Instruments SLOA097

Appendix A: How to Choose a Reference

What is a reference? In order to understand how to design a proper reference circuit, it is useful to review what a reference is, what the characteristics of a proper reference should be, and the ways actual references can differ from the ideal. A reference is an accurate, stable dc voltage to which other points in a data acquisition (such as inputs) can be referred—hence the name *reference*. Some of the characteristics of references include:

- **Accuracy:** A reference should be accurate. Accuracy is usually expressed in percentage – the lower the value the better. An ideal reference would be completely accurate. Reference inaccuracies affect the upper and lower endpoints of ADC inputs—whether a single or dual reference is used.

- **Drift:** A reference should not change—the dc level should not change over time or temperature. Drift is usually expressed in terms of parts per million. An ideal reference never changes over time or temperature. Drift can change the calibration of a data acquisition system, requiring frequency self-calibration and error correction cycles.

- **Noise:** A reference should not introduce any noise into the data acquisition system. Ripple and noise are usually specified in terms of mV or μV. An ideal reference has no noise.

The most common application is to use the ADC internally generated reference(s) as the system reference. The ADC references then determines the common mode point of the circuit, and the low and high limits of the input.

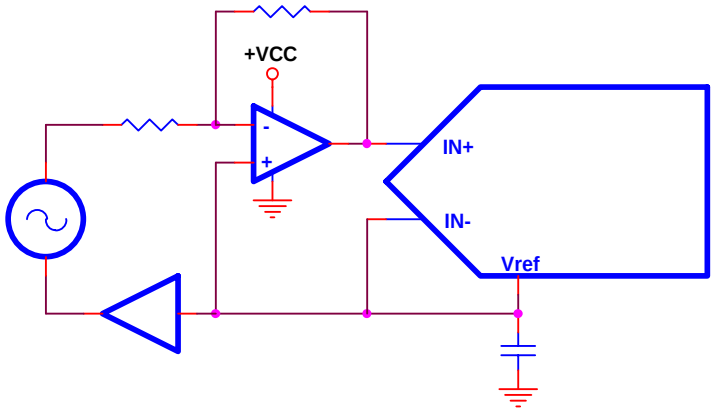


Figure 32. ADC Reference

The example above shows how the reference is also used to generate the negative input of the ADC. This is very common in single-ended systems, and causes no decrease in accuracy. The reference voltage level of the ADC must also be the return level of the input source; otherwise the op amp is driven into saturation. Most ADC reference output voltages cannot drive any appreciable load, so they must be buffered with a stage that increases their ability to drive current.

Many ADC references can be inputs as well as outputs, because they are simple resistive voltage dividers. This means that they can be driven by external sources. In some applications, this may make more sense than using the internally generated reference levels. One of the simplest examples of this is a strain gauge pressure transducer (with one variable leg), which produces a very high accuracy dc reference from the other side of the bridge. Using this level as the system reference forces the common mode point of the op amp and the reference level of the ADC to the same level, producing highly accurate results.

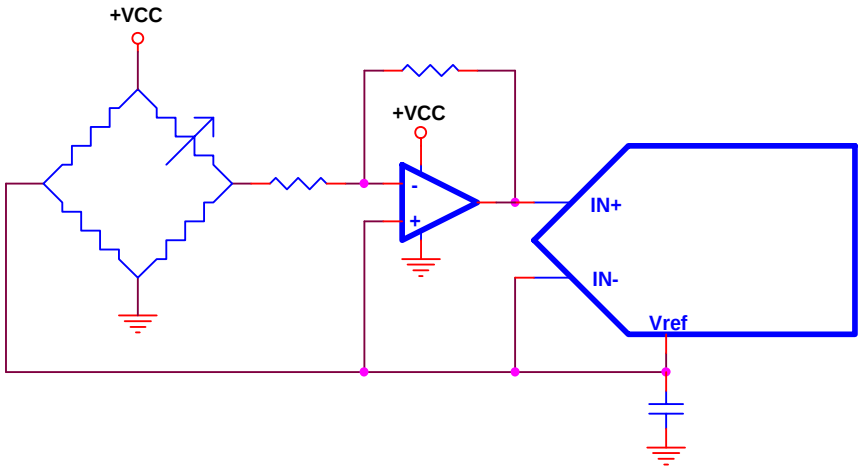


Figure 33. Reference From Sensor

The example above shows how the reference is also used to generate the negative input of the ADC. This is very common in single-ended systems, and causes no decrease in accuracy.

The designer needs to answer the question: *What is the most accurate voltage level in the system*. Many times, the answer is the ADC reference level. Some times it is not the ADC reference level. The ADC reference level may have a considerable amount of noise on it from internal or external switching transients. If there is no suitable reference in the system, designers can always design one of their own:

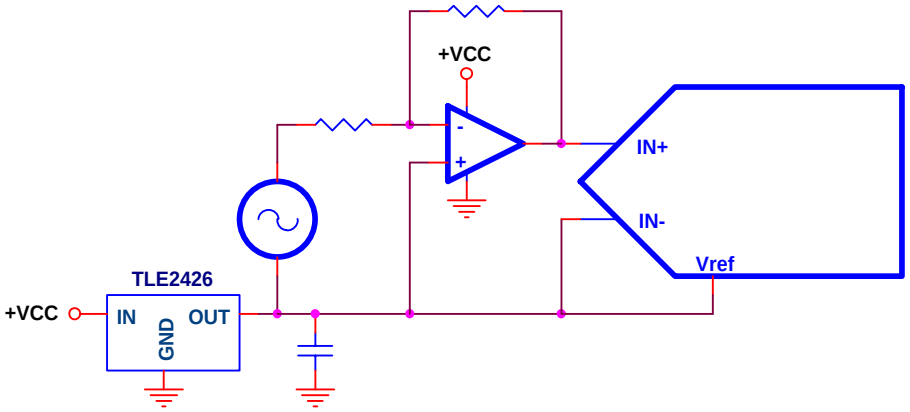


Figure 34. External Reference

The TLE2426 has excellent characteristics as a voltage reference. Texas Instruments manufactures a full line of voltage references that can also be used with excellent results. An example of a dual reference design is shown in Figure 35:

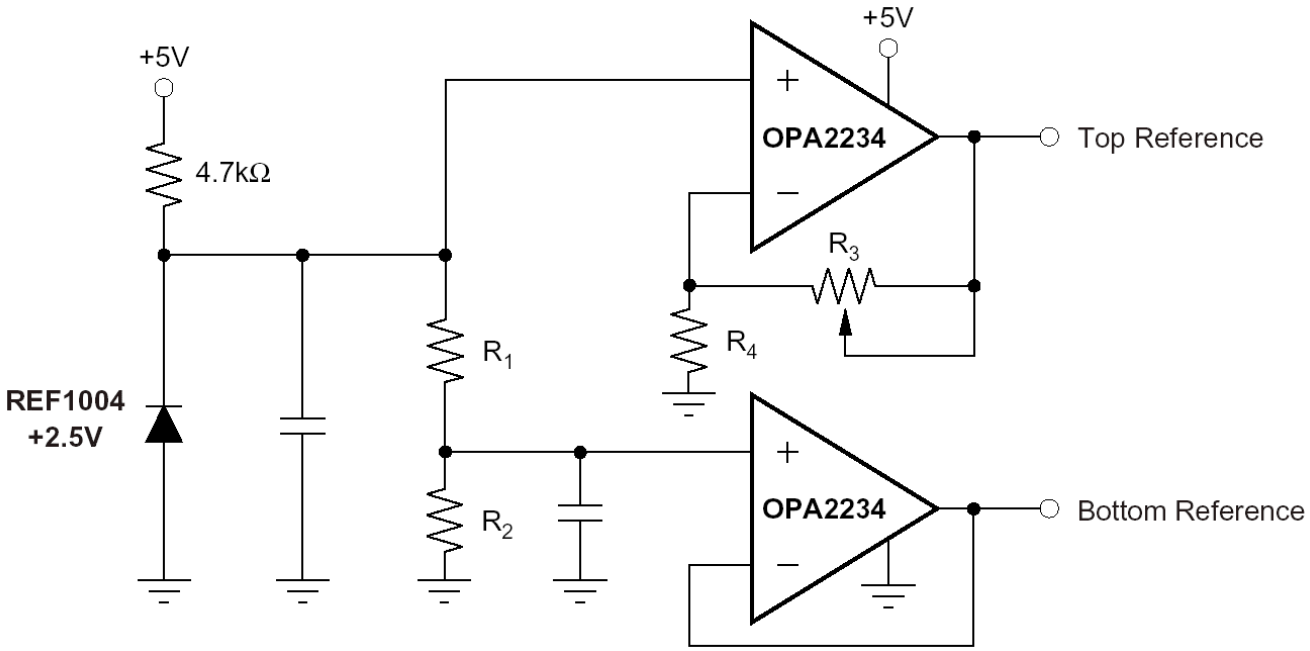


Figure 35. Dual Reference

The accuracy of the references created in Figure 35, of course, is closely related to the accuracy of the resistors. Since 1% resistors are commonly available, 1% accuracy is about all this circuit is capable of. That is not good enough for even an 8-bit system – but auto-calibration cycles are built into most modern data acquisition systems. Auto calibration takes calibration errors into account, and allows high degrees of accuracy, even in systems with low-accuracy resistors.

There is another aspect of accuracy that is more insidious, and cannot be cancelled by auto-calibration. That is the aspect of noise. The nature of noise is complex and beyond the scope of this document, and the reader is referred to Reference 2. The bottom line, however, is that noise gets worse as the frequency decreases—particularly when a band gap voltage reference or an op amp is used to drive the reference. It is far better to rely on resistive voltage dividers, bypassed by capacitors. This is not a perfect solution, however. Small value resistors can drive more current and have less noise—but also draw more current from the power supply. Larger value resistors cannot drive much current, have more thermal noise, and are susceptible to voltage divider effects with resistive elements in the ADC and other system components. Like many other aspects of design, the design of a reference circuit is an exercise in trade-offs.

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