

ERRATA

TO THE SN65LV1023A 10-MHz to 66-MHz, 10:1 LVDS Serializer/Deserializer DATA SHEET

(TEXAS INSTRUMENTS LITERATURE NO. SLLZ028, September 2003)

This document is an errata to the SN65LV1023A data sheet (Literature No. SLLS570).

Purpose

This document describes the SYNC pattern behavior of the SN65LV1023A. A logic error was found and the detail is discussed here.

Sync Pattern Generation

The sync pattern generation is designed to work as the following:

After SYNC1 or SYNC2 is held high for at least 6T($T = 1$ refclk cycle), the SYNC pattern is generated on the serial line for 1026T. During this 1026-cycle SYNC pattern transmission, it is not required that SYNC1 or SYNC2 be held high.

Now there are two different cases in general where user might use this SYNC pattern generation:

Case#1) SYNC1 or SYNC2 is held high once at least 6T but no more than 1026T:

In this case, the sync pattern generation should generate 1026T of SYNC pattern only once and the data that follow the SYNC pattern on the serial line should reflect the parallel inputs. In this scenario the sync pattern generation is working as it is designed.

Case#2) SYNC1 or SYNC2 is held high continuously more than at least 1038T (6T to invoke the first series of SYNC pattern, and 1026T which is the duration of the first series of SYNC pattern, and 6T to invoke the second series of SYNC pattern):

If the sync pattern generator were to operate as it is intended, a user should be able to observe the continuous SYNC pattern on the serial line. For example, if the SYNC1 or SYNC2 is held high for 1039T, a user will see the SYNC pattern being generated continuously for 2052T ($=1026T+1026T$). However, as shown in Figure 1 the device behaves in a way that if the SYNC1 or SYNC2 is held high more than 1038T, it sends out 1028T of SYNC pattern plus 4T of data (which reflect the data that is present on the parallel input at that time) and another 1026T of SYNC pattern. Figure 1 basically shows what would happen to the data on the serial line if the SYNC1 or SYNC2 is held for an extended period of time.

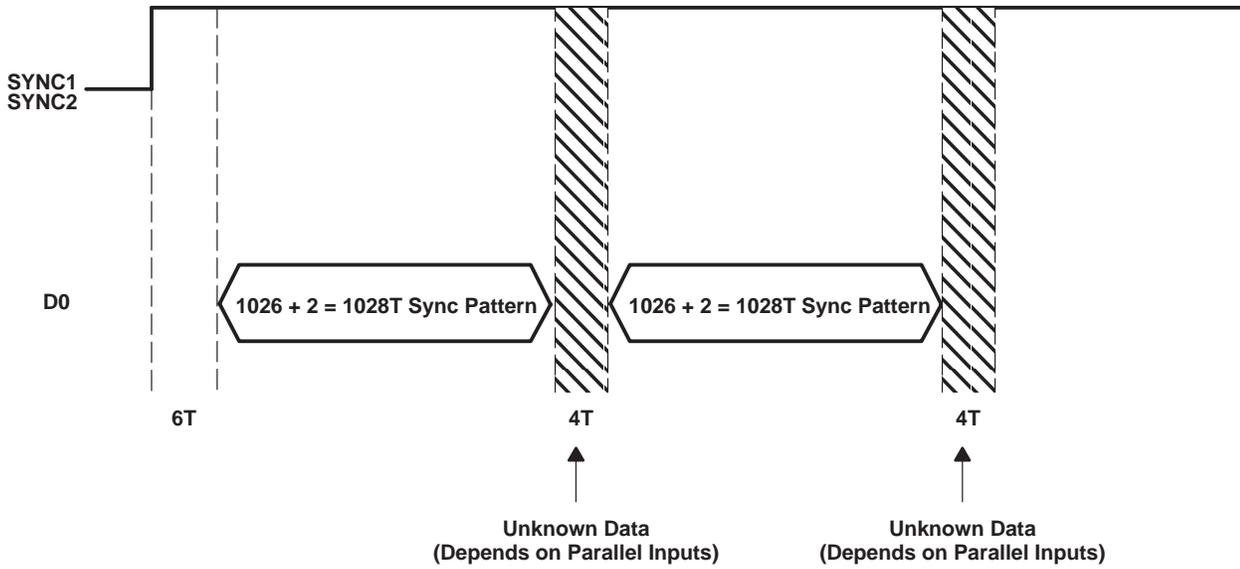


Figure 1. Sync Pattern Generation

System Impact

No system impact was reported by customers due to this behavior. However, if the receiver is designed to require more than 1026T of SYNC pattern to lock, then user needs to understand the device behavior described previously.

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