

# ***TAS5508-5122C6EVM User's Guide***

***PurePath Digital™ 5.1 Channel Evaluation Module for the  
TAS5508B Digital Audio PWM processor and  
TAS5122DCA Digital Amplifier Power Output Stage in  
Both Bridge-Tied-Load and Single-Ended Configuration***

*User's Guide*

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## ***User's Guide***

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October 2004–Revised April 2006



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## ***Read Me First***

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### **About This Manual**

This manual describes the operation of the TAS5508-5122C6EVM evaluation module from Texas Instruments.

### **How to Use this Manual**

This document contains the following chapters:

Chapter 1 - Overview

Chapter 2 - System Interfaces

Chapter 3 - Protection

### **Information about Cautions and Warnings**

This manual may contain cautions and warnings.

#### **CAUTION**

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

#### **WARNING**

**This is an example of a warning statement.**

**A warning statement describes a situation that could potentially cause harm to you.**

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

## Related Documentation from Texas Instruments

The following table contains a list of data manuals that have detailed descriptions of the integrated circuits used in the design of the TAS5508-5122C6EVM. The data manuals can be obtained at the URL <http://www.ti.com>.

**Table 1. Related Documentation From Texas Instruments**

PART NUMBER	LITERATURE NUMBER
TAS5508B	SLES162
TAS5122	SLES088
SN74LVC1G08	SCES217
SN74LVC1G126	SCES224
LMV331I	SLCS136
TPS76433	SLVS180

## Additional Documentation

1. TAS5508-5122C6EVM Applications Report (SLEA042A)
2. PC Configuration Tool for TAS5508B (TAS5508 GUI ver. 2.1 or later)
3. General Application Notes

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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# Overview

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## 1.1 Overview

The TAS5508-5122C6EVM PurePath Digital™ customer evaluation module demonstrates two integrated circuits: the TAS5508A and the TAS5122DCA from Texas Instruments (TI).

The TAS5508BPAG is a high performance 32 bit (24 bit input) multichannel PurePath Digital™ Pulse Width Modulator (PWM) based on Equibit™ technology with new fully symmetrical AD modulation scheme. The device also has Digital Audio Processing (DAP) that provides 48-bit signal processing, advanced performance, and a high level of system integration. The device has interfaces for headphone output and Power Supply Volume Control (PSVC).

The TAS5122DCA is a high performance digital amplifier power stage designed to drive two 8-Ω loudspeakers up to 40 W (10% THD+N) in BTL configuration or four 4-Ω loudspeakers up to 20 W (10% THD+N) in single-ended configuration. It contains integrated gate-drivers, eight matched and electrically isolated enhancement-mode N-channel power DMOS transistors, and protection/fault-reporting circuitry.

This EVM is configured with five SE channels for the satellites and one BTL channel for the subwoofer.

The TAS5508-5122C6EVM, together with a TI input board, is a complete 6-channel digital audio amplifier system which includes digital input (S/PDIF), analog inputs, interface to PC, and DAP features like digital volume control, input and output mixers, automute, equalization, tone controls, loudness, dynamic range compression, and PSVC output. There are configuration options for stereo line level output, stereo headphone output, and power stage failure protection.

The system was designed for home theater applications such as DVD minicomponent systems, home theater in a box (HTIB), DVD receivers, or Plasma Display Panels (PDP).

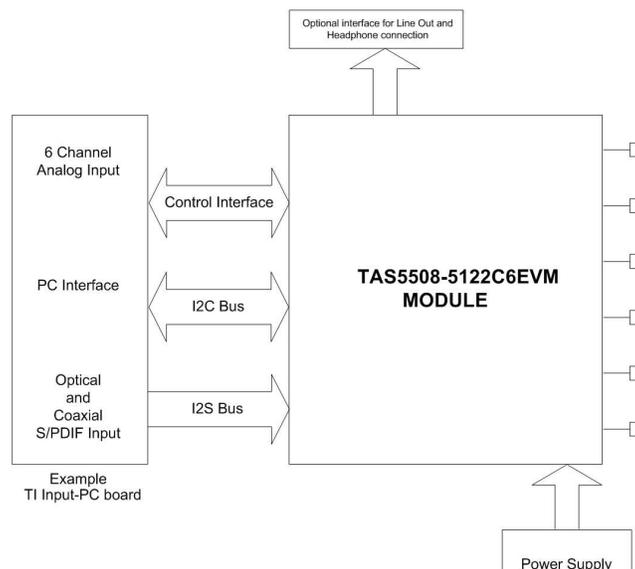


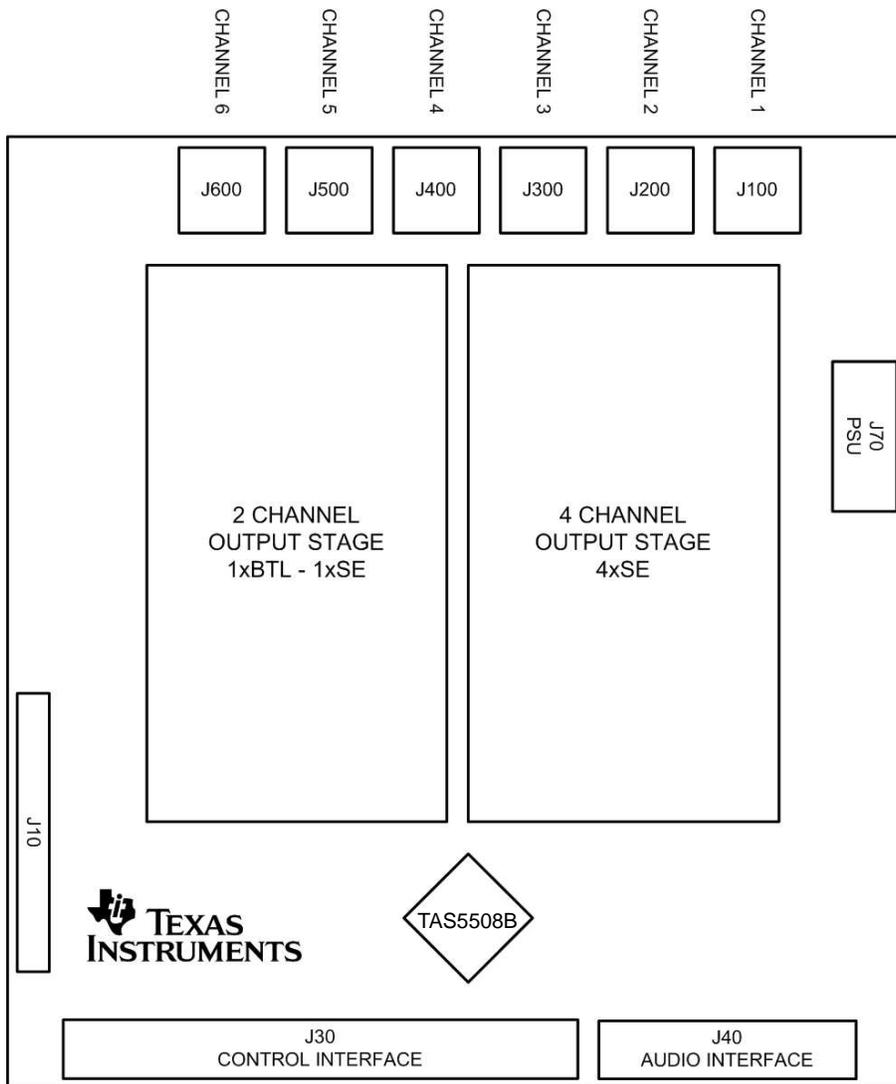
Figure 1-1. Complete PurePath Digital™ System

## 1.2 TAS5508-5122C6EVM Features

- 6-channel PurePath Digital™ evaluation module design
- Self-contained protection system (short circuit and thermal)
- Standard I2S and I2C / control connector for TI input board
- Double-sided plated-through PCB layout

### 1.3 PCB Key Map

Physical structure for the TAS5508-5122C6EVM is illustrated in [Figure 1-2](#).



**Figure 1-2. Physical Structure for the TAS5508-5122C6EVM (Rough Outline)**



## System Interfaces

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This chapter describes the TAS5508-5122C6EVM board in regards to power supply (PSU) and system interfaces.

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## 2.1 PSU Interface

The TAS5508-5122C6EVM module must be powered from one or two external regulated power supplies. High audio performance requires a stabilized output stage power supply with low ripple voltage and low output impedance.

**Note:** The length of power supply cable must be minimized. Increasing length of PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

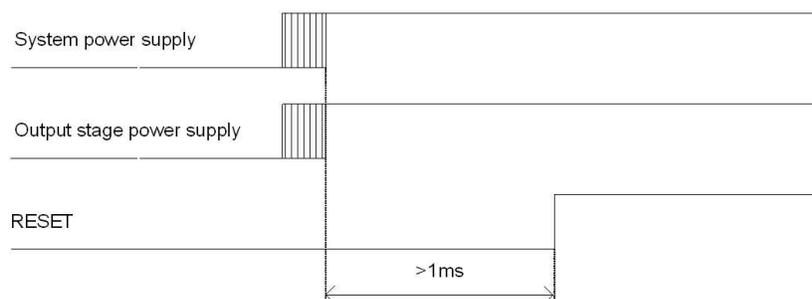
Maximum output stage supply voltage depends on the speaker load resistance. Check the recommended maximum supply voltage in the TAS5122 data sheet ([SLES088](#)).

**Table 2-1. Recommended Power Supplies**

DESCRIPTION	VOLTAGE LIMITATIONS(4-8 Ω LOAD)	CURRENT RECOMMENDATIONS
System power supply	15 V – 25 V	0.25 A
Output power stage supply	0 – 25 V	2.7 A <sup>(1)</sup>

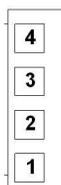
<sup>(1)</sup> The rated current correspond to two channels (Ch 1-5) full scale (15W/4ohm each) + one channel (CH 6) full scale (30W/8ohm), which most likely is adequate for a standard 6 channel amplifier design.

The recommended TAS5122 power-up sequence is shown in [Figure 2-1](#). For proper TAS5122 operation, the **RESET** signal should be kept low during power-up. **RESET** is pulled low during power-up for 200 ms by the onboard reset generator (U80).



**Figure 2-1. Recommended Power Up Sequence**

## 2.2 PSU Connector (J70)



**Figure 2-2. J70 Pin Numbers (PCB connector top view)**

**Table 2-2. J70 Pin Description**

PIN NUMBER	NET-NAME AT SCHEMATICS	DESCRIPTION
1	VDD	Output stage power supply
2	-	System power supply

**Table 2-2. J70 Pin Description (continued)**

PIN NUMBER	NET-NAME AT SCHEMATICS	DESCRIPTION
3	GND	Ground
4	GND	Ground

## 2.3 Loudspeaker Connectors (J100 ... J600)

### CAUTION

Both positive and negative speaker outputs are floating and may not be connected to ground (e.g. through an oscilloscope).



**Figure 2-3. J100 ... J600 Pin Numbers (PCB Connector Top View)**

**Table 2-3. J100 - J600 Pin Description**

PIN NUMBER	NET-NAME AT SCHEMATICS	DESCRIPTION
1	OUT_A	Speaker negative output
2	OUT_B	Speaker positive output

## 2.4 Optional Header for Line Out and Headphone (J10)

This is an optional interface for line out and headphone connections.

**Table 2-4. J10 Pin Description**

PIN NUMBER	DESCRIPTION
1	Left line out channel PWM (M)
2	Left line out channel PWM (P)
3	/Valid for line out channels
4	Right line out channel PWM (M)
5	Right line out channel PWM (P)
6	Ground
7	Left headphone channel (M)
8	Left headphone channel (P)
9	Right headphone channel (M)
10	Right headphone channel (P)
11	Headphone select – Active when low and inactive when high
12	Ground

## 2.5 Digital Audio Interface (J40)

The digital audio interface contains digital audio signal data (I2S), clocks etc. See the TAS5508B data manual ([SLES162](#)) for signal timing and details not explained in this document.

**Table 2-5. J40 Pin Description**

PIN NUMBER	NET-NAME AT SCHEMATICS	DESCRIPTION
1	GND	Ground
2	MCLK	Master Clock input. Low jitter system clock for PWM generation and reclocking. Ground connection from source to TAS5508B must be a low impedance connection.
3	GND	Ground
4	SDIN1	I2S Data 1, Channel 1 and 2
5	SDIN2	I2S Data 2, Channel 3 and 4
6	SDIN3	I2S Data 3, Channel 5 and 6
7	SDIN4	I2S Data 4, Channel 7 and 8
8	-	Reserved
9	-	Reserved
10	GND	Ground
11	SCLK	I2S bit clock.
12	GND	Ground
13	LRCLK	I2S left-right clock
14	GND	Ground
15	-	Reserved
16	GND	Ground

## 2.6 Control Interface (J30)

This interface connects the TAS5508-5122C6EVM board to a Texas Instruments input board.

**Table 2-6. J40 Pin Description**

PIN NUMBER	NET-NAME AT SCHEMATICS	DESCRIPTION
1	GND	Ground
2	-	Reserved
3	GND	Ground
4	/RESET	System reset (bi-directional). Activate $\overline{\text{MUTE}}$ before $\overline{\text{RESET}}$ for quiet reset
5	/BKND_ERR	Backend error (or soft reset) provides reduced click and pop reset without resetting I2C volume register settings.
6	/MUTE	Ramp volume from any setting to noiseless soft mute. Mute can also be activated by I2C.
7	/PDN	Power down. TAS5508B will go to power down state when activated
8	-	Reserved
9	-	Reserved
10	SDA	I2C data clock
11	GND	Ground
12	SCL	I2C bit clock
13	-	Reserved
14	-	Reserved
15	-	Reserved
16	-	Reserved
17	GND	Ground
18	-	Reserved
19	-	Reserved

**Table 2-6. J40 Pin Description (continued)**

PIN NUMBER	NET-NAME AT SCHEMATICS	DESCRIPTION
20	/SD	Shutdown error reporting for all channels. Activated if TAS5122 has high current or high temperature for ~100 ms. See Chapter 3: Protection
21	-	Reserved
22	/OTW	Temperature warning. Activated with low signal if one or more TAS5122 has reached temperature warning level
23	-	Reserved
24	/HP_SEL	Headphone select. Headphone active when low and inactive when high. Default setting is high.
25	GND	Ground
26	GND	Ground
27	-	Reserved
28	-	Reserved
29	-	Reserved
30	-	Reserved
31	GND	Ground
32	GND	Ground
33	+5V	+5Vdc power supply (output)
34	+5V	+5Vdc power supply (output)



## Protection

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### 3.1 Short Circuit Protection and Fault Reporting Circuitry

The TAS5122 is a self-protecting device that provides device fault reporting (including high-temperature protection and short circuit protection). TAS5122 is configured in back-end auto-recovery mode and therefore resets automatically after all errors (M1 and M2 is set low). This means that the device will re-start itself after an error occasion and report shortly through the  $\overline{SD}$  error signal.

### 3.2 Device Fault Reporting

The  $\overline{OTW}$ ,  $\overline{SD\_AB}$ , and  $\overline{SD\_CD}$  outputs from TAS5122 indicate fault conditions. Please refer to the TAS5122 data manual for a description of these pins.

**Table 3-1. TAS5122 Error Signal Decoding**

$\overline{OTW}$	$\overline{SD\_XX}$	DESCRIPTION
0	0	High temperature error and/or high current error
0	1	High temperature warning
1	0	Under voltage lockout or high current error
1	1	Normal operation, no errors/warnings

The temperature warning ( $\overline{OTW}$ ) signals at the TAS5508-5122C6EVM board are wired-or to one temperature warning signal ( $\overline{TEMP\_WARNING}$ — pin 22 in control interface connector). Shutdown signals ( $\overline{SD\_AB}$  and  $\overline{SD\_CD}$ ) are wired-or to one shutdown signal ( $\overline{SHUTDOWN}$ — pin 20 in control interface connector). The shutdown signals, together with the temperature warning signal, give information on the chip state information as described in the [Table 3-1](#). Device fault reporting outputs are open-drain outputs.

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## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 15 V to 25 V and the output voltage range of 0 V to 25 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 75° C. The EVM is designed to operate properly with certain components above 75° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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