

## TVP5147 PCB Layout Guidelines

## **TVP5147 PCB Layout Guidelines**

- A High-K printed circuit board having a minimum of 4 layers is recommended for best thermal transfer and performance.
- The choice of single GND plane or split DGND/AGND plane will depend on board content and parts
  placement. If a single GND plane is used, keep digital components and return currents away from the
  analog section. If separate planes are used, keep analog power, decoupling, and traces over the
  AGND plane and digital traces over the DGND plane.
- Place the TVP5147 as close as possible to the video input jacks.
- Anti-alias filters terminated with 75 ohms are recommended for each video input for the best quality.
   Use 0.1µF AC-coupling capacitors prior to the TVP5147 video input pins.
- Try to maintain a video input trace impedance of 75 Ω.
- Ensure that power bus/plane routing is adequate to handle current requirements of the device. Linear regulators are preferred for the analog power supplies.
- Use adequate power supply filtering. If analog and digital supplies share a common regulator, filter each node separately.
- All device 0.1µF decoupling capacitors should be placed near the power and GND pins of the device.
- Keep reasonable clearances between the 14.31818-MHz crystal/associated circuitry and adjacent video and digital trace routing. Placing a cutout in the ground plane and ground fill layers around the 14.31818-MHz crystal and associated circuitry will help isolate the crystal input.
- All video input traces should have a minimum clearance of ten times the trace width between each other and other adjacent traces to minimize potential crosstalk between inputs.
- SDA/SCL traces should be routed together and have a minimum clearance of ten times the trace width from any adjacent traces.
- Maintain good trace length matching of digital video output traces and clock. Length matching tolerance will depend on setup/hold time margins of the receiving device.
- Use  $10-\Omega$  to  $22-\Omega$  series termination resistors on the clock and data lines for best signal quality and noise reduction. Place the resistors as close as possible to the TVP5147 output pins.
- All high-speed signals should be routed over solid power/ground planes and not routed over power/ground splits. Route signals over their associated power/ground plane where possible.
- Use ground fills on the top and bottom of the board for additional signal isolation.
- When a split GND plane design is used, connect the TVP5147 exposed thermal pad to the digital ground plane. Use an array of thermal vias to connect the thermal land to the internal GND plane.
- See Figure 1 for the recommended GND split in split GND designs.



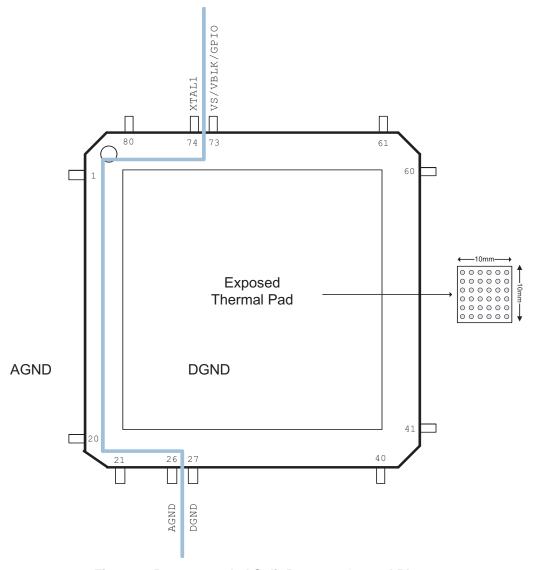


Figure 1. Recommended Split Between Ground Planes

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