

PGAxxxEVM-037 Pressure Sensor Signal Conditioner Evaluation Module

The PGAxxxEVM-037 provides a platform to test the PGA902, PGA904, and PGA302 in the TSSOP package. The EVM comes shipped as the PGA902EVM-037, the PGA904EVM-037, or the PGA302EVM-037, with the name indicating the associated device included with the EVM. The PGA902EVM-037 and PGA904EVM-037 includes a TSSOP socket, and can be used interchangeably for all three devices. This user's guide describes both the EVM hardware platform, and the graphical user interface (GUI) software used to configure and calibrate the PGAxxx pressure devices.

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1 Introduction

The PGAxxxEVM-037 is a fully-assembled evaluation module (EVM) designed to provide evaluation of the PGA902, PGA904, and PGA302 pressure sensor signal conditioner ICs. The user is able to configure the EVM by using any of the available digital interfaces (I2C, OWI, and SENT) depending on which device and EVM are being used. For ease of use, the most basic evaluation can be completed with only the PGAxxxEVM-037, a voltage supply capable of at least 7-V output, and a Microsoft[®] Windows[®] PC with the PGAxxxEVM GUI installed.

Temperature and pressure inputs can be simulated by the onboard *Resistive Bridge Emulator* (see Section 4.15.5), or the user can connect external temperature and pressure sensors to evaluate their performance in conjunction with the PGAxxx device.



Introduction



Figure 1. PGA302EVM-037 Top Board Sections



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Figure 2. PGA302EVM-037 EVM Bottom Board Sections

The PGAxxxxEVM-037 is divided into the following sections:

- 1. Power
 - a. External power connectors
 - b. Onboard regulators
- 2. OWI Communication
- 3. MSPR430F5510 Microcontroller
- 4. External resistive bridge interface
- 5. Resistive bridge emulator
- 6. Programming circuitry
 - **NOTE:** Pictured is a PGA302EVM-037 which does not include additional circuitry for firmware programming and SENT communication that is present on the PGA90xEVM-037. The PGA90xEVM-037 also includes a socket instead of a soldered down device.

PGAxxxEVM-037 Pressure Sensor Signal Conditioner Evaluation Module



2 Default Configuration

The EVM requires a 7-V to 28-V input applied to PWR_IN and GND_IN. The power supply should be current limited to 100 mA. The default jumper settings connect the resistive bridge emulator to the VBRG outputs and to the VINP inputs of the PGAxxx device and are described in full in Table 1.

Jumper	Setting	Function
J4	Pins 1-2 Closed	Connect VINTP to RT1 10-k Ω thermistor
J5	Pins 1-2 Closed	Connect top of resistive bridge emulator to VBRGP
J6	Pins 1-2 Closed	Connect resistive bridge emulator output to VINPP
J7	Pins 1-2 Closed	Connect resistive bridge emulator output to VINPN
J9	Pins 2-3 Closed	Power 3.3-V LDO from VCC
J11	Open	Disconnect SENT output

Table 2. Additional Jumper Settings Description		
Jumper	Setting	Function
J4	Pins 2-3 closed	Connect DAC_CAP to RT1 10-k thermistor
15	Pins 2-3 closed	Connect top of resistive bridge emulator to TEST1
J2 -	Open	Connect VBRGP to J3 pin 1
IC	Pins 2-3 closed	Connect resistive bridge emulator output to VINTP
J0	Open	Connect VINPP to J2 pin 1
17	Pins 2-3 Closed	Connect resistive bridge emulator output to VINTN
JI	Open	Connect VINPN to J2 pin 2
J9	Pins 1-2 Closed	Power 3.3-V LDO from USB VBUS
J11	Closed	Connect SENT output

Table 2. Additional Jumper Settings Description

3 EVM Setup and Operation

3.1 Quick Start Procedure

The PGAxxxEVM-037 is designed to be ready for immediate evaluation out of the box with the onboard resistive bridge emulator as a simulation of a pressure sensor input. The following procedure details the steps necessary to begin evaluation with the PGAxxxEVM-037 and the PGAxxx EVM GUI.

- 1. Collect the following supplies:
 - PGAxxxEVM-037
 - PC running Windows 7 or later
 - Micro-USB to USB cable
 - A single power supply unit, battery, or AC/DC adapter to provide a voltage output from 7 V to 28 V and a current output of up to 100 mA.
- 2. Follow the instructions in the *Installation* section (see Section 4.1) of the User's Guide to install and run the PGAxxx EVM GUI.
- 3. With the power supply off, connect the positive output of the supply to the PWR_IN connector on the EVM, and the power supply ground to the GND_IN connector. Only turn on the power supply output after connecting to the EVM.
- 4. Plug the micro-USB cable into the USB port on the EVM, and the USB side of the cable into the PC. The EVM setup should look similar to the one shown in Figure 3.





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Figure 3. EVM Quick Start Setup

- 5. Navigate to the GUI installation directory to run the PGAxxx EVM GUI.
- 6. Verify that communication has been established between the EVM and the GUI by checking the *EVM Status* section in the main panel, or in the status bar on the bottom left of the GUI as shown in Figure 4.

Ē	VM Status			
	USB Controller:	US	B2ANY I/F Found	
	USB Firmware:	2.7	7.0.52	_
	Connection Statu	IS:	Connected	
	PGA Device Statu	IS:	Revision: 0.0	

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Figure 4. EVM GUI Connection Status

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3.2 VDD Voltage Setup

The OWI circuitry can be sensitive to component variances and loading. To ensure proper voltage levels, a 10-k Ω potentiometer (R21) must be adjusted by the user. The potentiometer is located on the bottom of the board (pictured in Figure 5) and should be adjusted while the PGAxxxEVM-037 is powered up first by pulling the OWI_5P5 pin high with the *EVM Pin State* controls in the GUI (see Section 4.3.2), then by monitoring the voltage on the VDD test point or with the *Voltage Monitor* tab (see section 4.15.3) and turning the potentiometer until VDD is between 4.5 V and 5.5 V.



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EVM Setup and Operation

Figure 5. VDD Voltage Adjustment Potentiometer

3.3 Pressure Inputs

The PGAxxxEVM-037 includes a resistive bridge emulator designed to simulate a typical 5-k Ω pressure sensor topology. The variable leg consists of a digital potentiometer in parallel with a 2.61-k Ω resistor, and the parallel components are in series with a 2.55-k Ω resistor as shown in Figure 6.





Figure 6. Schematic of Resistive Bridge Emulator

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The default configuration of the EVM connects the PGAxxx to the resistive bridge emulator with VBRGP and VBRGN supplying voltage, while VINPP and VINPN are connected to measure the differential voltage across the legs of the bridge. To use an external bridge or pressure sensor, remove the jumpers J5, J6, and J7. Next, connect the positive bridge voltage to J3 pin 1 (VBRGP) and the negative terminal of the bridge to J3 pin 2 (VBRGN). The differential voltage outputs of the bridge can be connected to J2, with pin 1 being VINPP and pin 2 being VINPN, as shown in Figure 7.





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Figure 7. External Bridge Connections

3.4 Temperature Inputs

The external temperature sensor inputs can be connected to either the resistive bridge emulator, or to an external temperature sensor. By default, the EVM is configured with the external temperature sensor inputs, VINTP and VINTN, disconnected from the resistive bridge emulator, but accessible via J1 with pin 1 being VINTP and pin 2 being VINTN. To use the resistive bridge emulator to test the external temperature sensor measurement, place the jumpers as described in Table 3.

www.ti.com

Table 3. Jumper Settings to Connect Resistive Bridge to Temperature Inputs
--

Jumper	Setting	Function
J5	Open	Disconnect VBRGP from resistive bridge emulator
J6	Pins 2-3 closed	Connect resistive bridge emulator output to VINTP
J7	Pins 2-3 closed	Connect resistive bridge emulator output to VINTN

NOTE: This configuration connects an adjustable $10-k\Omega$ resistance between VINTP and VINTN as a test mode. It is not intended for use as a functioning external temperature sensor

Voltage Output 3.5

The PGAxxx devices can output measured pressure and temperature values in analog voltage form via the 14-bit output DAC. On the PGAxxxEVM-037 this VOUT voltage can be measured externally at the VOUT_SENT test point or through the GUI, which makes use of the internal ADC of the MSP430 to measure the voltage and display it on the Voltage Monitor tab of the GUI.

4 Software

4.1 Installation

Download and install the GUI from www.ti.com. Navigate to the default installation path of the executable file by clicking on the Windows Start button. Click on All Programs and then navigate to the Texas Instruments folder to find the PGAxxxGUI application shortcut.

4.2 **GUI Navigation**

The GUI is comprised of three main sections: the menu tree, the main control panel, and the tool panel as Figure 8 shows. All PGA device settings will be adjusted through the main control panel, which can be changed to display different groups of settings via the menu tree. The following sections describe the settings available in each item in the menu tree.





Figure 8. GUI Sections



Software

4.3 EVM Settings Page

EVM Status	EVM Pin State
USB Controller: USB2ANY I/F Found	VP_OTP_EN: LOW VOU_TX: HI-Z V
USB Firmware: 2.7.0.52	OWI_ACT: HI-Z 👻
Connection Status: Connected	OWI_5P5: HI-Z ▼
PGADevice Status: Revision: 0.0	
)WI Settings	
OWI Baud Rate: 4800 👻 bps	
Stop Bits : 1 👻 bit	
Send VDD Activation Pulse	
Send Register Activation Command	
2C Settings	
Lo counigo	
I2C Frequency: 800 - kHz	

Figure 9. EVM Settings Page

4.3.1 EVM Status

The GUI can automatically detect the presence of the PGAxxxEVM. In the event of a successful or failed connection between the PC, MSP430F5510, and PGAxxxEVM-037, the EVM status fields are updated according to Table 4.

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Table 4. EVM Status Possibilities

EVM Status	Success	Failure
USB Controller	USB2ANY I/F Found	Not Detected
USB Firmware	2.7.0.52	N/A
Connection Status	Connected	N/A
PGA Device Status	Revision 0.0	Not available

Table 5. EVM Status Field Descriptions

EVM Status	Definition
USB Controller	The MSP430F5510 is programmed with TI's USB2ANY host interface (I/F) controller firmware. The GUI calls API functions for the USB2ANY to execute. The USB2ANY I/F is the only compatible USB controller for the PGAxxxEVM GUI.
USB Firmware	The USB2ANY firmware can be updated for improvements or bug fixes. Version 2.7.0.52 is the only firmware version tested and known to be working for the PGAxxxEVM GUI.
Connection Status	Typically, only one USB2ANY is connected to a PC, though the USB2ANY APIs are able to distinguish multiple USB2ANY devices on the same USB bus. For a single USB2ANY I/F, the status will read Connected, but for multiple, the status will read Multiple Found. TI advises that a single USB2ANY I/F be connected to your PC during the evaluation of the PGAxxxEVM GUI.
PGA Device Status	 When an I2C read command is successfully executed on the PGA device, the status will be updated to <i>Ready</i>. If the status reads back <i>Not available</i>, use the following checklist to troubleshoot: Is the device seated properly in the socket (PGA902/904 only)? Is the PGAxxx-037 EVM powered with a voltage of 7–28 V? Is the power supply unit able to source at least 20 mA? If the device was powered after the GUI was first initialized, click the application reset button to reconnect

4.3.2 EVM Pin State

The *EVM Pin State* is automatically updated when the GUI is started and connected to a PGAxxx device. Any of the available pins can be changed by the user to either HIGH, LOW, or HIZ states.

4.3.3 OWI Settings

The following OWI settings are available:

- OWI Buad Rate: Sets the baud rate for the OWI communication. The available options are 2400 bps or 4800 bps
- Stop Bits: Sets the number of stop bits for OWI communication. The available options are 1 or 2 stop bits.
- Send VDD Activation Pulse: Briefly raises the VDD voltage to 7 V to initiate OWI communication. This is used to test if the OWI circuitry is functioning properly.
- Send Register Activation Command: For the PGA90x devices without programmed firmware, a register activation command is sent to activate the OWI transceiver circuitry within the device.

4.3.4 I2C Settings

The I2C frequency selection allows the user to select 100 kHz, 400 kHz, and 800 kHz for I2C communication.

4.4 General Settings Page

Figure 10 shows the *General Settings Page* window.



Software

Power Enable	Clock Frequency	
Analog Blocks	I MHz	
I2C Interface	② 2 MHz	
OWI Interface	MHz	
	8 MHz 8	
Communication Buffer (COM	/BUF)	
Digital Interface to PGA:	0x0000	
PGA to Digital Interface :	0x0000 Read	
RAM Memory Built-In Self Te Algorithm Select Checker and Invers MARCH13N with Ba MARCH13N with Ba	st (BIST) e Checker Board ackground 0x0 ackground 0xA ackground 0x3, 0xF, 0x69	BIST Start : BIST Complete : BIST Fail :

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Figure 10. General Settings Page

4.4.1 **Power Enable**

Power can be disabled to specific blocks within the PGAxxx device to decrease total power consumption. The analog blocks, I2C communication, OWI communication, and SENT OUTPUT (PGA904 only) can all be individually enabled or disabled to save power.

4.4.2 **Clock Frequency**

This section allows the user to control the clock frequency of the internal microcontroller.



4.4.3 RAM Memory Built-In Self Test

A RAM Memory Built-In self test is available to ensure the RAM of the PGAxxx device is functioning properly. The user can select one or more algorithms to test the memory. Once the test is begun by clicking the *START* button, the GUI will initiate each selected test in turn, and will report once all tests are complete and if the any of the tests were failed.

4.5 Analog Front End Page

The analog front end panel allows the user to configure the AFE portion of the PGAxxx device in an easyto-use block diagram format (shown in Figure 11) as an initial test and debug measure. These same settings are available in the *PGA302 EEPROM Settings* page (PGA302 EVM GUI only), however the settings made in the *Analog Front End* page will not carry over to the EEPROM settings page, and they must be repopulated in order to program the EEPROM for future use.





Figure 11. Analog Front End Page

4.5.1 Offset Correction

The offset correction setting allows the user to adjust the voltage offset of the pressure inputs to account for minor offset errors and to make full use of the input range of the integrated ADC of the PGAxxx. Offset correction values from –54.75 mV to +54.75 mV are available, or the offset correction can be turned off entirely.

4.5.2 Input Signal MUX Select and Additional Settings

The MUX select setting allows the user to choose the input type of the signal connected to the VINPP and VINPN pins of the device. For a differential signal, select VINPP – VINPN, and for single-ended signals the user can choose either VINPP – 1.25 V, or 1.25 V – VINPN depending on which of the input pins the signal is connected to. The *Single Ended Input* box must also be selected if using a single-ended input signal. Additionally, the input signal can be inverted if desired by checking the *Invert Signal* box. The *Single Ended Input* and *Invert Signal* check boxes are available for both the P Gain and T Gain input blocks, and can be configured separately.

4.5.3 P Channel and T Channel

Both the P Channel and T Channel blocks have adjustable gains with a range of 1.33 V/V up to 200 V/V to properly amplify any input signal to take advantage of the full input range of the ADC.

4.5.4 P/T Channel Select

The *P/T Channel MUX Select* allows the user to determine which input signals are directed to the ADC of the PGAxxx device. In fixed-channel mode, either the P Channel or T Channel inputs can be directed to the ADC for sampling. The *Auto Scan* mode allows the ADC to sample from both the P Channel and the T Channel at user-defined intervals.

4.5.5 T Channel MUX Select

The T Channel MUX Select allows the user to determine which signals will be passed through the T Channel to the ADC for sampling. The VINTP and VINTN pin option can be selected for use with an external temperature sensor, or other sensor. To use the internal temperature sensor of the PGAxxx device, select the *Internal Temp Sense* option. The *Bridge Current* option allows the user to read the current through the internal VBRG voltage supply of the PGAxxx device. Additionally, the TEST1 pin can be MUXed through to monitor a variety of internal signals for debugging purposes. The output of the TEST1 pin can be set on the *Test Mode* page (see Section 4.10). Finally, the DACCAP pin can be used as an additional input if desired, and can be sent through the MUX to the ADC for sampling.

4.5.6 Block Enable Check Boxes

There are several block enable check boxes on the analog front end page. The ITEMP enable box will turn on and connect the internal temperature sensor current source for use with external temperature sensors that need current excitation. The VBRG enable box activates the internal bridge voltage supply to provide voltage excitation for resistive bridge pressure sensors. The ADC is enabled with a check box, and finally the DACCAP can be connected with an enable check box to provide a low-pass filter to the DAC output buffer.

4.5.7 ITEMP Select

ITEMP select gives the user the option to select the current output of the ITEMP internal current source. The current source can supply 50 to 1000 μ A, or it can be disabled with this control.

4.6 Output DAC Page

Figure 12 illustrates the output DAC page.





Figure 12. Output DAC Page

The *Output DAC* page allows the user to quickly test the functionality of the output DAC by inputting specific DAC Values and monitoring the result at the VOUT pin. The output DAC and DACCAP connections can also be enabled or disabled from this page. To easily read the voltage on VOUT, the user can use the *Voltage Monitor* tab on the tool panel to the right.

4.7 Diagnostics Page

Figure 13 shows the diagnostics page.



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Figure 13. Diagnostics Page



4.7.1 DAC Loopback Diagnostics Section

The DAC Loopback Diagnostics section allows the user to ensure proper signal chain operation by reading the DAC output through the ADC. With the feedback loop enabled, the user can set a DAC value, and then read the resulting ADC value on the Data Monitor page (see Section 4.14) to check for agreement.

4.7.2 Sensor Connectivity Diagnostic Resistors Section

The Sensor Connectivity Diagnostic Resistors section allows the user to enable the sensor diagnostic resistors to monitor short and open conditions on the sensor input pins. The output of these diagnostics is available in the *Fault Status* tab of the tool panel to the right under the AFE Diagnostics Section. Short and open conditions can be determined using the VINTP, VINTN, VINPP, and VINPN undervoltage and overvoltage fault status bits in combination with the internal pulldown resistors.

4.8 SENT Interface Page (PGA 904 Only)

The SENT Interface page (see Figure 14) allows the user to control SENT settings, and to test communication on both the fast and slow communication channels.

EVM Settings Device Configuration Cevice Settings General Analog Front End Diagnostics <u>SENT Interface</u> Memory Map Test Mode Memory Program Data Monitor	SENT Enable Data Length (Nibbles): 3 • Tick Period (us): 3 • Pause Pulse OFF ON (Determined by SENT Frame Length) ON (Determined by SENT Frame Length)	Serial Message (Slow Channel) Slow Channel Enable Slow Channel Format
	 ON (Constant Pause Pulse Value) 	Short
	Frame Length (Ticks): 0	Enhanced Config. Bit Value: 0 -
	Test Fast Channel	Test Slow Channel Status and Comm. Data: 00 👻
	Data: 0x000000	Message ID: 0x00 Data: 0x0000
	Send Fast Data	Send Slow Data

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Figure 14. SENT Interface Page

Data length controls the number of fast data *Nibbles* (4 bits) that will be sent within each transmission, and the *Tick* period determines the overall speed of the data output.



The pause pulse at the end of each data transmission can be either disabled or turned on with three options for how the length of the pause pulse is determined.

The serial message, or slow channel communication can be enabled and configured. The slow channel data will be contained in small portions as part of the STATUS frame at the beginning of each transmission, when enabled. Short mode will send only 8 bits, while enhanced mode will allow the user to send 12 or 16 bits depending on the *Enhanced Config Bit* value (0b0 = 12 bits and 0b1 = 16 bits).

Both the fast- and slow-channel communication can be tested from the SENT interface page. Note that when a test signal is begun, it will continuously output the test data until the SENT interface is disabled.

4.9 Memory Map Page

The *Memory Map*, shown in Figure 15, allows low-level access to all available registers in the PGAxxx device. Any changes made to the map on the left are not finalized until the user clicks either the *Write Selected* or *Write All* buttons to the right of the grid.

The user can save a grid or load a previously saved grid. Note that only the active tab will be saved to a file when saving a grid. The file created when saving the EEPROM tab grid is interchangeable with the file created when saving the EEPROM settings on the *Memory Program* page (see Section 4.11).

ADDRESS / REGISTER NAME	REG	b7	b6	b5	b4	b3	b2	b1	bO	
0x00 REVISION_ID [7:0]	00	0	0	0	0	0	0	0	0	
0x01 REVISION_ID [11:8]	00	0	0	0	0	0	0	0	0	Destauted
0x04 COM_MCU_TO_DIF_B1	00	0	0	0	0	0	0	0	0	Read Selected
0x05 COM_MCU_TO_DIF_B2	00	0	0	0	0	0	0	0	0	
0x06 COM_TX_STATUS	00	0	0	0	0	0	0	0	0	
0x08 COM_DIF_TO_MCU_B1	00	0	0	0	0	0	0	0	0	write Selected
0x09 COM_DIF_TO_MCU_B2	00	0	0	0	0	0	0	0	0	
0x0ACOM_RX_STATUS	00	0	0	0	0	0	0	0	0	Bood All
0x0B COM_RX_INT_ENABLE	00	0	0	0	0	0	0	0	0	Read All
0x0C MICRO_INTERFACE_CONTROL	00	0	0	0	0	0	0	0	0	
0x0D SECLOCK	00	0	0	0	0	0	0	0	0	Write All
0x10 PADC_DATA [7:0]	00	0	0	0	0	0	0	0	0	
0x11 PADC_DATA [15:8]	00	0	0	0	0	0	0	0	0	
0x12 PADC_DATA [23:16]	00	0	0	0	0	0	0	0	0	
0x13 PADC_DATA [31:24]	00	0	0	0	0	0	0	0	0	
0x14 TADC_DATA [7:0]	00	0	0	0	0	0	0	0	0	ZERO GRID
0x15 TADC_DATA [15:8]	00	0	0	0	0	0	0	0	0	
0x16 TADC_DATA [23:16]	00	0	0	0	0	0	0	0	0	DESELECT GRID
0x17 TADC_DATA[31:24]	00	0	0	0	0	0	0	0	0	
0x18 ADC_VALID	00	0	0	0	0	0	0	0	0	SAVE GRID
0x1C MCU_MON [7:0]	00	0	0	0	0	0	0	0	0	
0x1D MCU_MON [15:8]	00	0	0	0	0	0	0	0	0	LOAD GRID
0x1E MCU_MON [23:16]	00	0	0	0	0	0	0	0	0	
0x1F MCU_MON [31:24]	00	0	0	0	0	0	0	0	0	

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Figure 15. Memory Map Page



Software

4.10 Test Mode Page

		3	
Analog Test Modes			
Analog Output Test MUX Select :	TEST1	- Enable	
	VINTP	VINTN	
Analog Input Test MUX Select :			- Enable
Note: The Analog Output Test MUX	(pin is TEST1, while the Ar	nalog Input Test MUX pins are \	/INTP and VINTN
Digital Test Modes			
TEST1 Digital Output Test MUX	Digital Test M	ode Enable	Ţ

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Figure 16. Test Mode Page

The *Test Mode* page (see Figure 16) provides access to the analog and digital test MUX settings of the PGAxxx device. The analog and digital test MUX outputs are output through the TEST1 pin, while the analog test MUX inputs are connected to the VINTP and VINTN pins. A variety of internal signals are accessible through these options for debugging purposes, but a full description of this functionality is outside the scope of this document.



4.11 Memory Program Page

LEF KOW Save	Load EEPROM File	Program calculated CRC
Program	Verify	0%
		•
TP Memory		
Check OTP Status	Load OTP File	
Program	Verify	0%
		^ ^
		-
	lory	
evelopment RAM Mem		Remap Enabled
DEVRAM Remap	LOad DEVRAM File	
DEVRAM Remap	Verify	Remap to ROM
DEVRAM Remap Program	Verify	
DEVRAM Remap Program	Verify	0%
DEVRAM Remap Program	Verify	0%

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Figure 17. Memory Program Page

For the EEPROM Memory, the user can load or save a memory map file as well as program the calculated CRC. It is a good practice to verify the EEPROM after each programming procedure. Note that the file loaded and saved on this page is interchangeable with the file that can be loaded or saved on the *Memory Map* page when viewing the EEPROM tab.

NOTE: The OTP Memory and Development RAM Memory sections are only available in the PGA902 and PGA904 EVM GUIs.



The Check OTP Status button allows the user to see if the OTP memory has already been burned on their PGAxxx device. An OTP file can be loaded and then programmed and verified in the OTP Memory Section.

When using the DEVRAM, the DEVRAM memory space must be remapped to the OTP memory so that the microcontroller operates from the correct memory. Select the *Remap to OTP* radio button, and click the *DEVRAM Remap* button before continuing. Once completed, a DEVRAM file can be loaded, programmed, and verified.



Calibration Model : 4 Pressure, 4	Temperature 👻		VDD Supply Vo	Itage : [V]		
Target System OutputPressure 1: Vout = 0.5 [V]Pressure 2: Vout = 1.8333 [V]Pressure 3: Vout = 3.1666 [V]Pressure 4: Vout = 4.5 [V]Desired VDD = [V]	System Output Calib DAC Code 1: 0x 0666 2: 0x 1777 3: 0x 2888 4: 0x 3999	Temp 1 Vout 1 : Vout 2 : Vout 3 : Vout 4 : t Calibration (Sens	AC Gain) Temp 2 Ter International Content of	mp 3 Temp 4		
Note: Press 1 < Press 2 < Press 3 < F Temp1 < Temp2 < Temp3 < Tem DAC 1 < DAC 2 < DAC 3 < DAC Advanced Options	Pressure 1 Press 4 Pressure 2 Pressure 3 Pressure 3 Pressure 4 Pressure 4	0x 0x 0x 0x		p 3 Temp 4 0x 0x 0x 0x 0x 0x 0x 0x 0x 0x		
Average Samples : 8 🚔 Full Data Manual Entry 🔲		START	Cance	1		
Message Center						

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Figure 18. PGA302 Linearity Calibration Page



One of the key features of the PGA302 pressure sensor signal conditioner is the preprogrammed firmware which includes linearization and temperature compensation algorithms to provide reliable results from a variety of pressure sensors in real world systems. To maximize the effectiveness of these algorithms, calibration of the PGA302 device for each sensor is critical. The PGA302 Linearity Calibration panel provides a simple interface to calibrate the input and output stages of the PGA302 device with minimal external equipment. The following example procedure will walk the user through the calibration process by using the onboard resistive bridge to simulate a pressure sensor.

4.12.1 PGA302 Linearity Calibration Procedure

- 1. Follow the *PGAxxxEVM-037 Quick Start Procedure* (Section 3.1) to power up the EVM and establish communication with the PGAxxx device. Make sure that the jumpers are set to their default position as shown in Table 1.
- 2. Place the microcontroller in Reset by clicking the Microcontroller State field.
- 3. Select the Calibration Model you wish to use. For this example, select "3 Pressure, 1 Temperature"
- 4. Click *START* at the bottom of the page, and follow the prompts from the message center below the *START* button.
- 5. Update the desired output voltage for Pressure 1 and click *NEXT* when finished. Repeat this process for Pressure 2 through Pressure 4. In this case (3 Pressure, 1 Temperature), Pressure 3 is not accessible for updating.
- 6. Update the desired DAC Code for Pressure 1 and click *NEXT* when finished. Repeat this process for Pressures 2 and 4.
- 7. Click NEXT again. Check the value in the Vout 1 row under the column Temp 2. This value will be automatically populated with the Vout voltage output associated with the DAC code entered in the previous step. The voltage is measured by the ADC in the MSP430 microcontroller on the PGAxxxEVM-037. If you wish to verify the voltage with an external voltage meter, measure the voltage on the VOUT_SENT test point on the EVM. The voltage value can be left as is, or an updated value can be manually entered by the user. Once the value is set, click NEXT. Repeat this process for Vout 2, and Vout 4.
- 8. Before continuing, set the number of *Average Samples* to use in the *Advanced Settings* section of the page. This value can range from 1 to 128 and will average the number of samples selected to generate the ADC value populated in the calibration algorithm. Increasing the number of samples averaged will increase the amount of time it takes for the ADC value to populate. For this example, the default value of 8 will be selected.
- 9. Set the resistive bridge leg resistance to the desired value using the *Resistive Bridge Configuration* panel. For this example use "5.0850k" as the Pressure 1 value. Click *NEXT* when finished. The cell will be populated automatically with the value read by the ADC. If the value does not populate properly, or if the value does not seem correct, the *Data Monitor* page (see Section 4.14) can be used to help debug by reading the ADC values in real time. The value in the cell can be manually entered at any time by clicking the *Full Manual Data Entry* checkbox.
- 10. Set the resistive bridge leg resistance to the second pressure value. For this example, use "5.0806k". Once complete, click *NEXT* to populate the ADC value in the cell. Repeat this process for the third and final pressure point, using a resistive bridge leg resistance of "5.0713k".
- 11. After completing the pressure readings, click *NEXT* to populate the temperature cell. The cell will be automatically populated with the ADC value read from the internal temperature sensor of the PGA302. Click *NEXT* again.
- 12. The VDD Supply Voltage field will now be automatically populated with the value measured by the ADC of the MSP430. If desired, the *VDD Supply Voltage* can be measured externally from the test point labeled *VDD* on the EVM, and entered manually into the calibration page. Click *NEXT* again.
- 13. Now the desired VDD Supply Voltage field will be populated. Click NEXT again.
- 14. Click *CALCULATE*. This will use the data generated through the calibration procedure to calculate the coefficient values for linearity and temperature compensation and display them in the message center at the bottom of the page. Click *PROGRAM* to program the values to the EEPROM.
- 15. Navigate to the *PGA302 EEPROM Settings* page to verify the coefficients have been populated in the *Linearity Calibration Parameters* section of the page. While on this page, click the *UPDATE* button to correct the EEPROM CRC value. The PGA302 device is now fully calibrated.



- 16. To test the results of the calibration click the *Microcontroller State* field to begin running the microcontroller, and navigate to the *Voltage Monitor* tab in the tool panel.
- 17. Select the second pressure point in the *Resistive Bridge Configuration* panel, by setting the resistance of the leg to "5.0806k". The VOUT voltage in the tool panel should match the voltage selected for the Pressure 2 output during the calibration procedure.

4.13 PGA302 EEPROM Settings Page (PGA302 Only)

Figure 19 illustrates the PGA302 EEPROM settings page.

Linearity Calibratio	n Parameters				
H0 : 0x 0000	G0 : 0x 0000	N0 : 0x 0000 M0	: 0x 0000 F	PADC GAIN : 0x 00	Algorithm Type
	C1:0x 0000	N1 : 0x 0000 M1	· 0x 0000 T		Normal
	G1.0x 0000	NO. 0. 0000 MT	. 0. 0000 1		
H2:0x 0000	G2:0x 0000	N2:0x 0000 M2	: 0x 0000	PADC OFF : 0X 0000	
H3 : 0x 0000	G3:0x 0000	N3:0x 0000 M3	: 0x 0000	TADC OFF : 0x 0000	
Analog Front End §	Settings				
P Channel I	nput	T Channel Input		T Channel Current)rive
Single	Ended Input : 📃	Single E	nded Input : 📃	ITEMP Select : 50	✓ uA
	nvert Signal :		vert Signal : 📗	Destination : VINT	rp 👻
P GAIN : 1.	33 🔻	T GAIN : 1.33 ▼			
P MUX : VI	NPP - VINPN 👻	T MUX : VINTP - VI	NTN Pins 👻		
Offset Corr :	OFF 👻 mV				
DAC Output Setting DAC	gs CLevel During Diag	nostic Fault : 0x 00 0	0	DACCAP Pin Enable :	
No	rmal Output Range	High Limit : 0x 0000	Output Hi	gh Clamp Limit : 0x 0000	0
No	ormal Output Range	e Low Limit : 0x 0000	Output L	ow Clamp Limit : 0x 0000	0
Diagnostics Enabl	e		E	EPROM Lock : 📃	
VINP_OV :	PGAIN_OV:		Diagnostics 0	Global Enable : 🔳	
VINP_UV:	PGAIN_UV:	Production	n Serial Number	: 0x 0000000	
VINT_OV :	TGAIN_OV:		Output IIR Filter (Cut-Off : OFF 👻 [Hz]	
VINT_UV:	TGAIN_UV:				
	_	Co	rrect EEPROM C	RC : Update	
ote: When Updatin	o Text Box Paramet	ers. pess the "Enter" k	ev to program ch	andes.	
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Figure 19. PGA302 EEPROM Settings Page



When making changes to any parameters on the PGA302 EEPROM settings page, the new settings are automatically burned to the EEPROM. No separate programming action is required. However, it is necessary to update the CRC once any of the EEPROM settings have been changed, including at the end of a calibration procedure.

4.13.1 Linearity Calibration Parameters

The linearity calibration parameters are automatically set once the *Linearity Calibration Procedure* (see Section 4.12.1) has been completed. No user input is necessary; however, individual coefficients can be changed manually if desired.

4.13.2 Analog Front End Settings

The Analog Front End Settings are the same as those included in the Analog Front End block diagram panel. To program the settings in the EEPROM, they must be entered in the PGA302 EEPROM Settings panel. For a full description of the Analog Front End Settings, see Section 4.5.

4.13.3 DAC Output Settings

The DAC Output Settings allow the user to configure the DAC output ranges as well as the DAC output level during a fault.

4.13.4 Diagnostics Enable

Allows the user to enable analog front end diagnostic bits to be viewed in the *Fault Status* tab. See Table 6 for a description of diagnostic bits.

4.13.5 Other Settings

Other settings on this page include locking the EEPROM so that the values cannot be changed, enabling all diagnostics with a single check box, viewing the production serial number of the PGA302 device (read only), or setting the *IIR Filter Cutoff* frequency.



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4.14 Data Monitor Page

X-Axis: San Y-Axis: LSE	nples Code			Record Lengt	h: 512 🚔 [Samples]
X - Axis : San Y - Axis : LSE Data Source	nples Code			Record Lengt	h : 512 🚔 [Samples]
X - Axis : San Y - Axis : LSE Data Source V P ADC	PADC Value :	0 LSB	3: 0 x 0000000	Record Lengt	h : 512 🚔 [Samples]
X - Axis : San Y - Axis : LSE Data Source V P ADC T ADC	PADC Value : TADC Value :	0 LSB 0 LSB	9: 0 x 0000000 9: 0 x 0000000	Record Lengt	h : 512 🚔 [Samples] Loop 🔽
X - Axis : San Y - Axis : LSE Data Source P ADC TRACE FIFO	PADC Value : TADC Value :	0 LSB 0 LSB	8: 0 x 0000000 8: 0 x 0000000	Record Lengt	h : 512 🚔 [Samples] Loop 🔽 RUN
X - Axis : San Y - Axis : LSE Data Source I P ADC T ADC TRACE FIFO	PADC Value : TADC Value : TADC Value :	0 LSB 0 LSB atus:	9: 0 x 00000000 9: 0 x 00000000	Record Lengt	h : 512 🚔 [Samples] Loop RUN Clear Plot

Figure 20. Data Monitor Page

The *Data Monitor* page (see Figure 20) allows you to see the ADC sample values being read in real time. Data can be read from the P Channel, the T Channel, or both on the same graph. The number of samples recorded can be adjusted from 128 to 4096. By default, the graph will continually loop until it is stopped by the user, but by unchecking the *Loop* checkbox the samples will stop when the record length is reached.

Data can be exported to a .txt file format by clicking the *Export Data* button. The file contains all of the data currently displayed in the plot in a comma separated value format with the sample number, the P channel value, and the T channel value for each sample for easy data manipulation.



4.15 Tool Panel



Figure 21. Tool Panel

4.15.1 Utilities Tab

The *UTILITIES* tab (see Figure 22) includes useful tools for interacting with the low level memory of the PGAxxx device and for communication debugging purposes.



UTILITIES	Data Log	Voltage	Monitor	Fault Status	
-Base Cor	verter				
	Decimal :			255	
He	-Decimal :			FF	
	Binary :		111111111	111111	
EVM Low	Level Com	municat	ion		
12C: 1	Device Addr	ress: Ox	Dat	a Write: 0x	
Re	egister Addı	ress: Ox	Dat	a Read: 0x	
	120	C Write		C Read	
owi:	Transmit	Buffer:	Receive I	Buffer:	
	0x		0x	*	
	0x		0x		
	0x		0x		
	UX Ox		UX Ox		
	0x		0x		
	0x		0x		
OWI Se	nd 0x	~	0x	- OWI Rea	d

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Figure 22. UTILITIES tab

4.15.1.1 Base Converter

A base converter is included to quickly convert among decimal, hexadecimal, and binary number systems. Simply type a number into one of the three fields, and press the enter key to populate the converted values in the remaining two fields.

4.15.1.2 EVM Low-Level Communication

The *EVM Low-Level Communication* section allows for direct access to device registers, and provides an easy method to debug I2C and OWI communications. To configure a specific register enter the I2C device address, the PGAxxx device register address desired, and the register value in the *Data Write* field then click the *I2C Write* button to send the data.

4.15.2 Data Log tab

The *Data Log* tab (see Figure 23) logs all communication functions between the GUI and the PGAxxx device. Each line displays the communication type, followed by whether data was read or written, and finally the actual data in hexadecimal form.



UTILITIE S	Data Log	Voltage Monitor	Fault Status
🔽 ENAI	BLE		Clear
I2C Write I2C Read I2C Write I2C Write I2C Write I2C Write	e: 0x40 0x00 : 0x40 0x00 e: 0x42 0x33 e: 0x42 0x65 e: 0x42 0x04 e: 0x42 0x04 e: 0x42 0x04	C 0x00 C Return Data: 0x 8 0x01 7 0x01 B 0x02 4 0x01 4 0x00	¢00
			Ŧ

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Figure 23. Data Log Tab



4.15.3 Voltage Monitor Tab

The *Voltage Monitor* as illustrated in Figure 24 provides a quick way to check vital system voltages for EVM functionality and debugging purposes. These voltages are measured via the ADC in the MSP430 microcontroller included on the EVM.

UTILITIES	Data Log	Voltage Monitor	Fault Status	
	VOUT :	0.014666308593	[V]	
	TEOT4 -	2 202640440240	D.0	
	IESIT.	2.302010449218	[v]	
	TEST2 :	1.794178417968	M	
	VCC :	4.859039496093	[V]	

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Figure 24. Voltage Monitor Tab



4.15.4 Fault Status tab

The *Fault Status* tab shown in Figure 25 includes fault status registers for the digital interfaces, OWI status, the power supply monitor, and AFE diagnostics for quick diagnosis and debug of the most common device and EVM issues. Table 6 describes the available fault status bits. Note that the *AFE Diagnostics* must be enabled in the EEPROM Settings before they are updated in the *Fault Status* tab.

UTILITIES Data Log	Voltage Monito	or Fault Status					
Digital Interface Error Status							
0 I2C_ERR	0 OWI_ERR	0 TF_ERR					
OWI Error Status							
0 SYNC <320bps	6 0	DATA STOP Bad					
0 SYNC >9600bp	os 0	DATA STOP Short					
0 SYNC STOP St	nort 0	DATA STOP Override					
0 CMD STOP Bac	d 0	SYNC Tolerance Err					
0 CMD STOP She	ort 0	OWI Invalid CMD					
Power Supply Monit	or (PSMON1)						
0 VBRG_OV	0 REF_OV	0 DVDD_OV					
0 VBRG_UV	0 REF_UV	0 DVDD_UV					
AFE Diagnostics (AF	EDIAG)						
0 VINP_OV	0	PGAIN_OV					
0 VINP_UV	0	PGAIN_UV					
0 VINT_OV	0	TGAIN_OV					
0 VINT_UV	0	TGAIN_UV					

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Figure 25. Fault Status tab

Table 6. Fault Status Indicators

Fault Indicator	Description
I2C_ERR	An error response on the access from I2C during access to the slave
OWI_ERR	An error response on the access from OWI during access to the slave
TF_ERR	Error response on the access from Trace FIFO
SYNC <320BPS	SYNC field data rate under 320 bits per second
SYNC >9600BPS	SYNC field data rate over 9600 bits per second
SYNC STOP Short	SYNC stop bit too short
CMD STOP Bad	Incorrect CMD stop bit value
CMD STOP Short	CMD stop bit too short
Data STOP Bad	Incorrect DATA stop bit value
Data STOP Short	DATA stop bit too short
Data STOP Override	DATA Field slave transmit value overdriven to dominant value during stop bit transmit
SYNC Tolerance Err	Consecutive bits in the sync field are different by more than ±25% tolerance

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Fault Indicator	Description				
OWI Invalid CMD	OWI command field invalid. See device datasheet for available OWI commands				
VBRG_OV	Bridge Supply OV Flag; Bridge Supply voltage > 1.15 times nominal value				
VBRG_UV	Bridge Supply UV Flag; Bridge Supply voltage < 0.85 times nominal value				
REF_OV	Reference OV Flag; Reference voltage > 1.1 times nominal value				
REF_UV	Reference UV Flag; Reference voltage > 0.9 times nominal value				
DVDD_OV	DVDD OV Flag; DVDD voltage > 1.15 times nominal value				
DVDD_UV	DVDD UV Flag; DVDD voltage < 0.9 times nominal value				
VINP_OV	Overvoltage on VINPP or VINPN pins				
VINP_UV	Undervoltage on VINPP or VINPN pins				
VINT_OV	Overvoltage on VINTP or VINTN pins				
VINT_UV	Undervoltage on VINTP or VINTN pins				
PGAIN_OV	Overvoltage at PGAIN output				
PGAIN_UV	Undervoltage at PGAIN output				
TGAIN_OV	Overvoltage at TGAIN output				
TGAIN_UV	Undervoltage at TGAIN output				

Table 6. Fault Status Indicators (continued)

4.15.5 Resistive Bridge Configuration Panel



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Figure 26. Resistive Bridge Configuration Panel

The *Resistive Bridge Configuration* panel allows the user to control the digital potentiometer that makes up one leg of the resistive bridge emulator on the EVM. This can be used to generate a differential voltage across the VINTP and VINTN or the VINPP and VINPN pins depending on the jumper configuration. The drop-down box allows the user to select a resistance in $k\Omega$; the resulting change in the Vp voltage as well as the differential voltage of Vp – Vn are automatically updated in the schematic.



5 Board Layout

Figure 27 through Figure 30 illustrate the EVM PCB layouts.



Figure 27. Top Layer





Figure 28. Top Component Placement



Board Layout



Figure 29. Bottom Layer







Figure 30. Bottom Component Placement



6 Schematic and Bill of Materials

6.1 Schematic

NOTE: The schematic pictured in Figure 31 shows the board configuration for the PGA904EVM which includes additional components populated for OTP programming and a socket for the PGAxxx devices.



Schematic and Bill of Materials

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Figure 31. PGA302EVM Schematic







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Figure 32. PGAxxxEVM MSP430 Interface Schematic

6.2 Bill of Materials

NOTE: The bill of materials in Table 7 shows the components for the PGA904EVM-037. The PGA302EVM-037 and PGA904EVM-037 contain fewer components, but any component present on all three boards will have the same value and part number.

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		MHR037	Any		
C4, C7, C9, C10, C20, C21, C23, C40	8	0.1uF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet		
C5	1	100uF	CAP, AL, 100 µF, 35 V, ±20%, SMD	F80	EMVA350ADA101MF80G	Chemi-Con		
C6	1	100uF	CAP, AL, 100 µF, 35 V, ±20%, 0.34 ohm, SMD	F80	EMZA350ADA101MF80G	Chemi-Con		
C11, C19, C29	3	2200pF	CAP, CERM, 2200 pF, 50 V, ±10%, X7R, 0603	0603	C0603C222K5RAC	Kemet		
C13, C14, C17, C18	4	0.15uF	CAP, CERM, 0.15 µF, 16 V, +80/-20%, Y5V, 0603	0603	C0603C154Z4VACTU	Kemet		
C15	1	470pF	CAP, CERM, 470 pF, 50 V, ±10%, X7R, 0603	0603	C0603C471K5RACTU	Kemet		
C22	1	0.47uF	CAP, CERM, 0.47 µF, 10 V, ±10%, X5R, 0603	0603	C0603C474K8PACTU	Kemet		
C24, C25, C26	3	1uF	CAP, CERM, 1 µF, 16 V, ±10%, X5R, 0603	0603	C0603C105K4PACTU	Kemet		
C27, C32	2	220pF	CAP, CERM, 220pF, 50V, ±1%, C0G/NP0, 0603	0603	06035A221FAT2A	AVX		
C28	1	220pF	CAP, CERM, 220 pF, 50 V, ±10%, C0G/NP0, 0603	0603	C0603C221K5GACTU	Kemet		
C30	1	100pF	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, 0603	0603	C0603C101J5GAC	Kemet		
C31	1	2200pF	CAP, CERM, 2200pF, 50V, ±10%, X7R, 0603	0603	C0603X222K5RACTU	Kemet		
C33	1	0.47uF	CAP, CERM, 0.47 µF, 10 V, ±10%, X5R, 0402	0402	C1005X5R1A474K050BB	TDK		
C34, C35, C36	3	0.1uF	CAP, CERM, 0.1 µF, 10 V, ±10%, X5R, 0402	0402	C1005X5R1A104K	TDK		
C37, C38	2	30pF	CAP, CERM, 30 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H300JA01D	Murata		
D1	1	75V	Diode, Switching, 75 V, 0.3 A, SOT-23	SOT-23	BAV99-7-F	Diodes Inc.		
D2	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On		
D3	1	75V	Diode, Switching, 75 V, 0.3 A, SOD-523	SOD-523	1N4148X-TP	Micro Commercial Components		
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	BandF Fastener Supply		
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone		
J1, J2, J3	3		Therminal Block, 5 mm, 2-pole, TH	TH, 2-Leads, Body 10x9mm, Pitch 5mm	1935161	Phoenix Contact		
J4, J5, J6, J7, J9	5		Header, 100mil, 3x1, Gold, SMT	Samtec_TSM-103-01- X-SV	TSM-103-01-L-SV	Samtec		
J8	1		Conn Rcpt Mini USB2.0 Type B 5POS SMD	USB Mini Type B	1734035-2	TE Connectivity		
J11	1		Header, 100mil, 2x1, Gold with Tin Tail, SMT	2x1 Header	TSM-102-01-L-SV	Samtec		
J12	1		Header, 100mil, 10x2, Tin, SMT	1000x180x290mil	TSM-110-01-T-DV-P	Samtec		
J13, J14	2		Standard Banana Jack, Uninsulated, 5.5mm	Keystone_575-4	575-4	Keystone		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650"H x 0.200"W	THT-14-423-10	Brady		

Table 7. Bill of Materials⁽¹⁾

⁽¹⁾ Unless otherwise noted in the Alternate Part Number or Alternate Manufacturer columns, all parts may be substituted with equivalents.



Table 7. Bill of Materials⁽¹⁾ (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
PWR	1	Green	LED, Green, SMD	2x1.25mm	LG R971-KN-1	OSRAM		
Q1	1	40 V	Transistor, PNP, 40 V, 0.2 A, SOT-23	SOT-23	MMBT3906-7-F	Diodes Inc.		
R1, R4, R27, R28	4	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo America		
R2, R5, R7, R55	4	10.0	RES, 10.0, 1%, 0.1 W, 0603	0603	RC0603FR-0710RL	Yageo America		
R9, R11, R15, R17, R53	5	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo America		
R10	1	1.2k	RES, 1.2 k, 5%, 0.1 W, 0603	0603	RC0603JR-071K2L	Yageo America		
R12	1	2.40k	RES, 2.40 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K4L	Yageo America		
R13	1	2.37k	RES, 2.37 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K37L	Yageo America		
R14, R22, R42, R45, R49, R51	6	4.70k	RES, 4.70 k, 1%, 0.1 W, 0603	0603	RC0603FR-074K7L	Yageo America		
R16	1	17.8k	RES, 17.8 k, 1%, 0.1 W, 0603	0603	RC0603FR-0717K8L	Yageo America		
R18	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo America		
R19, R52	2	6.19k	RES, 6.19 k, 1%, 0.1 W, 0603	0603	RC0603FR-076K19L	Yageo America		
R20	1	0	RES, 0, 5%, 0.125 W, 0805	0805	RC0805JR-070RL	Yageo America		
R21	1		TRIMMER 10K OHM 0.1W	3.8x3.6mm	TC33X-2-103E	Bourns		
R23	1	0	RES, 0, 5%, 0.125 W, 0805	0805	CRCW08050000Z0EA	Vishay-Dale		
R24	1	2.55k	RES, 2.55 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD072K55L	Yageo America		
R25, R29, R30	3	4.99k	RES, 4.99 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD074K99L	Yageo America		
R26	1	2.61k	RES, 2.61 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD072K61L	Yageo America		
R31, R32	2	33	RES, 33 ohm, 5%, 0.063W, 0402	0402	CRCW040233R0JNED	Vishay-Dale		
R33	1	1.5k	RES, 1.5k ohm, 5%, 0.063W, 0402	0402	CRCW04021K50JNED	Vishay-Dale		
R34	1	1.07Meg	RES, 1.07Meg ohm, 1%, 0.1W, 0603	0603	CRCW06031M07FKEA	Vishay-Dale		
R35, R47	2	33k	RES, 33k ohm, 5%, 0.063W, 0402	0402	CRCW040233K0JNED	Vishay-Dale		
R36	1	2.7k	RES, 2.7 k, 5%, 0.1 W, 0603	0603	RC0603JR-072K7L	Yageo America		
R37	1	27.0k	RES, 27.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0727KL	Yageo America		
R38	1	76.8k	RES, 76.8 k, 1%, 0.1 W, 0603	0603	RC0603FR-0776K8L	Yageo America		
R39	1	560	RES, 560, 1%, 0.1 W, 0603	0603	RC0603FR-07560RL	Yageo America		
R40	1	82.0k	RES, 82.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0782KL	Yageo America		
R41, R44, R48	3	2.43k	RES, 2.43 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K43L	Yageo America		
R50	1	9.53k	RES, 9.53 k, 1%, 0.1 W, 0603	0603	RC0603FR-079K53L	Yageo America		
R54	1	220	RES, 220, 1%, 0.1 W, 0603	0603	RC0603FR-07220RL	Yageo America		
R59	1	470k	RES, 470 k, 1%, 0.0625 W, 0402	0402	RC0402FR-07470KL	Yageo America		
RT1	1	10.0k ohm	Thermistor NTC, 10.0k ohm, 1%, 0402	0402	NCP15XH103F03RC	Murata		
S1	1		Switch, Tactile, SPST-NO, 0.1A, 16V, SMT	4.93x4.19x6.2 mm	7914G-1-000E	Bourns		
SH-J4, SH-J5, SH-J6, SH-J7, SH-J9	5		Shunt, 100mil, Gold plated, Black	Shunt 2 pos. 100 mil	881545-2	TE Connectivity		
TP1, TP2, TP3	3	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
U1	1		Sensor Signal Conditioner with 0-5V Ratiometric Output, PW0016A (TSSOP-16)	PW0016A	PGA302PWQ1	Texas Instruments		



Table 7. Bill of Materials⁽¹⁾ (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
U2	1		Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitor, DCK0006A (SOT-6)	DCK0006A	INA210BIDCKR	Texas Instruments	INA210BIDCKT	Texas Instruments
U3	1		DUAL DIFFERENTIAL COMPARATORS, DGK0008A	DGK0008A	LM2903DGKR	Texas Instruments		Texas Instruments
U4	1		3-TERMINAL ADJUSTABLE REGULATOR, DCY0004A	DCY0004A	LM317DCYR	Texas Instruments	LM317DCY	Texas Instruments
U6	1		256 Taps Single Channel Digital Potentiometer With SPI Interface, DCN0008A	DCN0008A	TPL0501-100DCNR	Texas Instruments		
U7	1		36-V, Single-Supply, Low-Power Operational Amplifier for Cost-Sensitive Systems, D0008A (SOIC-8)	D0008A	TLV2171IDR	Texas Instruments		
U8	1		Dual Output High PSRR LDO, 200 mA, Fixed 3.3, 1.8 V Output, 2 to 5.5 V Input, 6-pin WSON (DSE), -40 to 125 degC, Green (RoHS and no Sb/Br)	DSE0006A	TLV7113318DDSER	Texas Instruments	Equivalent	Texas Instruments
U9	1		25 MHz Mixed Signal Microcontroller with 32 KB Flash, 4096 B SRAM and 47 GPIOs, -40 to 85 degC, 64-pin QFN (RGC), Green (RoHS and no Sb/Br)	RGC0064B	MSP430F5510IRGCR	Texas Instruments	Equivalent	Texas Instruments
U10	1		2-Bit Bidirectional Voltage-Level Translator for Open- Drain and Push-Pull Application, DQE0008A	DQE0008A	TXS0102DQER	Texas Instruments		
Y1	1		Crystal, 24 MHz, 18 pF, SMD	ABM3	ABM3-24.000MHZ-D2Y-T	Abracon Corporation		
C1	0	0.1uF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet		
C2, C8, C16	0	0.01uF	CAP, CERM, 0.01 µF, 25 V, ±5%, C0G/NP0, 0603	0603	C0603H103J3GACTU	Kemet		
C3	0	4.7uF	CAP, CERM, 4.7 µF, 10 V, ±10%, X5R, 0603	0603	C0603C475K8PACTU	Kemet		
C12	0	1uF	CAP, TA, 1 µF, 35 V, ±10%, 1.7 ohm, SMD	3528-21	T495B105K035ATE1K7	Kemet		
C39	0	2200pF	CAP, CERM, 2200 pF, 50 V, ±10%, X7R, 0603	0603	C0603C222K5RAC	Kemet		
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A		
J10	0		Header, 100mil, 2x1, Gold with Tin Tail, SMT	2x1 Header	TSM-102-01-L-SV	Samtec		
R3	0	25.5k	RES, 25.5 k, 1%, 0.1 W, 0603	0603	RC0603FR-0725K5L	Yageo America		
R6	0	4.70k	RES, 4.70 k, 1%, 0.1 W, 0603	0603	RC0603FR-074K7L	Yageo America		
R43, R46	0	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo America		
R57	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo America		
R58	0	4.70Meg	RES, 4.70 M, 1%, 0.1 W, 0603	0603	RC0603FR-074M7L	Yageo America		
U5	0		Single Output LDO, 50 mA, Adjustable 1.175 to 26 V Output, 7 to 28 V Input, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS and no Sb/Br)	DGN0008B	TPS7A4201DGNR	Texas Instruments	Equivalent	Texas Instruments
U11	0		Sensor Signal Conditioner with 0-5V Ratiometric Output, PW0016A (TSSOP-16)	PW0016A	PGA902PWQ1	Texas Instruments		
XU1	0		Socket, SOP-16, 0.65mm Pitch, TH	Socket, 16-Leads, Body 17.6X21.5mm, Pitch 0.65mm	OTS-16(28)-0.65-01	Enplas Tech Solutions		

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- 3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 Japan

- 3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に 輸入される評価用キット、ボードについては、次のところをご覧ください。 http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page
- 3.3.2 Notice for Users of EVMs Considered "Radio Frequency Products" in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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- 3.4 European Union
 - 3.4.1 For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 Safety-Related Warnings and Restrictions:
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
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- 10. Governing Law: These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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