

MSP430F415 Device Erratasheet

1 Functional Errata Revision History

Errata impacting device's operation, function or parametrics.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev E	Rev C
FLL3	✓	✓
PORT4		✓
PORT5		✓
PORT7		✓
TA12	✓	✓
TA16	✓	✓
TA21	✓	✓
TAB22	✓	✓
WDG2	✓	✓
XOSC9	✓	✓

2 Preprogrammed Software Errata Revision History

Errata impacting pre-programmed software into the silicon by Texas Instruments.

✓ The check mark indicates that the issue is present in the specified revision.

The device doesn't have Software in ROM errata.

3 Debug only Errata Revision History

Errata only impacting debug operation.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev E	Rev C
EEM20	✓	✓

4 Fixed by Compiler Errata Revision History

Errata completely resolved by compiler workaround. Refer to specific erratum for IDE and compiler versions with workaround.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev E	Rev C
CPU4	✓	✓



Refer to the following MSP430 compiler documentation for more details about the CPU bugs workarounds.

TI MSP430 Compiler Tools (Code Composer Studio IDE)

- MSP430 Optimizing C/C++ Compiler: Check the --silicon_errata option
- MSP430 Assembly Language Tools

MSP430 GNU Compiler (MSP430-GCC)

- MSP430 GCC Options: Check -msilicon-errata= and -msilicon-errata-warn= options
- MSP430 GCC User's Guide

IAR Embedded Workbench

• IAR workarounds for msp430 hardware issues

2



www.ti.com Package Markings

5 Package Markings

PM64

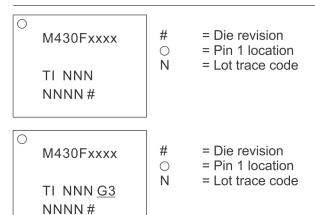
LQFP (PM), 64 Pin



= Die revision
O = Pin 1 location
N = Lot trace code

RTD64

QFN (RTD), 64 Pin





6 Detailed Bug Description

CPU4 CPU Module

Category Compiler-Fixed

Function PUSH #4, PUSH #8CPU4 - Bug

Description The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8.

The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is

different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround Refer to the table below for compiler-specific fix implementation information.

IDE/Compiler	Version Number	Notes
IAR Embedded Workbench	IAR EW430 v2.x until v6.20	User is required to add the compiler flag option belowhw_workaround=CPU4
IAR Embedded Workbench	IAR EW430 v6.20 or later	Workaround is automatically enabled
TI MSP430 Compiler Tools (Code Composer Studio)	v1.1 or later	
MSP430 GNU Compiler (MSP430-GCC)	MSP430-GCC 4.9 build 167 or later	

EEM20 EEM Module

Category Debug

Function Debugger might clear interrupt flags

Description During debugging read-sensitive interrupt flags might be cleared as soon as the

debugger stops. This is valid in both single-stepping and free run modes.

Workaround None.

FLL3 FLL+ Module

Category Functional

Function FLLDx = 11 for /8 may generate an unstable MCLK frequency

Description When setting the FLL to higher frequencies using FLLDx = 11 (/8) the output frequency

of the FLL may have a larger frequency variation (e.g. averaged over 2sec) as well as a lower average output frequency than expected when compared to the other FLLDx bit

settings.

Workaround None

PORT4 PORT Module

Category Functional



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Function SIF clock output depends on P2.7 AND P3.0

Description The SIF - clock output is not available at port P2.7 when setting P2.7 as secondary

function and output as described in data sheet

Workaround Also set P3.0 to alternate function and output. The SIF clock signal is then available at

P2.7.

PORT5 PORT Module

Category Functional

Function SIF comparator output is not available at P6.3

Description The SIF comparator output is not available at port P6.3 when setting P6.3 as secondary

function and output as described in data sheet

Workaround None

PORT7 PORT Module

Category Functional

Function SIFDAC output function not available at P6.6

Description The SIFDAC output is not available at port P6.6 when setting P6.6 as secondary

function and output as described in data sheet

Workaround None

TA12 TIMER_A Module

Category Functional

Function Interrupt is lost (slow ACLK)

Description Timer_A counter is running with slow clock (external TACLK or ACLK)compared to

MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer_A counter has incremented again. Therefore the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1).

This interrupt gets lost.

Workaround Switch capture/compare mode to capture mode before the CCRx register increment.

Switch back to compare mode afterwards.

TA16 TIMER_A Module

Category Functional

Function First increment of TAR erroneous when IDx > 00

Description The first increment of TAR after any timer clear event (POR/TACLR) happens



immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround None

TA21 TIMER_A Module

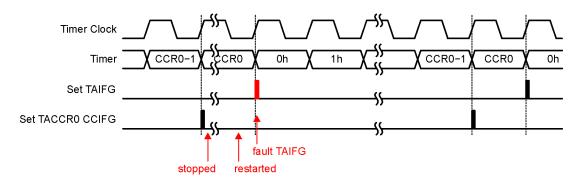
Category Functional

Function TAIFG Flag is erroneously set after Timer A restarts in Up Mode

Description In Up Mode, the TAIFG flag should only be set when the timer counts from TACCR0 to

zero. However, if the Timer A is stopped at TAR = TACCR0, then cleared (TAR=0) by setting the TACLR bit, and finally restarted in Up Mode, the next rising edge of the

TACLK will erroneously set the TAIFG flag.



Workaround None.

TAB22 TIMER A/TIMER B Module

Category Functional

Function Timer_A/Timer_B register modification after Watchdog Timer PUC

Description Unwanted modification of the Timer_A/Timer_B registers TACTL/TBCTL and TAIV/TBIV

can occur when a PUC is generated by the Watchdog Timer(WDT) in Watchdog mode

and any Timer A/Timer B counter register TACCRx/TBCCRx is

incremented/decremented (Timer_A/Timer_B does not need to be running).

Workaround Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC

may not fully initialize the register). TAIV/TBIV is automatically cleared following this

initialization.

Example code:

MOV.W #VAL, &TACTL

or

MOV.W #VAL. &TBCTL

Where, VAL=0, if Timer is not used in application otherwise, user defined per desired

function.



WDG2 WDT Module

Category Functional

Function Incorrectly accessing a flash control register

Description If a key violation is caused by incorrectly accessing a flash control register, the watchdog

interrupt flag is set in addition to the expected PUC.

Workaround None

XOSC9 XOSC Module

Category Functional

Function XT1 Oscillator may not function as expected in HF mode

Description XT1 oscillator does not work correctly in high frequency mode at supply voltages below

2.0V with crystal frequency > 4MHz.

Workaround None. When XT1 oscillator is used in HF mode with crystal frequency > 4MHz ensure a

supply voltage > 2.2V.



7 Document Revision History

Changes from family erratasheet to device specific erratasheet.

- 1. Errata PORT4 was added
- 2. Errata PORT5 was added
- 3. Errata PORT7 was added
- 4. Revision D was removed
- 5. Revision C was added

Changes from device specific erratasheet to document Revision A.

1. Errata EEM20 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. Errata TA21 was added to the errata documentation.

Changes from document Revision B to Revision C.

1. Package Markings section was updated.

Changes from document Revision C to Revision D.

1. TA21 Description was updated.

Changes from document Revision D to Revision E.

- 1. Function for CPU4 was updated.
- 2. Workaround for CPU4 was updated.

Changes from document Revision E to Revision F.

- 1. Erratasheet format update.
- 2. Added errata category field to "Detailed bug description" section

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