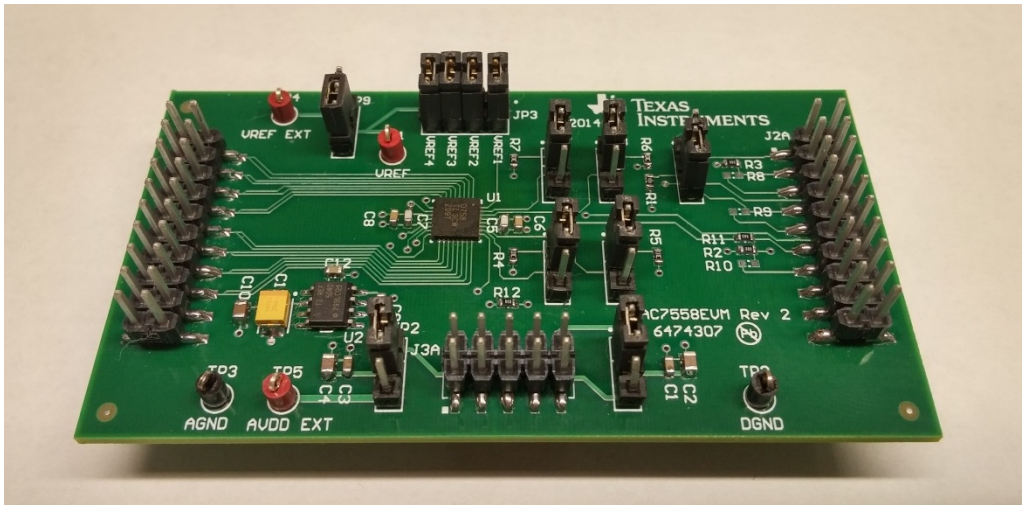
DAC7558 Evaluation Module



This user's guide describes the characteristics, operation, and use of the DAC7558EVM. The evaluation module (EVM) is a board designed to showcase the features and functionalities of the DAC7558. The DAC7558 is a low-power, voltage-output, 12-bit, octal channel digital-to-analog converter (DAC). This converter is controlled through a serial peripheral interface (SPI) that can operate at clock rates of up to 50 MHz. Additionally, the EVM includes a +4.096 V external reference voltage, giving a full-scale output that ranges from 0 V to +4.096 V. The EVM allows evaluation of all aspects of the device and allows user control over every pin on the DAC7558. Complete circuit descriptions, schematic diagrams, and a bill of materials (BOM) are included in this document.

The following related documents are available for download through the Texas Instruments web site at http://www.ti.com.

EVM-Related Device Datasheets

Device	Literature Number
DAC7558	SLAS435A
REF5040	SBOS410F

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1 EVM Overview

1.1 Features

- Full-featured evaluation board for the DAC7558
- Onboard external reference selection
- Wide selection of digital and I/O voltages
- Hardware and software control logic
- Compatible with the TI Modular EVM Motherboard MMB0

1.2 Introduction

The DAC7558 is a low-power, voltage-output, octal channel DAC that operates from a single +2.7- to +5.5-V supply. The DAC is controlled through a serial peripheral interface (SPI) that can operate at clock rates of up to 50 MHz. The EVM is designed to highlight the features and the performance of the 12-bit DAC. Additionally, the EVM includes a +4.096 V external reference voltage, giving a full-scale output that ranges from 0 V to +4.096 V.

The DAC7558EVM is designed to give easy access to all pins on the DAC7558. The evaluation module allows user control of the DAC logic using onboard jumpers, or digitally through the J2 header. By default, the evaluation module is configured to be used with an onboard +4.096 V external reference, but can be easily modified to use the DAC internal reference by changing a jumper setting and enabling the internal reference using software.

1.3 Electrostatic Discharge Warning

Many of the components on the EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

1.4 Power Requirements

1.4.1 Supply Voltage Ranges

Table 1 lists the supply voltage ranges.

Table 1. Supply Voltage Ranges

Signal	Location	Range
VDD	JP2.2	+2.7 V to +5.5 V
IOVDD	JP1.2	+2.7 V to +5.5 V
VREF1/2/3/4	JP3.2/4/6/8	0 V to VDD
REF5040_VIN	J3A.3	+2.7 V to +15 V

1.4.2 Motherboard Supply Mode

If you are using the MMB0 motherboard, it can supply the digital interface as well as the supply voltages required by the DAC7558EVM. The motherboard uses the DXP software found at http://www.ti.com/tool/dxp.

1.4.3 Standalone Supply Mode

The DAC7558EVM can be used without a motherboard, provided that the digital interface is driven by an external source. The supply voltages must be applied according to Table 1.

1.4.4 Reference Voltage

The EVM includes an on-board reference as well as the option to provide an external reference voltage. JP9 chooses between the on-board reference and the external reference. TP1 can be used to measure the selected reference, which is the on-board reference by default. JP3 can be used to supply different reference voltages to each VREF group.

1.5 EVM Default Hardware Setup

Table 2 lists the default jumper settings for the DAC7558EVM.

Table 2. Default Jumper Settings for the DAC7558EVM

Jumper	Position
JP1	1-2
JP2	1-2
JP3	1-2
	3-4
	5-6
	7-8
JP4	1-2
JP5	1-2
JP6	2-3
JP7	1-2
JP8	1-2
JP9	2-3

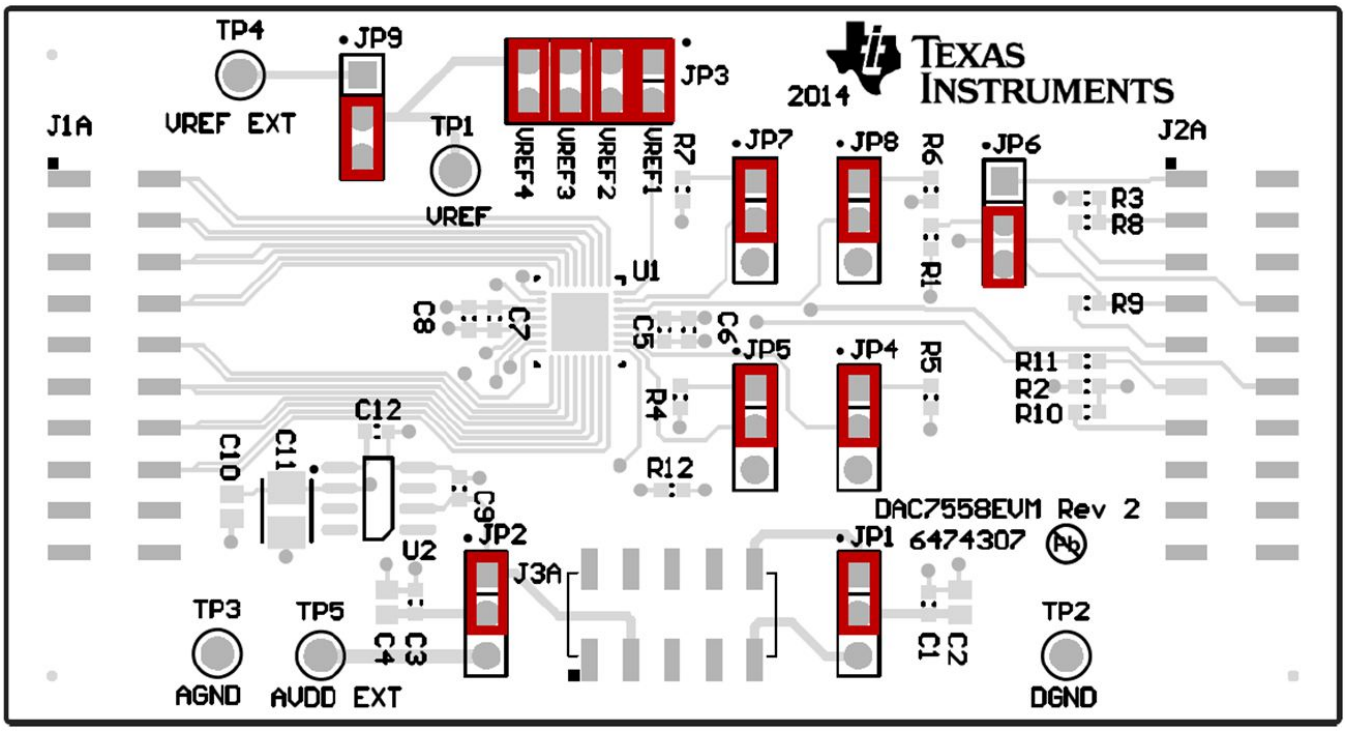

Figure 1. Default Jumper Placement for the DAC7558EVM

1.6 Questions and Support for This or Other Precision Data Converter EVMs

Join TI's E2E precision data converter support forum at http://e2e.ti.com/support/data_converters/precision_data_converters.

Post your question in the forum and one of our experts will help you answer it.

2 EVM Operation

2.1 Hardware Interface

Table 3 lists the EVM hardware description.

Table 3. Hardware Description

Jumper	Default Position	Description
JP1	1-2	When JP1 is in the 1-2 position, IOVDD receives +5 V from the motherboard. When JP1 is in the 2-3 position, IOVDD receives +3.3 V from the motherboard.
JP2	1-2	When JP2 is in the 1-2 position, VDD receives +5 V from the motherboard. When JP2 is in the 2-3 position, VDD uses an external supply.
JP3	1-2 3-4 5-6 7-8	Each reference group has the option of having its jumper CLOSED or OPEN. When the jumper is CLOSED, the reference group uses the on-board reference. When the jumper is OPEN, the reference group can use an external reference at JP3.2/4/6/8 for VREF1/2/3/4, respectively.
JP4	1-2	When JP4 is in the 1-2 position, PD is disabled. When JP4 is in the 2-3 position, PD is enabled.
JP5	1-2	When JP5 is in the 1-2 position, DCEN is disabled. When JP5 is in the 2-3 position, DCEN is enabled.
JP6	2-3	When JP6 is in the 1-2 position, SYNC is provided from J2.1. When JP6 is in the 2-3 position, SYNC is provided from J2.7.
JP7	1-2	When JP7 is in the 1-2 position, RST is disabled. When JP7 is in the 2-3 position, RST is enabled.
JP8	1-2	When JP8 is in the 1-2 position, RSTSEL is set to mid-scale. When JP8 is in the 2-3 position, RSTSEL is set to zero-scale.
JP9	2-3	When JP9 is in the 1-2 position, VREF uses the on-board reference. When JP9 is in the 2-3 position, VREF uses an external reference.

NOTE: For more details refer to the Schematic.

2.2 Digital Interface Options

Some of the hardware options can also be controlled through software, when the jumpers are in their default positions.

Table 4. Software Description

Jumper	Default Position	Description
JP4	1-2	When JP4 is in the 1-2 position, PD has a pullup resistor and can be controlled by software. When JP4 is in the 2-3 position, PD is enabled.
JP5	1-2	When JP5 is in the 1-2 position, DCEN has a pullup resistor and can be controlled by software. When JP5 is in the 2-3 position, DCEN is enabled.
JP7	1-2	When JP7 is in the 1-2 position, RST has a pullup resistor and can be controlled by software. When JP7 is in the 2-3 position, RST is enabled.
JP8	1-2	When JP8 is in the 1-2 position, RSTSEL has a pullup resistor and can be controlled by software. When JP8 is in the 2-3 position, RSTSEL is set to zero-scale.

2.3 Quick-Start

This section explains a quick way to test the EVMs functionality without using a motherboard.

The minimum requirements are:

1. An external source to provide the SPI master signals
2. An external +5-V power supply
3. A DC digital multimeter

Use the following steps:

1. Ensure that all of the jumpers are in their default position.
2. Ensure that all the power supplies are switched off.
3. Connect the power supply ground to any of the ground leads on the EVM board. (that is, TP2 and TP3)
4. Connect the SPI master ground to any of the ground leads on the EVM board.
5. Connect the DC DMM ground probe to any of the ground leads on the EVM board.
6. Connect +5 V to J3A.3.
7. Connect +5 V to J3A.10.
8. Connect the DC DMM signal probe to J1A.2.
9. Power-on the power supplies.
10. The DC DMM should display mid-scale +2.048 V. This means that your hardware setup is working.
    - If it does not, something may be wrong. Please check your connections and the jumper settings.
11. Send the SPI code 0x10FFF0.
12. The DC DMM should display full-scale +4.096 V. This means that your hardware and software setup are working.
    - If it does not, something may be wrong. Please check your digital interface implementation by looking at the digital signals on a signal analyzer or an oscilloscope.

3 Schematic, Printed-Circuit Board (PCB), and Bill of Materials

3.1 Schematic

Figure 2 shows the schematic for the DAC7558EVM board.

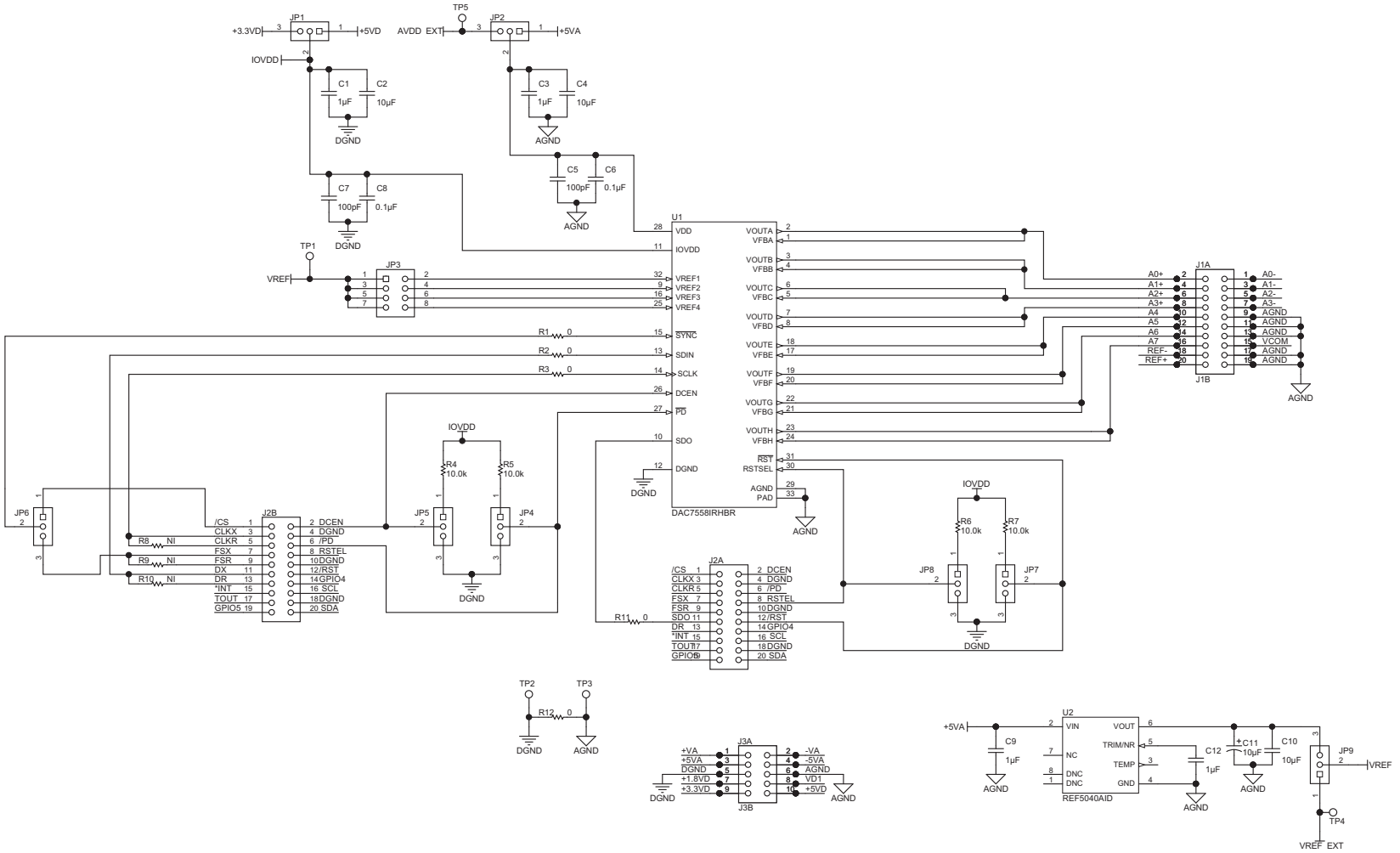

Figure 2. DAC7558EVM Schematic

3.2 PCB

Figure 3 shows the PCB layout and component placement for the DAC7558EVM board.

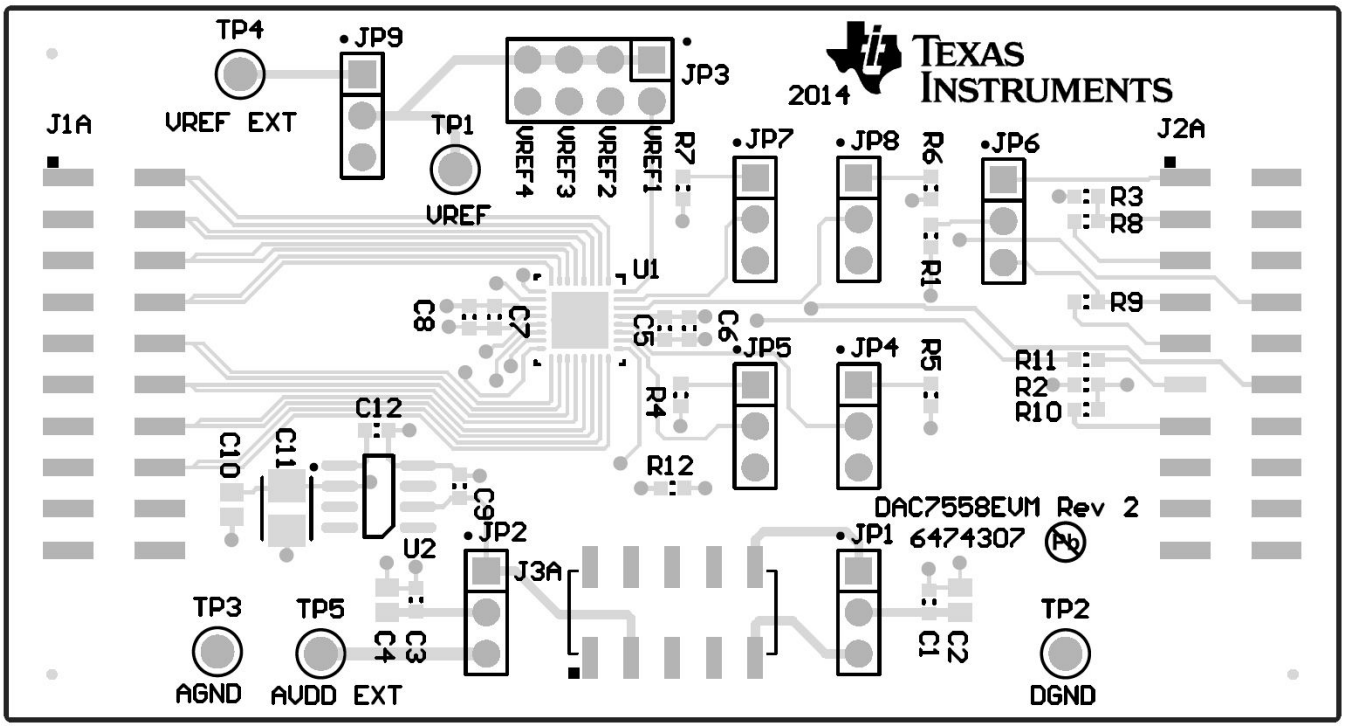

Figure 3. DAC7558EVM PCB Top Layer Layout

3.3 Bill of Materials

Table 5 shows the PCB layout and component placement for the DAC7558EVM board.

Table 5. DAC7558EVM Bill of Materials

Designator	QTY	Description	Manufacturer	Part Number
!PCB	1	Printed Circuit Board	Any	6474307
C1, C3, C9, C12	4	CAP, CERM, 1 µF, 50 V, +/- 10%, X5R, 0603	Murata	GRM188R61H105KAALD
C2, C4, C10	3	CAP, CERM, 10 µF, 25 V, +/- 10%, X5R, 0805	TDK	C2012X5R1E106K125AB
C5, C7	2	CAP, CERM, 100 pF, 100 V, +/- 5%, C0G/NP0, 0603	Murata	GRM1885C2A101JA01D
C6, C8	2	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	Murata	GRM188R71H104KA93D
C11	1	CAP, TA, 10 µF, 16 V, +/- 10%, 0.8 ohm, SMD	AVX	TPSB106K016R0800
FID1, FID2, FID3	3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
J1A, J2A	2	Header, 100mil, 10x2, SMD	Samtec, Inc.	TSM-110-01-T-DV-P
J1B, J2B	2	Connector, Receptacle, 100mil, 10x2, Gold plated, SMD	Samtec, Inc.	SSW-110-22-F-D-VS-K
J3A	1	Header, 100mil, 5x2, SMD	Samtec, Inc.	TSM-105-01-T-DV-P
J3B	1	Connector, Header, 10-Pos (10x2), Receptacle, 100x100-mil Pitch	Samtec, Inc.	SSW-105-22-F-D-VS-K
JP1, JP2, JP4, JP5, JP6, JP7, JP8, JP9	8	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S
JP3	1	Header, 100mil, 4x2, Gold, TH	Samtec	TSW-104-07-G-D
R1, R2, R3, R11, R12	5	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA
R4, R5, R6, R7	4	RES, 10.0 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0710KL
R8, R9, R10	0	NI	Vishay-Dale	
TP1, TP4, TP5	3	Test Point, Miniature, Red, TH	Keystone	5000
TP2, TP3	2	Test Point, Miniature, Black, TH	Keystone	5001
U1	1	12-bit octal, ultralow glitch, voltage output digital-to-analog converter, RHB0032E	Texas Instruments	DAC7558IRHBR

Revision History

Changes from Original (September 2005) to A Revision **Page**

- Changed entire content and structure of the *DAC7558 Evaluation Module* user's guide for board revision 2..... 1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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