Application Note

TAx5x1x/TAx5x1x-Q1 Incremental ADC (IADC) - Operation and Applications

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ABSTRACT

This application note describes the operation of the TAx5x1x/TAx5x1x-Q1 devices in Incremental ADC (IADC) mode. This can be used to digitize slow moving or DC signals with averaging for applications such as sensing. This application note is relevant for the following devices:

- TAC5212, TAC5112
- TAA5212
- TAC5212-Q1, TAC5112-Q1

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Trademarks

1 Introduction

In audio applications, a dynamic analog signal is typically digitized continuously by a delta-sigma analog-to-digital converter (ADC) followed by a decimation filter. This makes sure that the moving signal is captured at a sampling rate that covers the signal bandwidth.

However, in non-audio applications such as sensing, delta-sigma ADCs are mainly used to provide low-noise measurements for DC or slow-moving signals.

This application note describes the different ways to configure the ADC in the TAx5x1x/TAx5x1x-Q1 devices as *Incremental ADCs* (IADCs) for such applications.

2 Detailed Description

2.1 What is an Incremental ADC (IADC)?

In a typical Audio ADC, the analog audio input signal is converted to digital by a delta-sigma modulator. The output of the modulator is then decimated to the required sampling rate and then sent to Audio Serial interface (ASI) bus. The ADC continuously digitizes the running audio input signal here, without resetting or flushing the memory of prior samples.

In applications like sensing, the measurements involve individually sampling very slow moving or noisy DC voltages. For such applications, the delta-sigma modulator digitizes the voltage into individual samples, and the device averages a certain number of captured samples and provides an output code. The number of samples that is averaged is the over-sampling ratio (OSR) of the ADC. In this mode of operation, referred to here as Incremental ADC (IADC), whenever a conversion is initiated, the internal memory is consistently reset and the ADC averages a freshly captured set of samples and provides the output digital code.

2.2 IADC Operation

Table 2-1, Table 2-2 and Table 2-3 list out the different registers for configuring IADC, describing the individual bit fields and their functionality.

The IADC mode is enabled by setting the IADC_EN bit in B0_P0_R81 register. The user initiates start of conversion in two ways:

1. For one-shot conversion, setting the IADC_CONVST_ONESHOT bit (B0_P0_R81[4] starts the conversion.
2. The CONVST (**CON**version **ST**art) signal can also be provided through a GPIO pin. To use GPIO1 as a CONVST signal for the IADC:
   a. Configure the GPIO1 pin as a general-purpose input (GPI) or any other input function be setting the GPIO1_CFG[3:0] field to 1(B0_P0_R10[7:4]).
   b. Enable IADC using GPIO1 by setting the IADC_CONVST_GPIO[1:0] field to 1 (B0_P0_R21[5:4]).

The IADC_ONESHOT_CONV_DONE_STS bit (B0_P0_R81[2]) gives out the status of completion of the IADC conversion.

The IADC operates in three distinct phases, which are described in further sections:

1. The RESET phase
2. The SKIP phase
3. The CONVERT phase

Table 2-1. IADC_CFG Register (Book 0, Page 0, Register 76)

Bit	Field	Type	Reset	Description
7-5	IADC_NSKIP_SEL[1:0]	R/W	001b	ADC N_{SKIP} configuration.
				0d = 384 mod clks
				1d = 576 mod clks
				2d = 896 mod clks
				3d = 1024 mod clks
				4d = 2048 mod clks
				5d = 4096 mod clks
				6d-7d = Reserved
4-3	IADC_NRESET_SEL[1:0]	R/W	01b	IADC N_{RESET} configuration.
				0d = 50 mod clks
				1d = 75 mod clks
				2d = 100 mod clks
				3d = 150 mod clks
2-1	IADC_OSR_SEL[1:0]	R/W	11b	IADC OSR select configuration.
				0d = 32
				1d = 64
				2d = 96
				3d = 128
0	RESERVED	R	0b	Reserved bits; Write only reset value

Table 2-2. IADC_CH_CFG Register (Book 0, Page 0, Register 81)

Bit	Field	Type	Reset	Description
7	IADC_EN	R/W	0b	IADC enable configuration.
				0d = IADC disabled
				1d = IADC enabled
6-5	IADC_MODE[1:0]	R/W	00b	IADC mode configuration. (for single channel mode channel select is controlled by ADC_INSRC_SE_MUX config)
				0d = One-shot single channel
				1d = One-shot multichannel
				2d = Sequential single channel
				3d = Sequential multichannel
4	IADC_CONVST_ONESHOT	R/W	0b	IADC conversion start one short configuration.
				0d = No conversion
				1d = Start one shot conversion
3	IADC_STOP_SEQ_CONV	R/W	0b	IADC stop sequential conversion configuration.
				0d = Sequential conversion running
				1d = Stop sequential conversion
2	IADC_ONESHOT_CONV_ DONE_STS	R/W	0b	IADC one shot conversion done configuration.
				0d = Conversion not done
				1d = One shot conversion done
1-0	RESERVED	R	0b	Reserved bits; Write only reset value

Table 2-3. INTF_CFG6 Register Field for IADC (Book 0, Page 0, Register 21)

Bit	Field	Type	Reset	Description
5-4	IADC_CONVST_GPIO[1:0]	R/W	00b	IADC conversion start using GPIO select configuration.
				0d = Enable IADC using GPIO is disabled
				1d = Enable IADC using GPIO1
				2d = Enable IADC using GPIO2
				3d = Enable IADC using GPI1

A Single IADC Conversion Cycle represents the sequence of operations when an IADC conversion is initiated. Each phase operates for a certain number of modulator clock cycles. Hence the total conversion time for the IADC is:

$$T_{CONV\_IADC} = \frac{N_{RESET} + N_{SKIP} + N_{CONV}}{ModulatorClockFrequency} \quad (1)$$

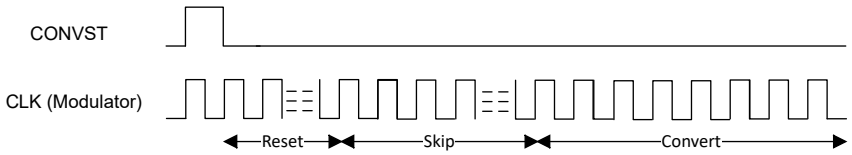


Figure 2-1. A Single IADC Conversion Cycle

2.2.1 RESET

When a conversion is initiated through either of the methods mentioned in IADC Operation, the IADC first enters the "RESET" phase. In this phase, the device resets the internal memory elements for the digital filters and the delta-sigma modulator. The device stays in this reset mode for N_{RESET} modulator clock cycles.

The N_{RESET} can be provided as an input in the register field B0_P0_R76[4:3], shown in Table 2-1.

2.2.2 SKIP

Once the modulator and digital filter memories are reset, the delta-sigma modulator starts converting the input voltage. However, the IADC digital filter skips the first N_{SKIP} samples for code computation. This is meant to enable DC inputs to settle to a steady state when sampling for code computation. The number of samples to be skipped can be programmed on the IADC_NSKIP_SEL[2:0] field (B0_P0_R76[7:5]), shown in Table 2-1.

2.2.3 CONVERT

After skipping the first N_{SKIP} samples, the IADC converts the input a further N_{OSR} modulator clock cycles, where OSR stands for Over-Sampling Ratio. These individual samples are stored in the internal memory and are then averaged to obtain the result. The N_{OSR} can be provided as an input in the register field B0_P0_R76[2:1], shown in Table 2-1.

At the end of the "CONVERT" phase, the digital output code is available for readback. Setting the IADC_DATA_IN_DIAG_REGS bit (B0_P1_R85[3]) enables storing of the 24-bit digital code into the following registers:

1. B0_P1_R98-100 contains the 24-bit digital code for IADC CH1.
2. B0_P1_R101-103 contains the 24-bit digital code for IADC CH2.
3. B0_P1_R104-106 contains the 24-bit digital code for IADC CH3.
4. B0_P1_R107-109 contains the 24-bit digital code for IADC CH4.

The 24-bit signed integer x can be used to calculate the input voltage by following the below equation:

$$v = \left(\frac{x*0.925}{2^{22}}*2*5.6569\right) + 1.375\ \text{V} \quad (2)$$

The input to the IADC can range from 0V to 5.6V for each pin.

2.3 IADC Modes of Operation

The IADC can operate in four different modes of operation, each selectable through the IADC_MODE field (B0_P0_R81[6:5]), shown in Table 2-2.

1. **One-shot Single Channel Mode:** In this mode of operation, the device does a single conversion on a single channel per ADC. Hence, for a stereo ADC, two channels are converted together. The conversion is initiated as described in IADC Operation, and the status of conversion can be monitored by reading the IADC_ONESHOT_CONV_ DONE_STS bit. The result can be read back on the registers described in CONVERT. The channel which is being converted is selected through the ADC_CHx_INSRC in SE_MUX mode (INxP/INxM).
2. **One-shot Multichannel Mode:** In this mode of operation, the device does a single conversion on all the input channels. For a stereo ADC, four inputs (IN1P, IN1M, IN2P, IN2M) are digitized. The conversion is initiated as described in IADC Operation, and the status of conversion can be monitored by reading the IADC_ONESHOT_CONV_ DONE_STS bit. The result can be read back on the registers described in CONVERT.
3. **Sequential Single Channel Conversion:** In this mode of operation the device continuously converts the input voltage from the selected channels. Setting the IADC_STOP_SEQ_CONV bit (B0_P0_R81[3]) stops this conversion. Clearing this bit again resumes the conversion. In sequential mode, the IADC automatically goes through the RESET-SKIP-CONVERT-RESET-SKIP… cycles.
4. **Sequential Multichannel Conversion:** In this mode of operation the device continuously converts the input voltage from all the input channels. Setting the IADC_STOP_SEQ_CONV bit (B0_P0_R81[3]) stops this conversion. Clearing this bit again resumes the conversion.

   Setting the HOLD_IADC_DATA (B0_P1_R85[2]) holds the previously converted data in the registers. After reading back these values, this bit can be cleared to enable register update with freshly converted values. Until this bit is cleared, the register does not get updated with any fresh conversion data.

2.4 Test Examples Using TAC5212EVM-K

This section contains example configuration scripts for IADC in various operational modes, with sample test results from a TAC5212EVM-K.

These examples are tested with the inputs shown in Figure 2-2.

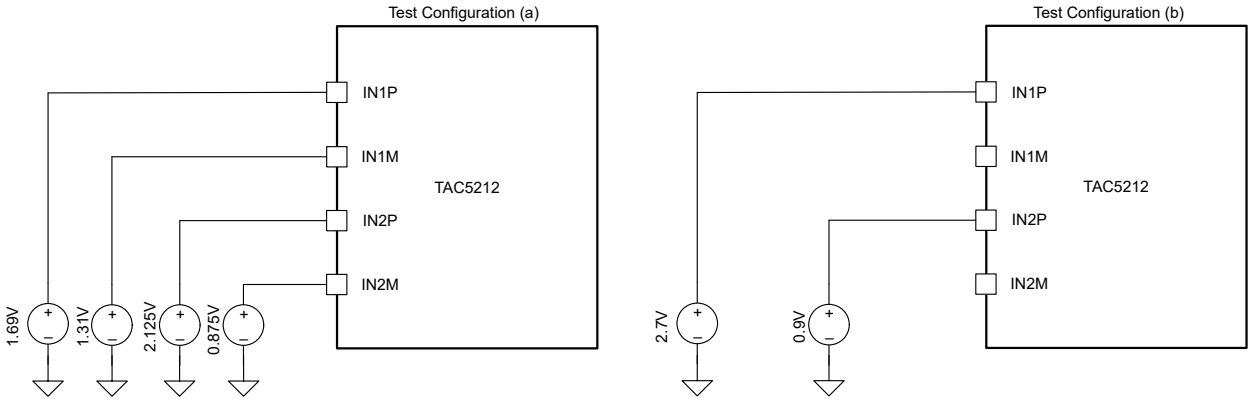


Figure 2-2. Test Setup for the Examples

Like any typical DC measurement system, the IADC is also subject to offset and gain errors. Hence, the user needs to calibrate these errors with the IADC also part of the system.

Figure 2-3 is a plot of the input voltage against the output of the IADC for each channel.

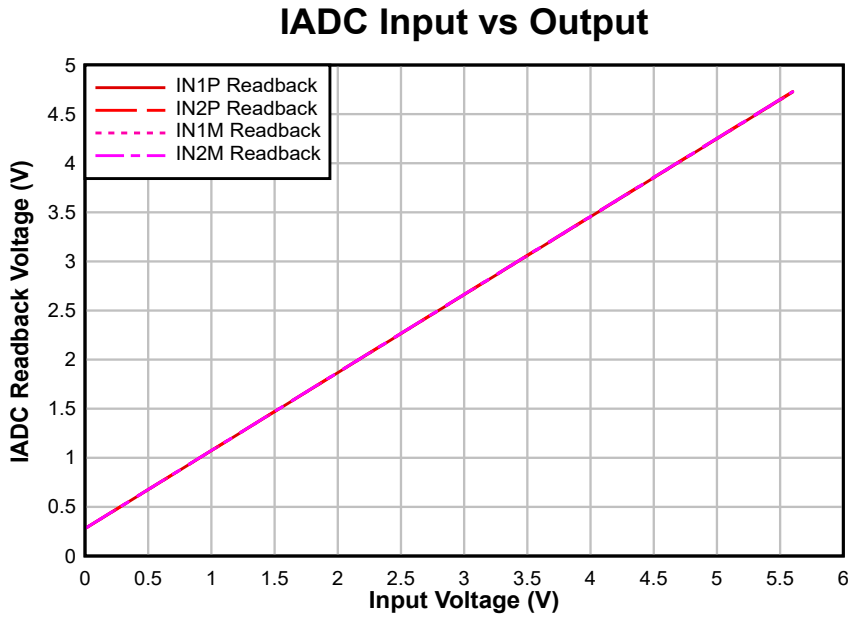


Figure 2-3. IADC Input vs Output Curve

The input *x* vs the output *y* follows a linear trend, with the graph fitting the equation:

$$y = mx + c \text{ V} \tag{3}$$

To obtain *m* and *c*

1. Set an input voltage x_1 (close, but not equal to 0V) and capture the IADC voltage "y_1".
2. Set an input voltage x_2 (close, but not equal to max voltage) and capture the IADC voltage "y_2".
3. Then:

$$\text{m} = \frac{y_2 - y_1}{x_2 - x_1} \text{ , and} \tag{4}$$

$$\text{c} = \text{y}_1 - mx_1 \text{ or} \tag{5}$$

$$\text{c} = \text{y}_2 - mx_2 \text{ .} \tag{6}$$

The calibrated IADC output y_{cal} for any measured value *y* can thus be calculated from the equation

$$y_{cal} = \frac{y - c}{m} \text{ V(cal)} \tag{7}$$

For the above graph, the average *m* and *c* across channels is 0.794V/V and 0.28V respectively.

2.4.1 One-Shot, Single Channel Conversion

In this test, the IADC is configured to run a single one-shot conversion, where the two ADCs of the TAC5212 convert the input DC voltage of two input channels set as per Figure 2-2(a).

The results corresponding to this example are listed in Table 2-4.

```
######################################################################
##### IADC Configured in One-Shot Single Channel Mode
w a0 00 00
w a0 01 01
w a0 02 09
d 10

#Configuration 1
w a0 50 88 #Channel 1 - DC-coupled, Single-ended MUX INP1 input
w a0 55 88 #Channel 1 - DC-coupled, Single-ended MUX INP2 input

#Configuration 2
#w a0 50 c8 #Channel 1 - DC-coupled, Single-ended MUX INM1 input
#w a0 55 c8 #Channel 1 - DC-coupled, Single-ended MUX INM2 input

#Configuration 3
#w a0 50 88 #Channel 1 - DC-coupled, Single-ended MUX INP1 input
#w a0 55 c8 #Channel 1 - DC-coupled, Single-ended MUX INM2 input

#Configuration 4
#w a0 50 c8 #Channel 1 - DC-coupled, Single-ended MUX INM1 input
#w a0 55 88 #Channel 1 - DC-coupled, Single-ended MUX INP2 input

#IADC Configurations
w a0 51 80 #Enable IADC in one-shot single channel mode
w a0 4c 2e #NSKIP = 576, NRESET = 75, OSR = 128

w a0 00 01 #Page 1
w a0 55 08 #Get IADC data in diags register
w a0 00 00
w a0 51 90 #Start one-shot conversion
w a0 76 f0
w a0 78 80 #Power up ADC

d 64
r a0 51 01 #Read conversion status
#Read IADC Locations
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00

d 64
r a0 51 01 #Read conversion status
#Read IADC Locations (will read same value since the conversion is one-shot)
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00

w a0 78 00 #Power down ADC
w a0 51 80 #Disable one-shot conversion
```

Table 2-4. Readback Values of IADC in One-Shot, Single-Channel Conversion

Configuration In Script	Readback Iteration	CH1 Readback	CH2 Readback
Configuration 1 {CH1 = IN1P, CH2 = IN2P}	1	1.620452V 1.689777V(cal) (0x03008C)	0.973501V 0.871903V(cal) (0xFB16D9)
	2	1.620452V 1.689777V(cal) (0x03008C)	0.973501V 0.871903V(cal) (0xFB16D9)
Configuration 2 {CH1 = IN1M, CH2 = IN2M}	1	1.316629V 1.307177V(cal) (0xFF493B)	1.968419V 2.123844V(cal) (0x074215)
	2	1.316629V 1.307177V(cal) (0xFF493B)	1.968419V 2.123844V(cal) (0x074215)
Configuration 3 {CH1 = IN1P, CH2 = IN2M}	1	1.618905V 1.687829V(cal) (0x02FBB4)	1.967531V 2.122727 V(cal) (0x073F4D)
	2	1.618905V 1.687829V(cal) (0x02FBB4)	1.967531V 2.122727V(cal) (0x073F4D)
Configuration 4 {CH1 = IN1M, CH2 = IN2P}	1	1.315406V 1.305637V(cal) (0xFF4567)	0.972039V 0.870063V(cal) (0xFB1245)
	2	1.315406V 1.305637V(cal) (0xFF4567)	0.972039V 0.870063V(cal) (0xFB1245)

2.4.2 One-Shot, Multichannel Conversion

In this test, the IADC is configured to run a single one-shot conversion, where the two ADCs of the TAC5212 convert the input DC voltage of all four input channels set as per Figure 2-2(a).

The results corresponding to this example are listed in Table 2-5.

```
########################################################################
##### IADC Configured in One-Shot Multi Channel Mode
w a0 00 00
w a0 01 01
w a0 02 09
d 10

#Configure ADC channels
w a0 50 88 #Channel 1 - DC-coupled, Single-ended MUX INP1 input
w a0 55 88 #Channel 1 - DC-coupled, Single-ended MUX INM1 input


#IADC Configurations
w a0 51 a0 #Enable IADC in one-shot multi channel mode
w a0 4c 6e #NSKIP = 1024, NRESET = 75, OSR = 128

w a0 00 01 #Page 1
w a0 55 08 #Get IADC data in diags register, hold IADC data till readback
w a0 00 00
w a0 76 f0
w a0 78 80 #Power up ADC

w a0 51 b0 #Start one-shot conversion
d 64
r a0 51 01 #Read conversion status
#Read IADC Locations
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00

d 64
r a0 51 01 #Read conversion status
```

```
#Read IADC Locations (will read same value since the conversion is one-shot)
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00

w a0 78 00 #Power down ADC
w a0 51 00 #Disable IADC
```

Table 2-5. Readback Values of IADC in One-Shot, Multichannel Conversion

Readback Iteration	CH1 Readback (IN1P)	CH2 Readback (IN2P)	CH3 Readback (IN1M)	CH4 Readback (IN2M)
1	1.615151V 1.683102V(cal) (0x02EFF3)	0.970523V 0.868155V(cal) (0xFB0D86)	1.313223V 1.303254V(cal) (0xFF3E91)	1.962638V 2.116962V(cal) (0x072FFB)
2	1.615151V 1.683102V(cal) (0x02EFF3)	0.970523V 0.868155V(cal) (0xFB0D86)	1.313223V 1.303254V(cal) (0xFF3E91)	1.962638V 2.116962V(cal) (0x072FFB)

2.4.3 One-Shot Conversion Using GPIO2

In this test, the IADC is configured to a one-shot, single-channel conversion. In this example, instead of initiating a conversion through I^2C write, the conversion is initiated by pulling the GPIO2 pin to HI. The two ADCs of the TAC5212 convert the input DC voltage of all four input channels set as per Figure 2-2(a).

The results corresponding to this example are listed in Table 2-6.

```
######################################################################
##### IADC Configured in One-Shot Mode using GPIO2
w a0 00 00
w a0 01 01
w a0 02 09
d 10

#Configure ADC channels
w a0 50 88 #Channel 1 - DC-coupled, Single-ended MUX INP1 input
w a0 55 88 #Channel 1 - DC-coupled, Single-ended MUX INP2 input

w a0 0b 10 #Configure GPIO2 as GPI
w a0 15 20 #Use GPIO2 to initiate conversion on IADC

#IADC Configurations
w a0 51 80 #Enable IADC in one-shot single channel mode
w a0 4c 6e #NSKIP = 1024, NRESET = 75, OSR = 128

w a0 00 01 #Page 1
w a0 55 08 #Get IADC data in diags register
w a0 00 00

w a0 76 f0
w a0 78 80 #Power up ADC

b #Breakpoint, Set GPIO2 to 1 here

r a0 51 01 #Read conversion status
#Read IADC Locations
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
w a0 00 00

b #Breakpoint, Set GPIO2 to 0 here
d 64

r a0 51 01 #Read conversion status
#Read IADC Locations (will read same value as above)
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
w a0 00 00
```

```
b #Breakpoint, Set GPIO2 to 1 here
d 64

r a0 51 01 #Read conversion status
#Read IADC Locations
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
w a0 00 00

b #Breakpoint, Set GPIO2 to 0 here
d 64

r a0 51 01 #Read conversion status
#Read IADC Locations (will read same value as above)
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
w a0 00 00

w a0 78 00 #Power down ADC
w a0 51 00 #Disable IADC
```

Table 2-6. Readback Values of IADC in One-Shot Single-Channel Conversion Using GPIO2

Readback Iteration	CH1 Readback	CH2 Readback
1 (GPIO2 = 1)	1.610549V 1.677306V(cal) (0x02E18A)	0.966599V 0.863218V(cal) (0xFB013D
2 (GPIO2 = 0)	1.610549V 1.677306V(cal) (0x02E18A)	0.966599V 0.863218V(cal) (0xFB013D)
3 (GPIO2 = 1)	1.606439V 1.672131V(cal) (0x02D4AB)	0.962487V 0.858043V(cal) (0xFAF45D)
4 (GPIO2 = 0)	1.606439V 1.672131V(cal) (0x02D4AB)	0.962487V 0.858043V(cal) (0xFAF45D)

2.4.4 Sequential, Single Channel Conversion

In this test, the IADC is configured to run continuous conversions until the conversion is stopped. The two ADCs of the TAC5212 convert the input DC voltage of two input channels set as per Figure 2-2(a).

The results corresponding to this example are listed in Table 2-7.

```
######################################################################
##### IADC Configured in Sequential Single Channel Mode
w a0 00 00
w a0 01 01
w a0 02 09
d 10

#Configure ADC channels
w a0 50 88 #Channel 1 - DC-coupled, Single-ended MUX INP1 input
w a0 55 88 #Channel 1 - DC-coupled, Single-ended MUX INP2 input

#IADC Configurations
w a0 51 c0 #Enable IADC in sequential single channel mode
w a0 4c 6e #NSKIP = 1024, NRESET = 75, OSR = 128

w a0 00 01 #Page 1
w a0 55 08 #Get IADC data in diags register
w a0 00 00
w a0 76 f0
w a0 78 80 #Power up ADC
d 64

#Read IADC Locations
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
```

```
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00

d 64

#Halt Sequential Conversion
w a0 00 00
w a0 51 c8
d 64

#Read IADC Locations
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00

d 64

#Read IADC Locations (will read same value since the conversion is stopped)
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00

w a0 78 00 #Power down ADC
w a0 51 00 #Disable IADC
```

Table 2-7. Readback Values of IADC in Sequential Single-Channel Conversion

Readback Iteration	CH1 Readback	CH2 Readback
1	1.611557V 1.678662V(cal) (0x02E4B2)	0.96794V 0.864857V(cal) (0xFB0570)
2 (Conversion halted here)	1.611194V 1.678205V(cal) (0x02E38F)	0.967111V 0.863814V(cal) (0xFB02D7)
3	1.611194V 1.678205V(cal) (0x02E38F)	0.967111V 0.863814V(cal) (0xFB02D7)

2.4.5 Sequential, Multichannel Conversion

In this test, the IADC is configured to run continuous conversions until the conversion is stopped. The two ADCs of the TAC5212 convert the input DC voltage of all four input channels set as shown in Figure 2-2(a).

The results corresponding to this example are listed in Table 2-8.

```
######################################################################
##### IADC Configured in Sequential Multi Channel Mode
w a0 00 00
w a0 01 01
w a0 02 09
d 10

#Configure ADC channels
w a0 50 88 #Channel 1 - DC-coupled, Single-ended MUX INP1 input
w a0 55 88 #Channel 1 - DC-coupled, Single-ended MUX INP2 input

#IADC Configurations
w a0 51 e0 #Enable IADC in sequential multi-channel mode
w a0 4c 6e #NSKIP = 1024, NRESET = 75, OSR = 128

w a0 00 01 #Page 1
w a0 55 08 #Get IADC data in diags register
w a0 00 00
w a0 76 f0
w a0 78 80 #Power up ADC
d 64
```

```
#Read IADC Locations
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00

d 64

#Read IADC Locations
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00

d 64

#Read IADC Locations
w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00

w a0 78 00 #Power down ADC
w a0 51 00 #Disable IADC
```

Table 2-8. Readback Values of IADC in Sequential, Multichannel Conversion

Readback Iteration	CH1 Readback (IN1P)	CH2 Readback (IN2P)	CH3 Readback (IN1M)	CH4 Readback (IN2M)
1	1.612474V 1.679731V(cal) (0x02E791)	0.969072V 0.866329V(cal) (0xFB08FB)	1.310879V 1.300301V(cal) (0xFF373A)	1.959433V 2.112929V(cal) (0x0725F2)
2	1.612131V 1.679299V(cal) (0x02E67E)	0.967906V 0.864862V(cal) (0xFB0554)	1.310251V 1.299510V(cal) (0xFF3543))	1.959676V 2.113234V(cal) (0x0726B5)
3	1.612001V 1.679135V(cal) (0x02E616)	0.968047V 0.865040V(cal) (0xFB05C5)	1.310327V 1.299606V(cal) (0xFF3580)	1.959466V 2.112970V(cal) (0x07260C)

2.4.6 Impact of OSR on the IADC Output

The below code is used to observe the effect of changing one of the IADC parameters, in this case, the OSR value. The voltages are set as per Figure 2-2, and the IADC output is measured 100 times. Figure 2-4 shows the impact on the measured values in time domain, while Figure 2-5 shows the same in a histogram.

```
######################################################################
##### IADC Configured to show the impact of OSR
w a0 00 00
w a0 01 01
w a0 02 09
d 10

#Configure ADC channels
w a0 50 88 #Channel 1 - DC-coupled, Single-ended MUX INP1 input
w a0 55 88 #Channel 1 - DC-coupled, Single-ended MUX INP2 input

#IADC Configurations
w a0 4c be #NSKIP = 4096, NRESET = 150, OSR = 128 - CHANGE OSR

w a0 51 c0 #Enable IADC in sequential single channel mode
w a0 00 01 #Page 1
w a0 55 08 #Get IADC data in diags register
w a0 00 00
w a0 76 f0
w a0 78 80 #Power up ADC
```

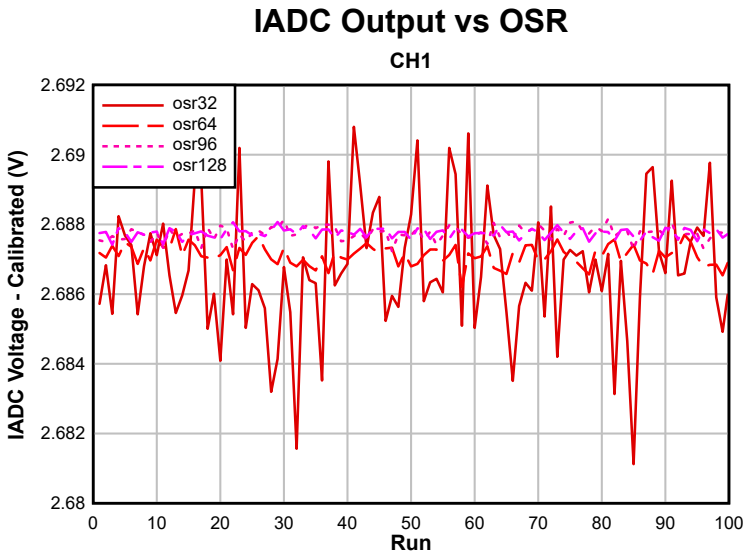
```
#Read IADC Locations (copy-paste below code snippet 100 times and capture the readback value)
##################################Copy from
here#################################################################
d 64

w a0 00 01 #Page 1
r a0 62 03 #IADC Channel 1
r a0 65 03 #IADC Channel 2
r a0 68 03 #IADC Channel 3
r a0 6b 03 #IADC Channel 4
w a0 00 00
##################################Till
here#################################################################

w a0 78 00 #Power Down ADC
w a0 51 00 #Disable IADC
```

Note that the results shown in Figure 2-4 and Figure 2-5 are the calibrated numbers calculated from the IADC output as described in Section 2.4.

(a) CH1 Voltage



(b) CH2 Voltage

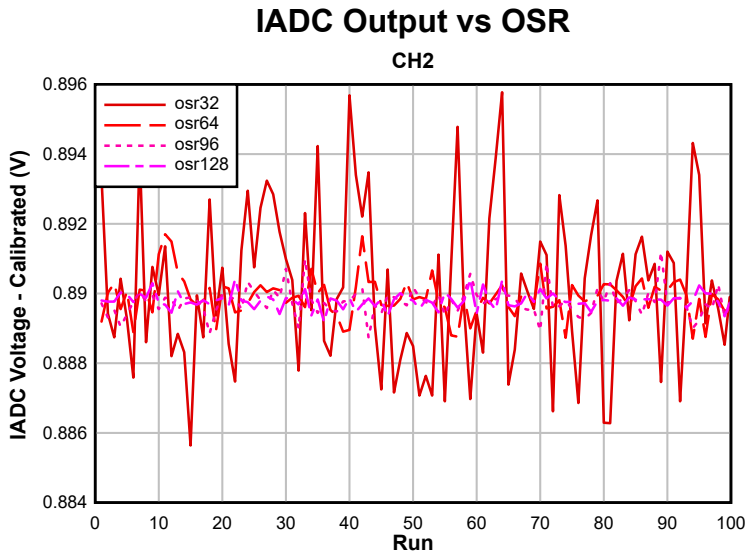
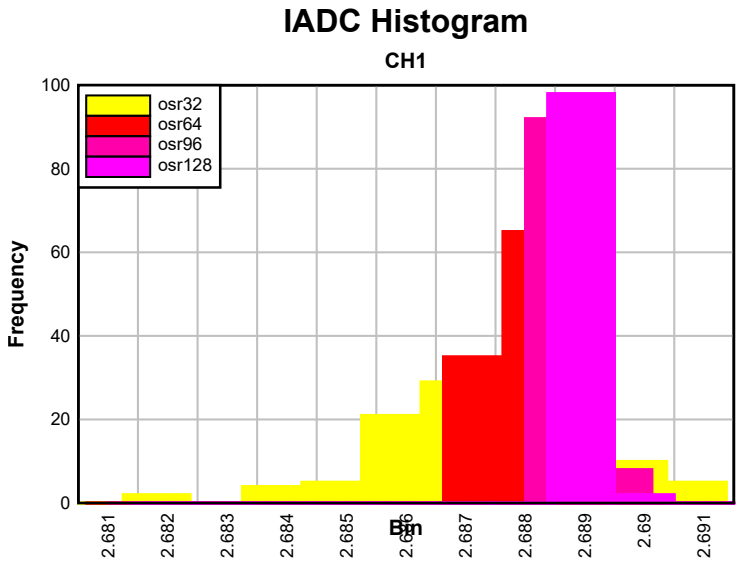


Figure 2-4. IADC Measurement across OSR

(a) CH1 Voltage



(b) CH2 Voltage

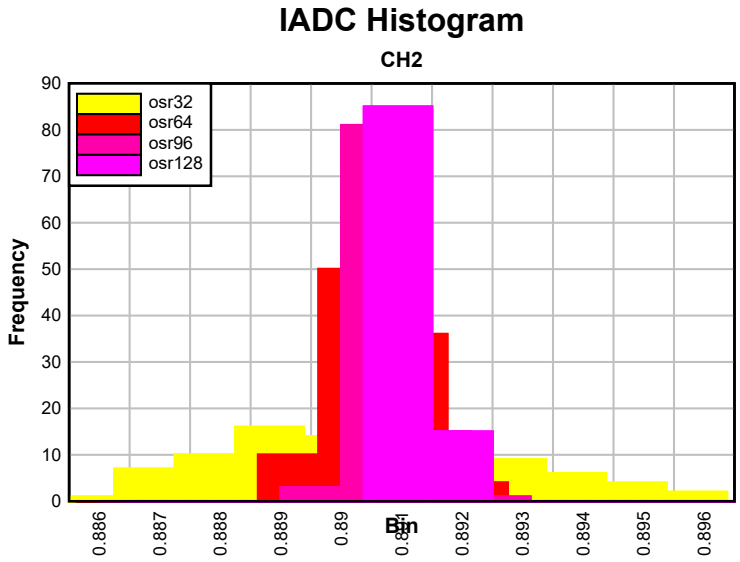


Figure 2-5. Distribution of IADC Measurement across OSR

3 Summary

This application note describes how the TAx5x1x/TAx5x1x-Q1 family of devices can be configured as Incremental ADCs. This application note is meant to showcase how the device can be used for DC measurement applications, both single channel and multichannel. This has been demonstrated using example configurations in the different operational modes, along with observations from each configuration.

4 References

1. Texas Instruments, *TAC5212 High-performance stereo audio codec with 119dB dynamic range ADC and 120dB dynamic range DAC*, datasheet.

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