*Functional Safety Information*

# *TPS763-Q1*
# *Functional Safety FIT Rate, FMD and Pin FMA*

## Table of Contents



## Trademarks

# 1 Overview

This document contains information for the TPS763-Q1 (SOT-23 (5) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

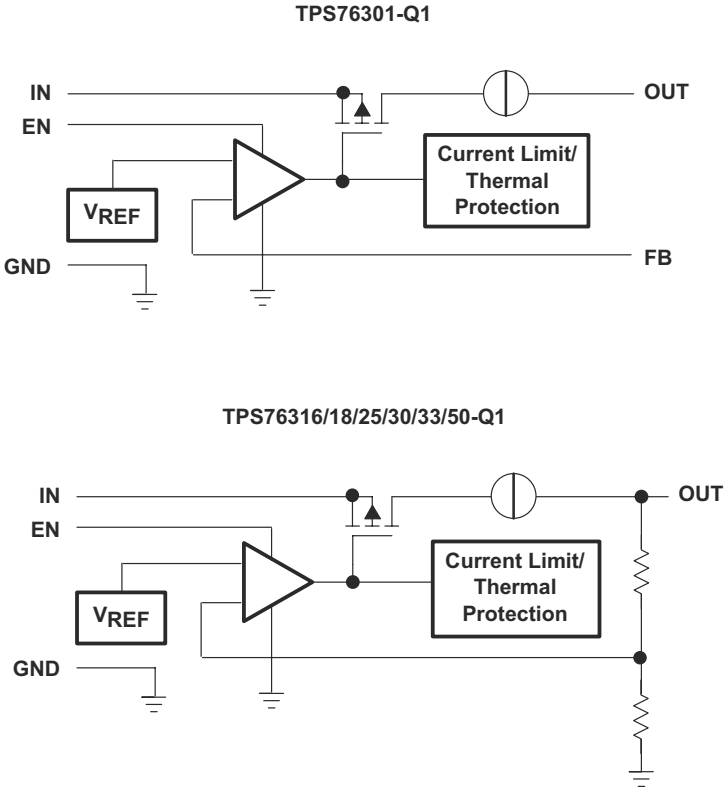


**Figure 1-1. Functional Block Diagram (Legacy Chip)**

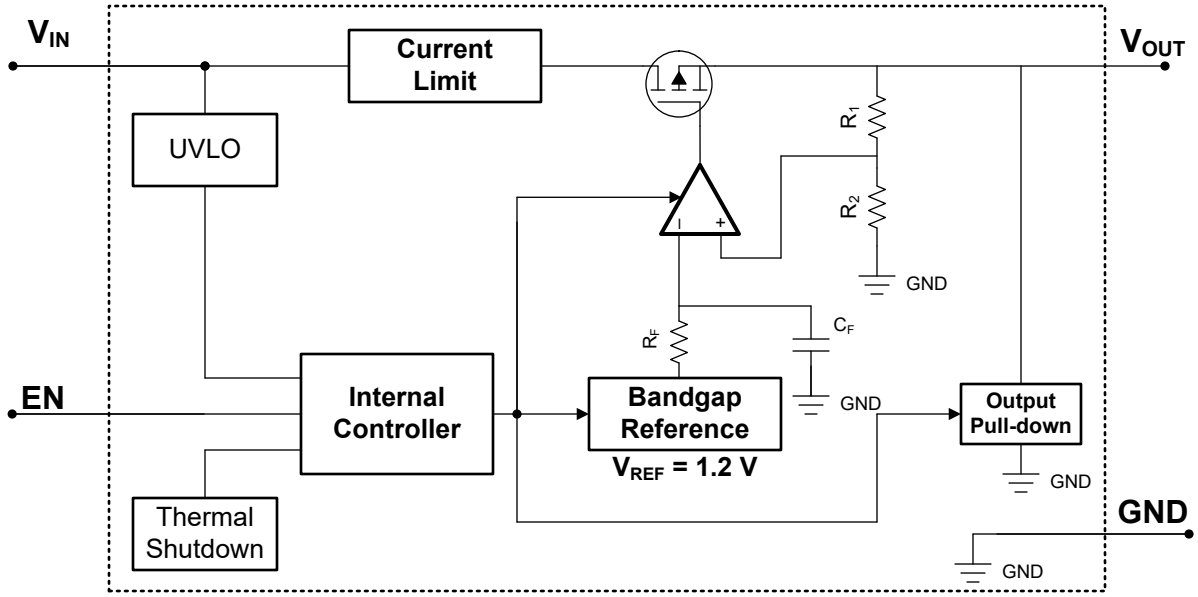


**Figure 1-2. Functional Block Diagram (New Chip, Fixed)**

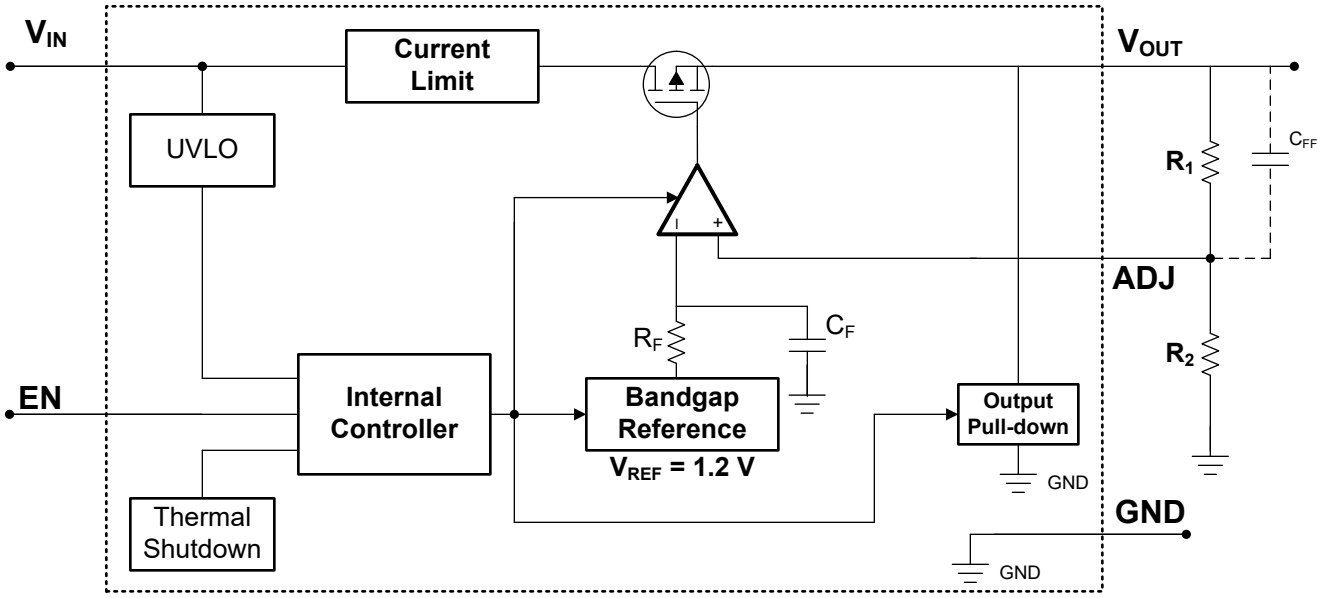


**Figure 1-3. Functional Block Diagram (New Chip, Adjustable)**

The TPS763-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS763-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total component FIT rate | 8 |
| Die FIT rate | 6 |
| Package FIT rate | 2 |

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 150mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog, or mixed | 25 FIT | 55°C |

The reference FIT rate and reference virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS763-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| No OUTPUT (Output low) | 50 |
| OUTPUT High (Following Input) | 10 |
| OUTPUT not in specification | 35 |
| Short circuit any two pins | 5 |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS763-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality. |
| B | No device damage, but loss of functionality. |
| C | No device damage, but performance degradation. |
| D | No device damage, no impact to functionality or performance. |

Figure 4-1 shows the TPS763-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS763-Q1 datasheet.

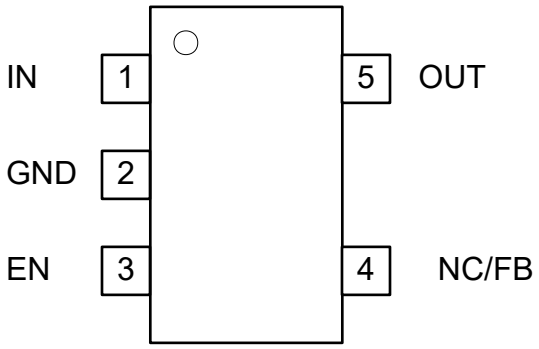


**Figure 4-1. Pin Diagram**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| IN | 1 | Power is not supplied to the device resulting in no output voltage. | B |
| GND | 2 | There is no effect on the device. The device operates as normal. | D |
| EN | 3 | The device is disabled resulting in no output voltage. | B |
| NC/FB | 4 | NC: There is no effect on the device. The device operates as normal.<br>FB: The device is in dropout. | D<br>B |
| OUT | 5 | The device is not operational when the output is pulled to GND. The current limit is triggered and the device can repeatedly enter and exit thermal shutdown depending on the magnitude of power dissipation. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| IN | 1 | Power is not supplied to the device resulting in no output voltage. | B |
| GND | 2 | A floating GND pin can result in incorrect voltage regulation or no output voltage. | B |
| EN | 3 | This is an undefined operation that can either enable or disable the device. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| NC/FB | 4 | NC: There is no effect on the device. The device operates as normal.<br>FB: The state of the device is unknown. If the device is on, the output voltage is indeterminate. | D<br>B |
| OUT | 5 | The load is disconnected but the device maintains regulation. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|---|
| IN | 1 | GND | Power is not supplied to the device resulting in no output voltage. | B |
| GND | 2 | EN | The device is disabled. | B |
| EN | 3 | NC/FB | NC: There is no effect on the device. The device operates as normal.<br>FB: If the enable voltage is greater than $V_{FB(ABS.\ MAX)}$, the device can become damaged. If the enable voltage is greater than or equal to $V_{EN(HIGH)}$, but less than or equal to $V_{FB(ABS.\ MAX)}$, there is no output voltage. If the enable voltage is less than $V_{EN(HIGH)}$, the device potentially disables resulting in no output voltage. | D<br>A |
| NC/FB | 4 | OUT | NC: There is no effect on the device. The device operates as normal.<br>FB: The device is in a unity gain configuration. | D<br>B |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| IN | 1 | There is no effect on the device. The device operates as normal. | D |
| GND | 2 | Power is not supplied to the device resulting in no output voltage. | B |
| EN | 3 | The device is enabled. | B |
| NC/FB | 4 | NC: There is no effect on the device. The device operates as normal.<br>FB: If the supply voltage is greater than $V_{FB(ABS.\ MAX)}$, the device can become damaged. If the supply voltage is greater than or equal to $V_{IN(MIN)}$, but less than or equal to $V_{FB(ABS.\ MAX)}$, there is no output voltage. If the supply voltage is below $V_{IN(MIN)}$, the device potentially disables resulting in no output voltage. | D<br>A |
| OUT | 5 | If the supply voltage is greater than 7V, the device can be damaged. If the supply voltage is greater than the nominal output voltage, then regulation is not possible. | A |

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from December 17, 2019 to December 1, 2025 (from Revision * (December 2019) to Revision A (December 2025))** **Page**

- Updated the document to the latest technical writing standard and style guide template..... 2
- Updated values in the *Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11* table..... 4

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